INTERNATIONAL CONFERENCE ON HIGH ENERGY PHYSICS

SEOUL, 04-11 JULY 2018

Imperial College London

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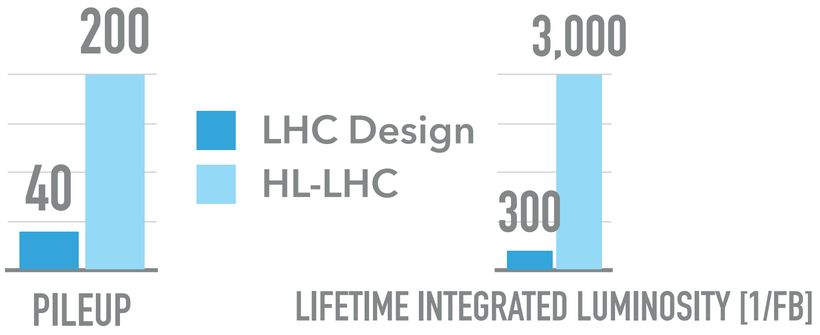
ON BEHALF OF CMS L1 TRACKING

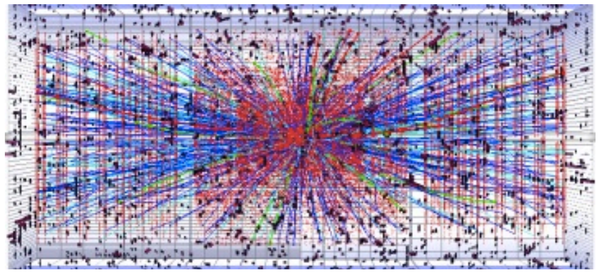
LEVEL-1 TRACK FINDING WITH AN ALL-FPGA SYSTEM AT CMS FOR THE HL-LHC

HIGH LUMINOSITY LHC

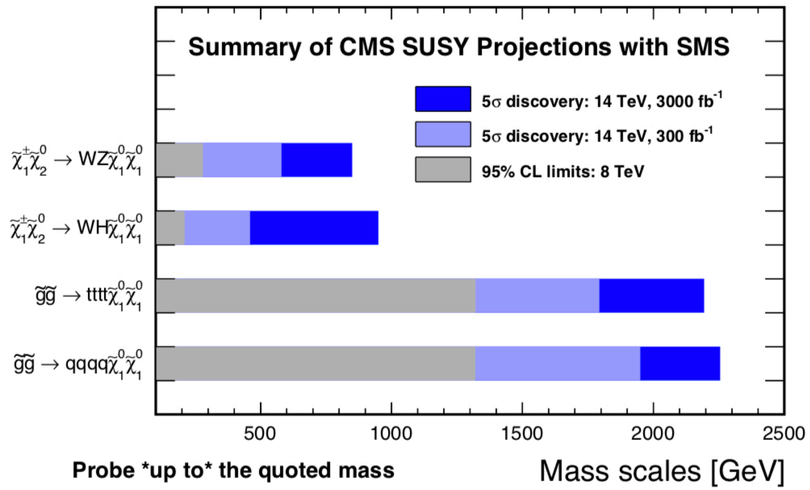
precision measurements, **push** search limits,
rare processes

- By **2026** (run 4) - LHC will be upgraded in luminosity -> 2-3x improved statistics by 2035 w.r.t no upgrade
- Silicon strip tracker will be replaced (radiation damage)
- **Challenging** high occupancy conditions, ~10,000 charged particles per bx
  - Must perform ≥ at present
  - Need completely **new handle** at L1 trigger, to keep rate < 750 kHz, while maintaining thresholds and sensitivity to interesting physics
  - **New tracker** design will allow read out of some data at 40 MHz

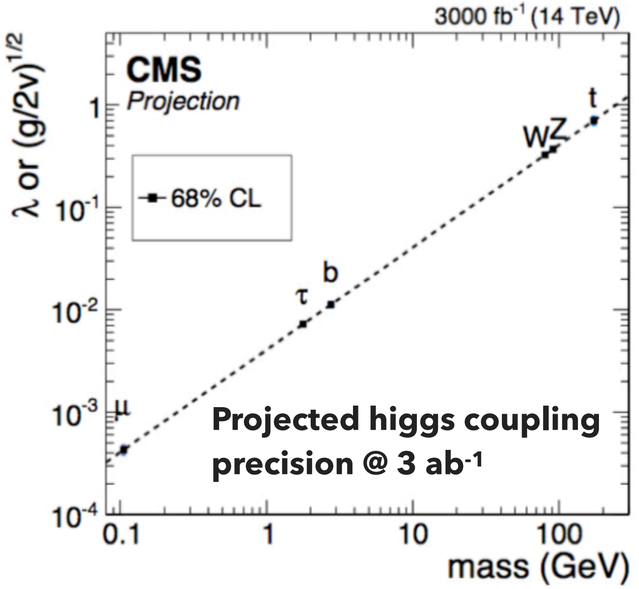




pileup 140 simulation



Probe *up to* the quoted mass



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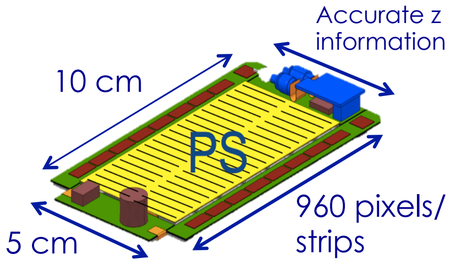
CMS TRACKER UPGRADE

"PS" Pixel + Strip Modules 20 < r < 60 cm



Strip Sensor × 2:
2. 5 cm × 100 μm

+

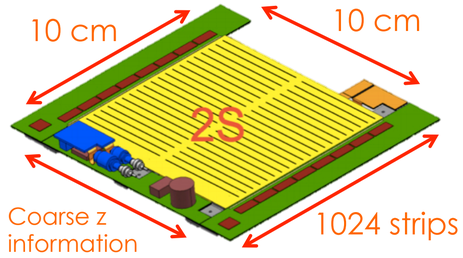
Pixel Sensor × 32:
1.5 mm × 100 μm

"2S" 2 Strip Modules r > 60 cm

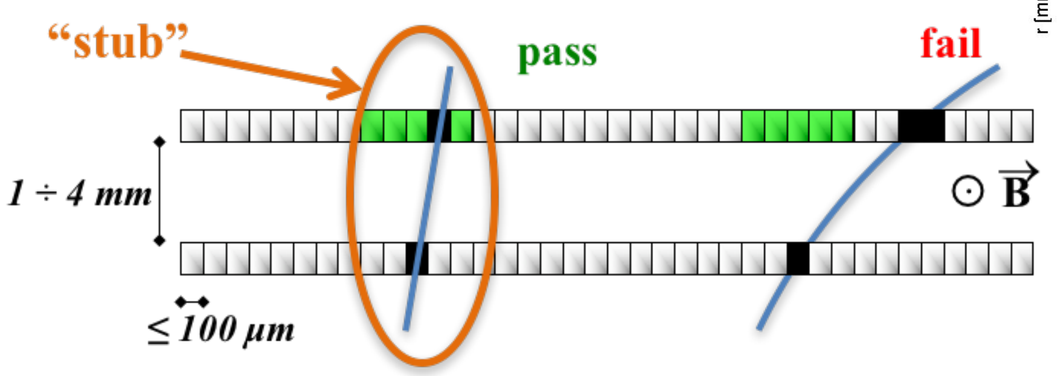
Strip Sensor × 2:
5 cm × 90 μm

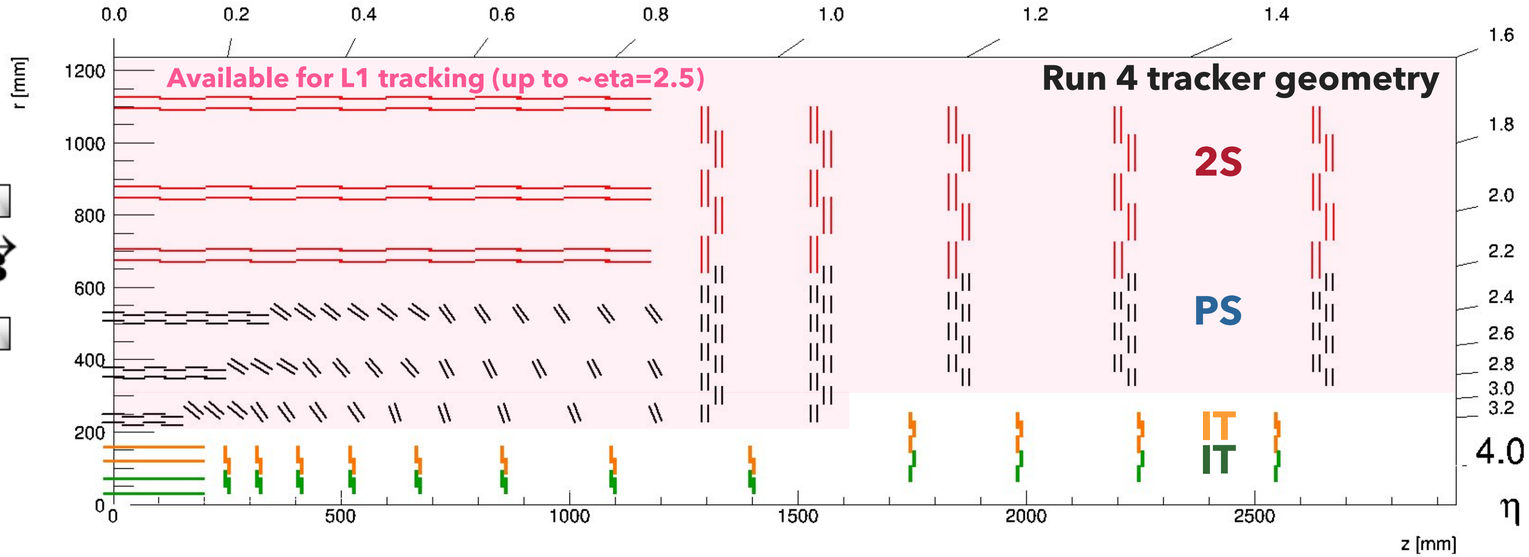
+

Strip Sensor × 2:
5 cm × 90 μm



- High p_T tracks signs of interesting physics (decays of high mass particles)
- Novel tracking modules utilise two 1.6 - 4.0 mm spaced silicon sensors, to discriminate p_T > 2-3 GeV
  - Forward these *stubs* to off-detector trigger electronics - rate reduction O(10) ~12,000 stubs per bx
- Tracks at L1: improved p_T resolution, possibility for vertex finding and track isolation





Exploring a variety of FPGA-based track-finding algorithms →

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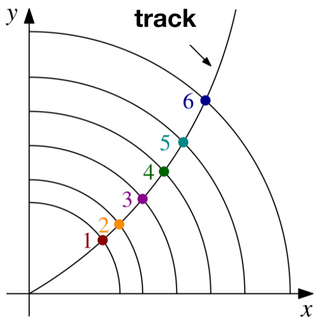
TRACK FINDING ALGORITHMS

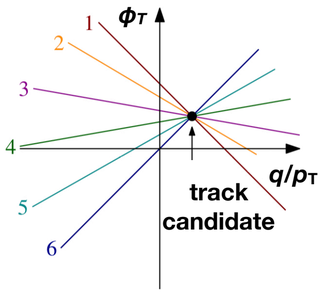
2D HOUGH TRANSFORM (HT)

- Widely used feature extraction technique to find imperfect instances of objects within a space e.g tracks in our tracker hit map
- Search for primary tracks in the r-φ plane, using the parameterisation (q/p_T, φ_0)
  - Stub positions correspond to straight lines in Hough Space
  - Where 4 or more lines intersect -> track candidate

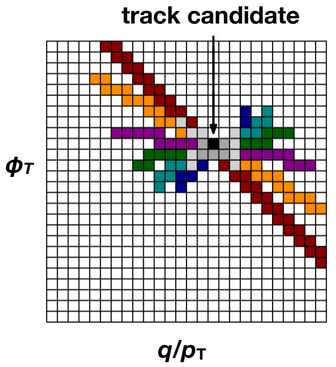
real space



hough space

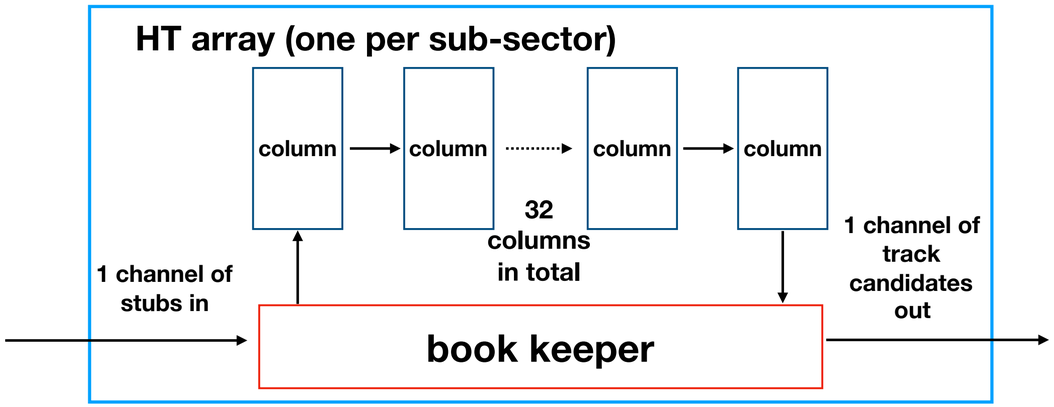


array in hough space



Each sub-sector (18 η, 18 φ) implemented as a fully independent, pipelined 32 x 64 array

p_T estimate from stacked modules used to constrain allowed q/p_T space



HT worker - simplified firmware diagram

1) Book keeper receives stubs and propagates to each q/p_T column in turn.

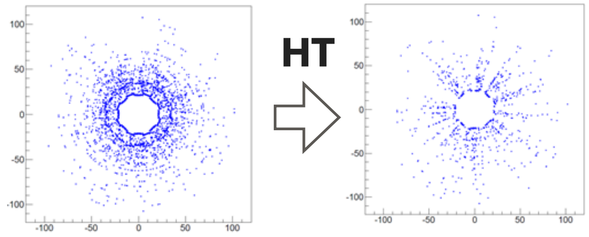
2) The corresponding **φ** of the stub for the column is calculated and the appropriate cell(s) are marked

3) Candidates marked with stubs from > 4 layers propagate back to the **Book Keeper for read-out**

200 PU

~12,000 stubs

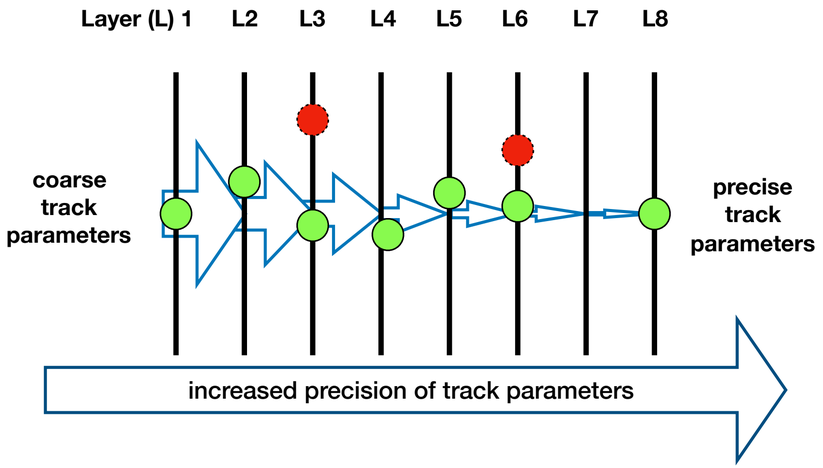
~270 track candidates

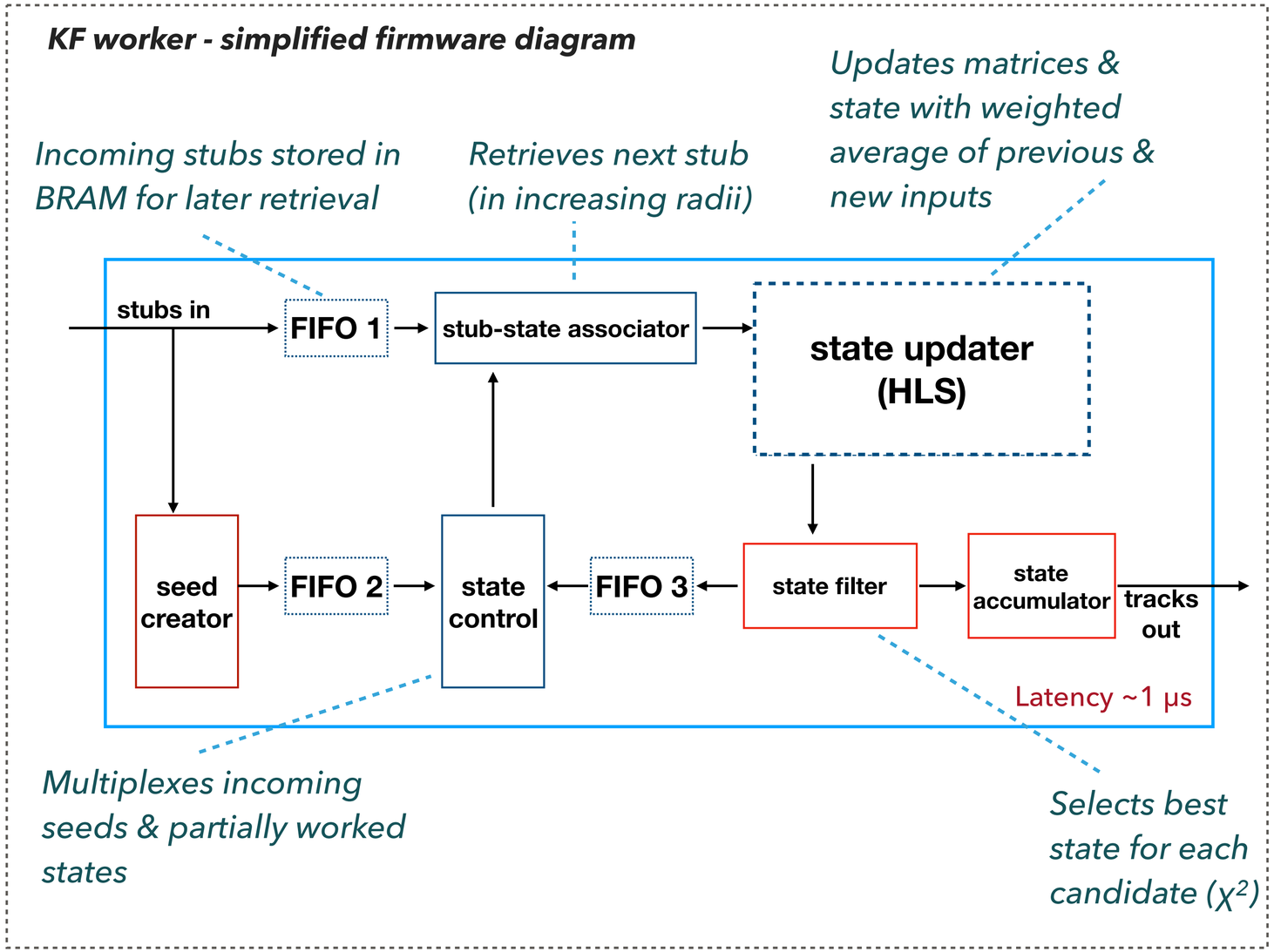


Latency ~1 μs including sort/pre-processing

3D KALMAN FILTER (KF)

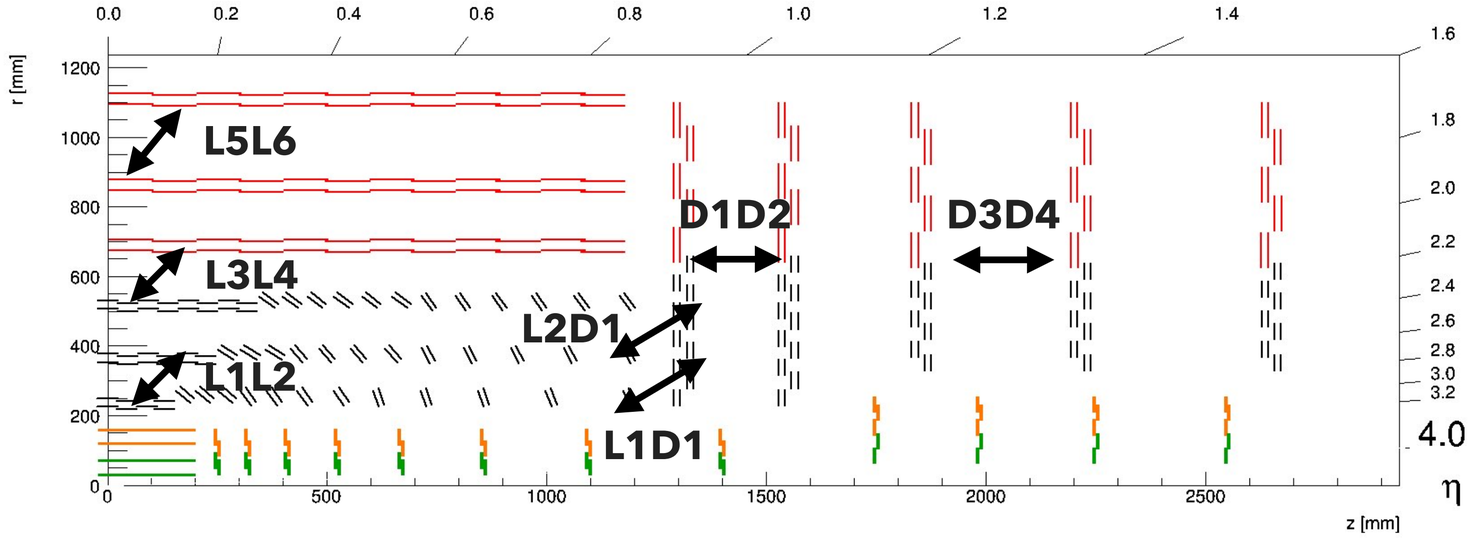
- Commonly used **iterative algorithm; series of measurements** containing inaccuracies and noise -> estimates of **unknown variables**
  1. Initial estimate of track parameters (HT seed) & their uncertainties
  2. Stub used to update state (weighted average)
  3. χ^2 calculated, used to reject false candidates, incorrect stubs on genuine candidates
  4. Repeat until all stubs are added

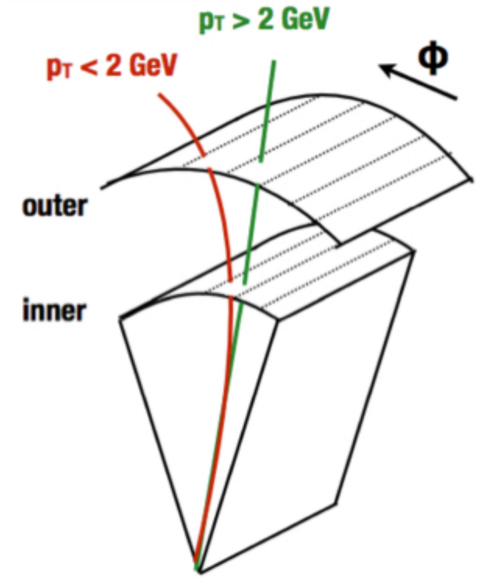


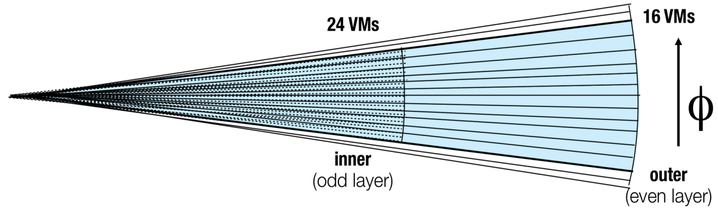


3D TRACKLET

- **Road search** algorithm
  - Tracker divided into up to 27 sectors in φ,
    - Each with an independent processing board
  - For parallel processing each sector is divided into 16-24 sub-divisions (virtual modules) in φ, full z
  - Only required virtual modules (consistent with track p_T > 2 GeV) are connected
- **Seeding**
  - Pair of adjacent layers used to form seed called a tracklet with a set of initial track parameters
  - Seeding done in multiple disk/layer pairs in parallel with built in redundancy







3D TRACKLET

- **Projection**
  - Tracklets + IP are projected to other layers
  - Matching stubs are identified
  - Calculate residuals between projection and matches stubs
- **Fit**
  - Linearized χ^2 fit used to calculate track params.
  - Utilises tracklet params and residuals
  - Complex calculations pre-computed and stored in look-up tables

corrections to tracklet parameters

$$\delta\eta = M^{-1}D^{T}V^{-1}\delta f^{m}$$

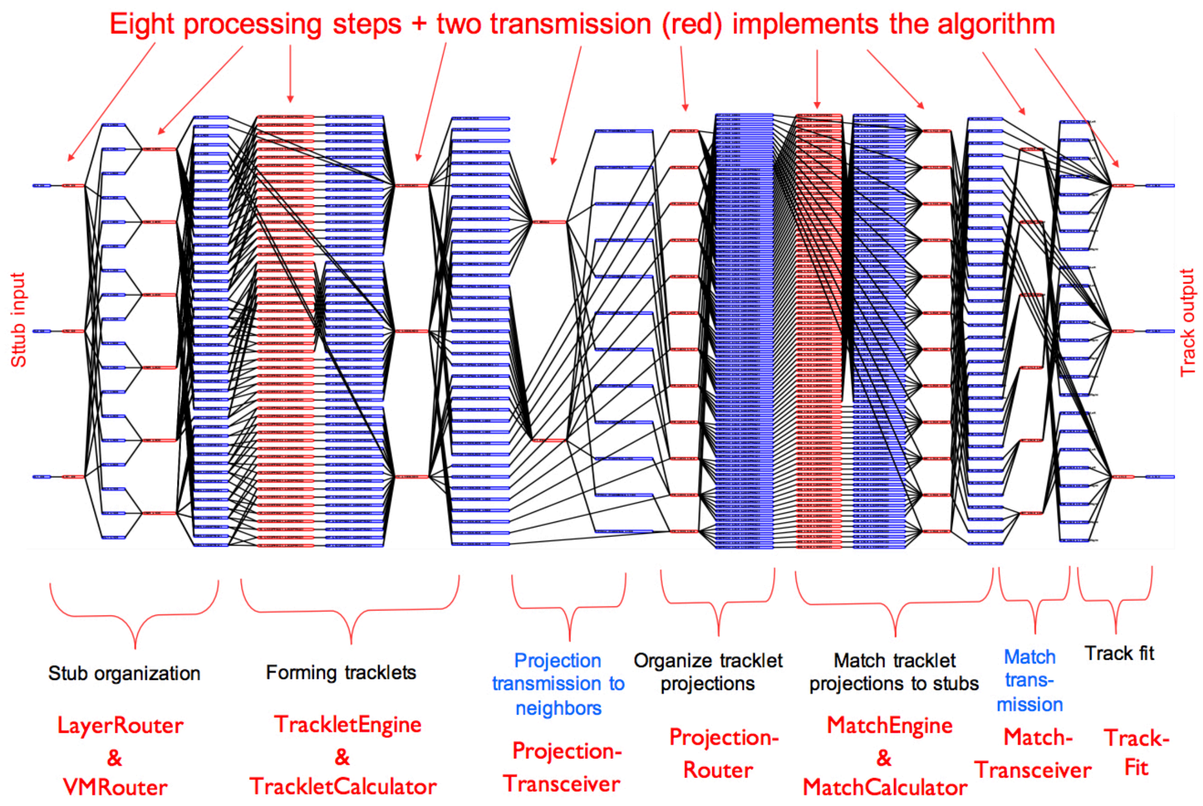
residuals

derivatives

$$M = D^{T}V^{-1}D$$

$$D_{ik} = \frac{\delta f_i}{\delta \eta_k}$$

Tracklet wiring diagram



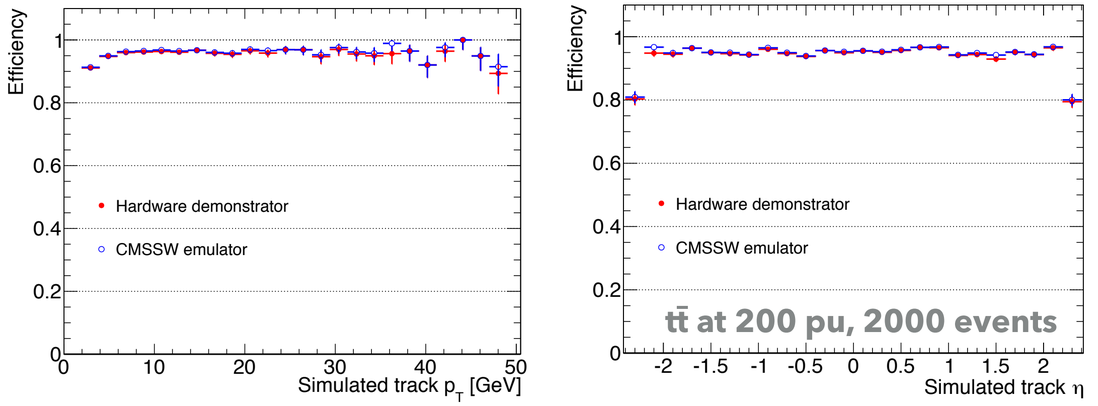
Tracklet algorithm latency ~2-3 μs

- **Duplicate Removal**
  - Check for tracks with shared stubs
  - Retain the one with the lowest χ^2/ndf

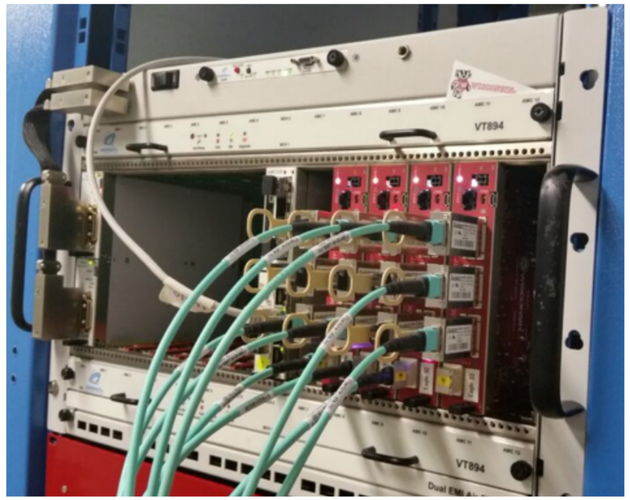
DEMONSTRATOR SYSTEMS

- HT, KF and Tracklet algorithms **proven** to work in **hardware demonstrators** within 3-4 μs
- Using μTCA boards with Virtex-7 FPGAs
- Objective - Run Monte-Carlo physics samples emulating conditions at HL-LHC through hardware demonstrator
- Compare hardware output directly with software emulator

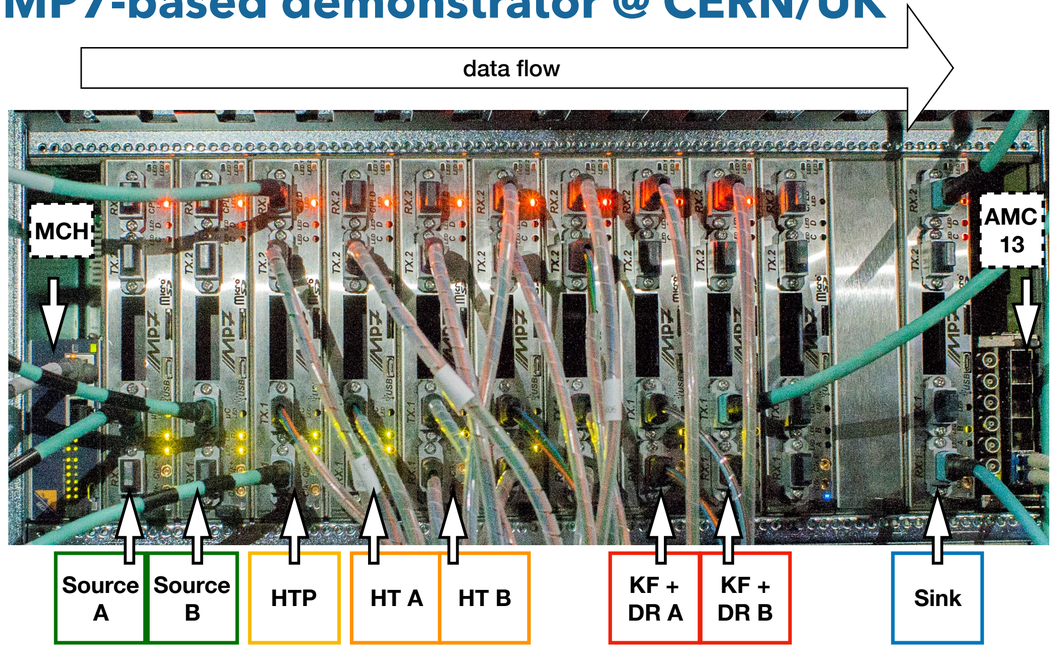
Excellent performance demonstrated in hardware



CTP7-based demonstrator @ CERN/Cornell



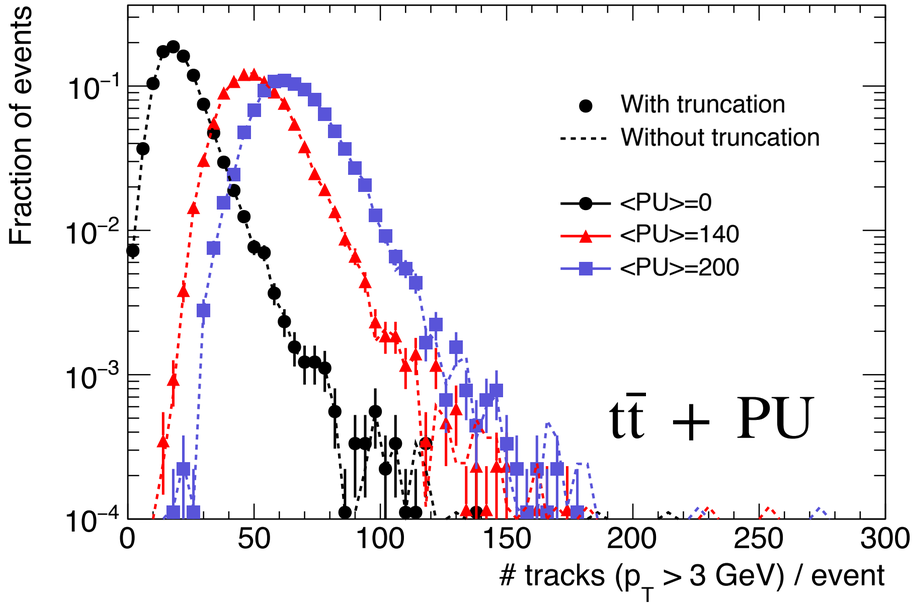
MP7-based demonstrator @ CERN/UK



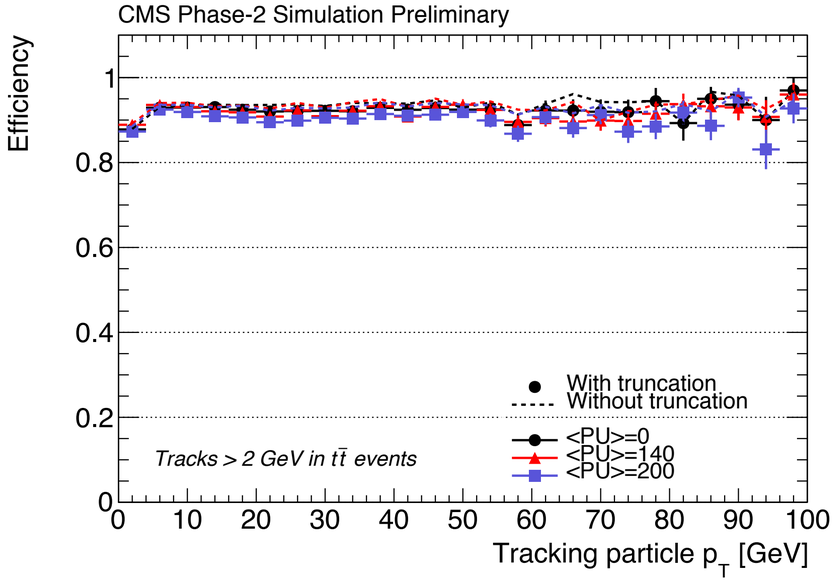
EMULATION RESULTS

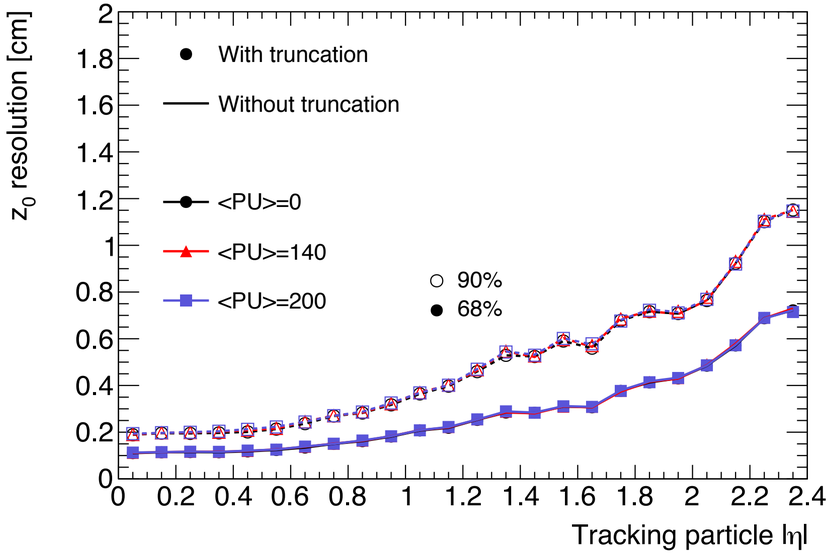
TRACK FINDING PERFORMANCE

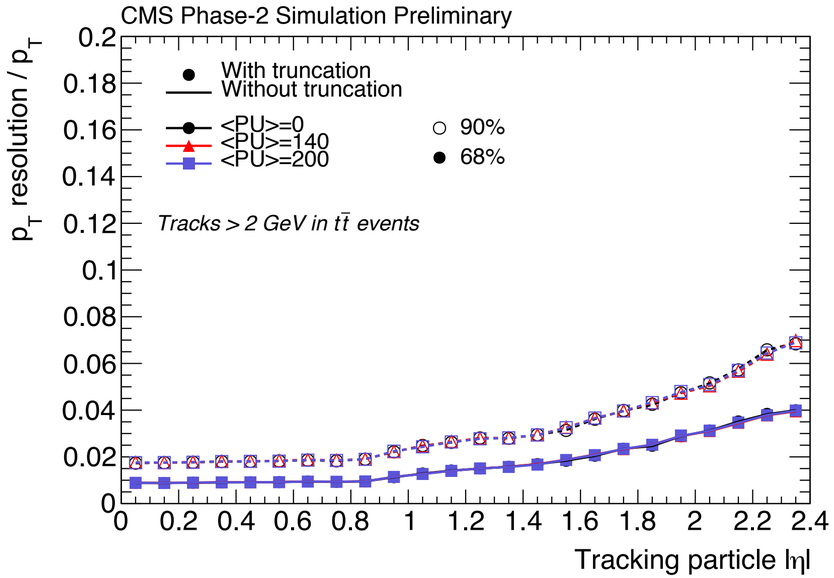
- Average track finding **efficiency** for **$t\bar{t}$** tracks > 95% *(> 3 GeV)*
- z_0 resolution ~ 1 mm *(barrel)*
- p_T resolution ~ 1% *(barrel)*
- Per event average ~70 tracks (3 GeV), ~200 (2 GeV) *($t\bar{t}$ at 200 PU)*



all tracks in $t\bar{t}$ events $p_T > 3$ GeV

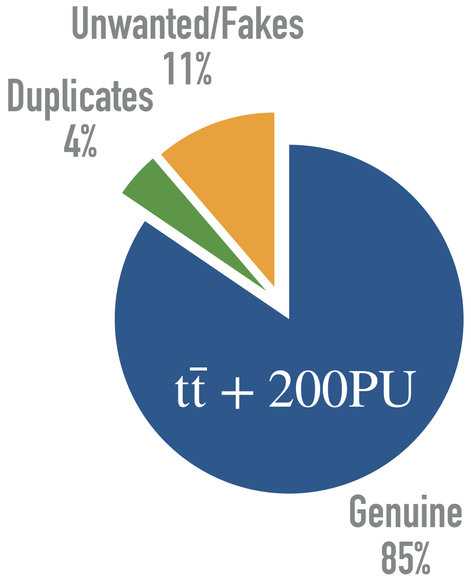




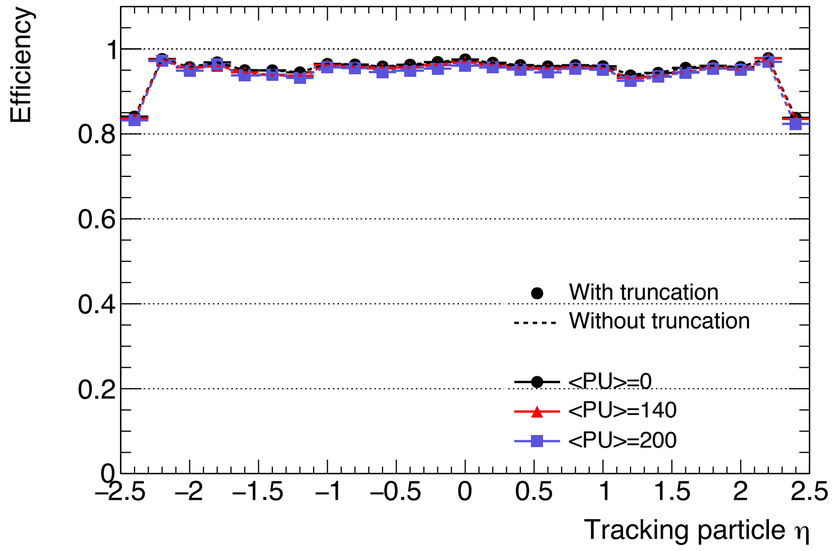


TRACK FINDING PERFORMANCE

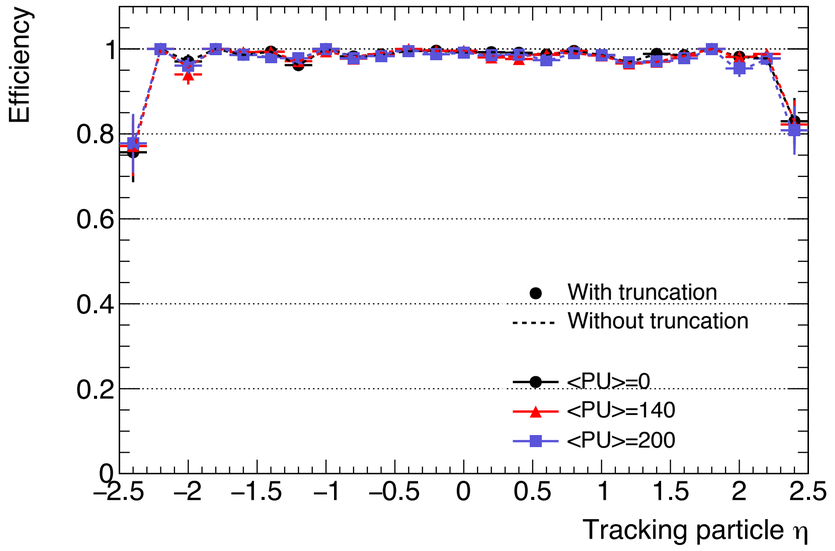
- Muon efficiency ~ 99%
- Electron efficiency ~90% above 10 GeV
- Fake rate ~10% can be reduced with BDT or tighter selection cuts
- Performs well up to 300 pileup



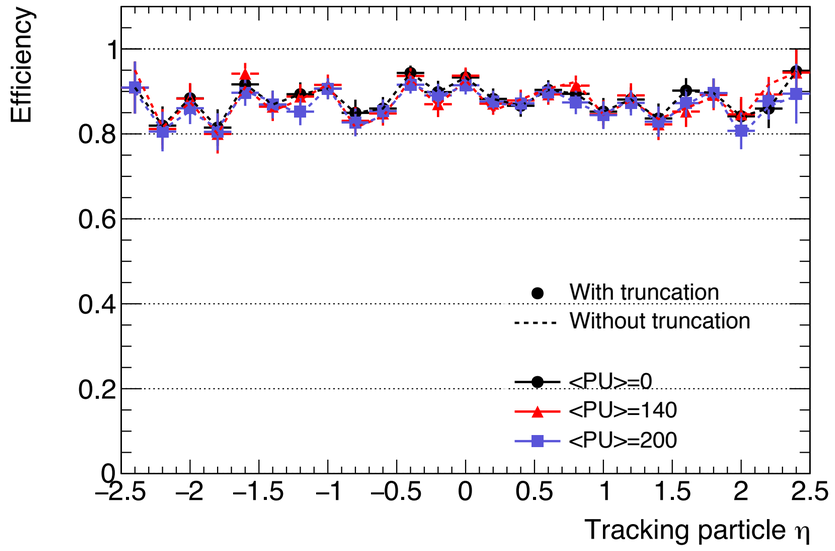
all tracks in $t\bar{t}$ events $p_T > 3$ GeV



$\mu^+\mu^-$ in $t\bar{t}$ events $p_T > 3$ GeV



e^+e^- in $t\bar{t}$ events $p_T > 8$ GeV

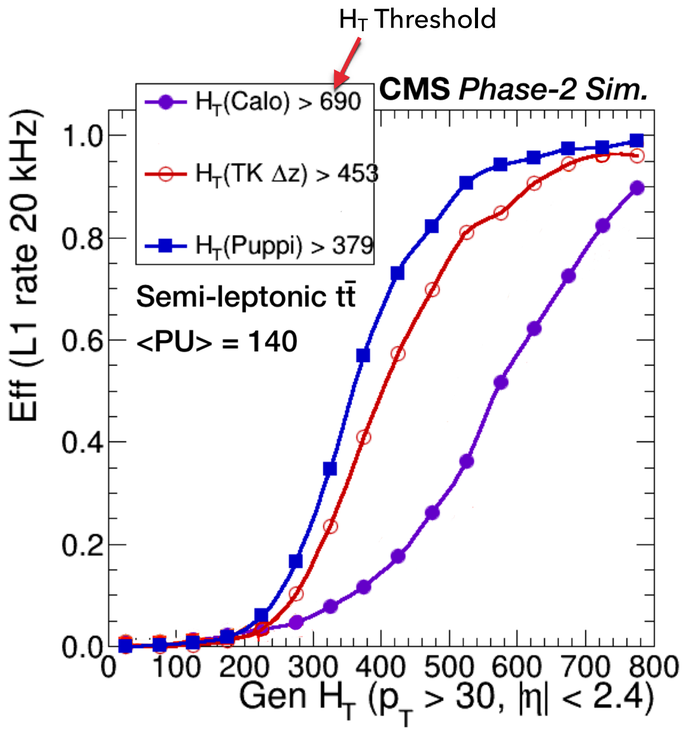


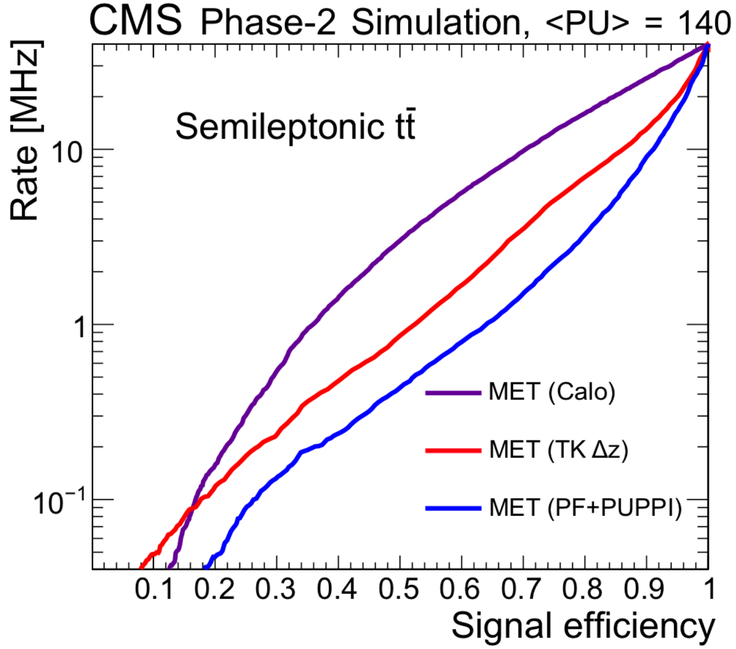
Interesting extension possibilities →

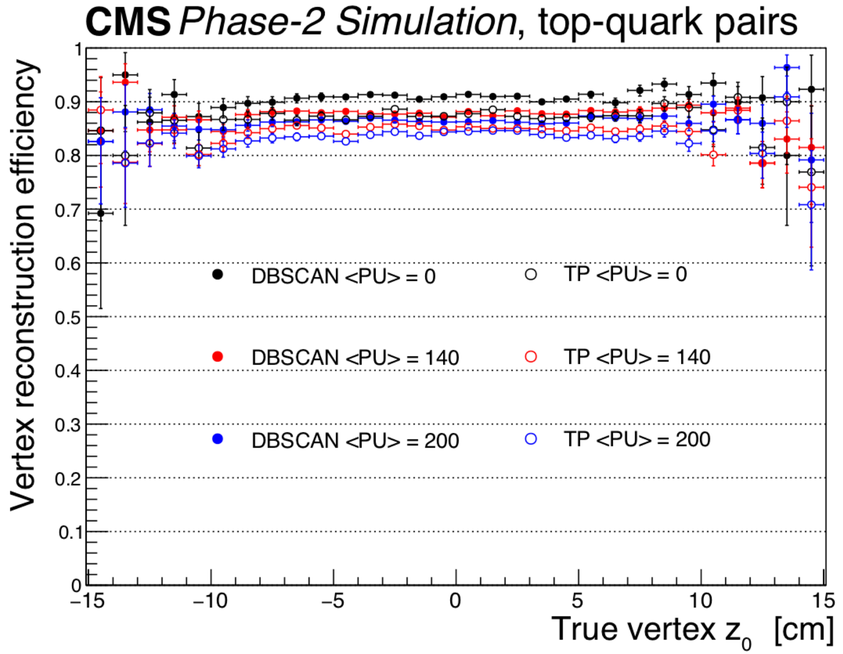
EMULATION RESULTS

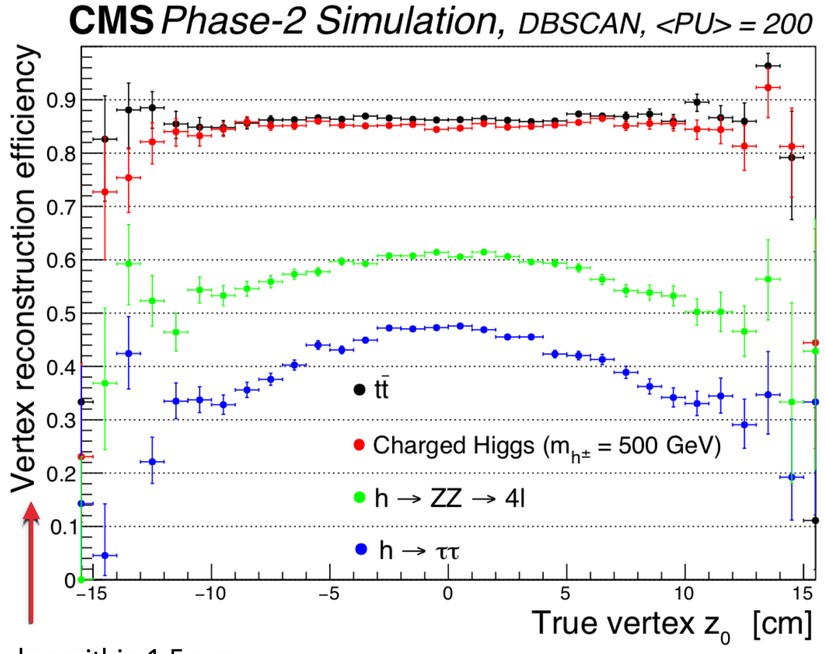
TRIGGER PERFORMANCE

- **Pileup rejection** greatly improved by **combining track and calo** information
- **Particle flow** approach feasible at L1, and gives significant performance gains
- **Vertex finding** performance is function of number and p_T of tracks
  - Very successful for channels with high energy jets, ~robust to high pileup
  - Variety of algorithms being studied







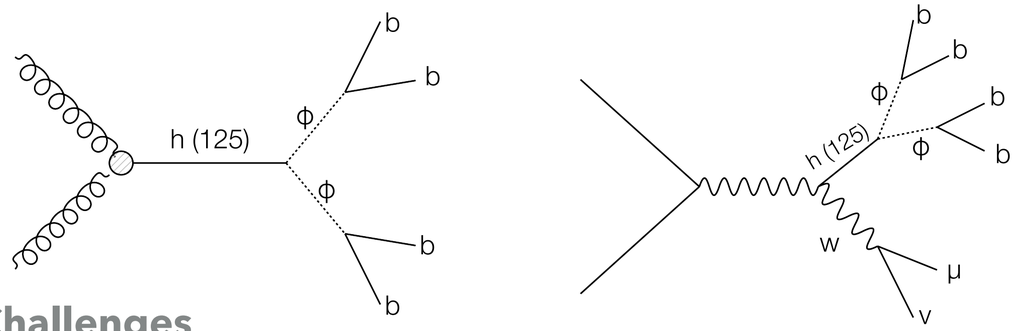


Defined as within 1.5 mm from MC truth

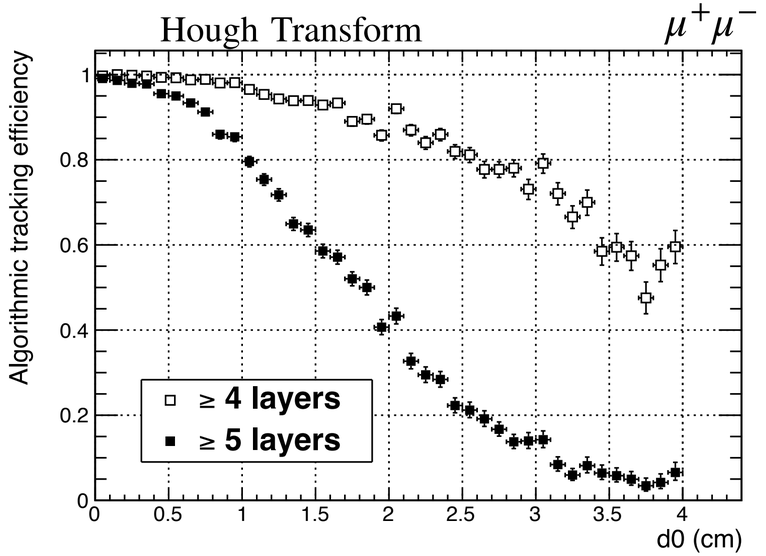
PROMISING EXTENSIONS TO L1 TRACK FINDING

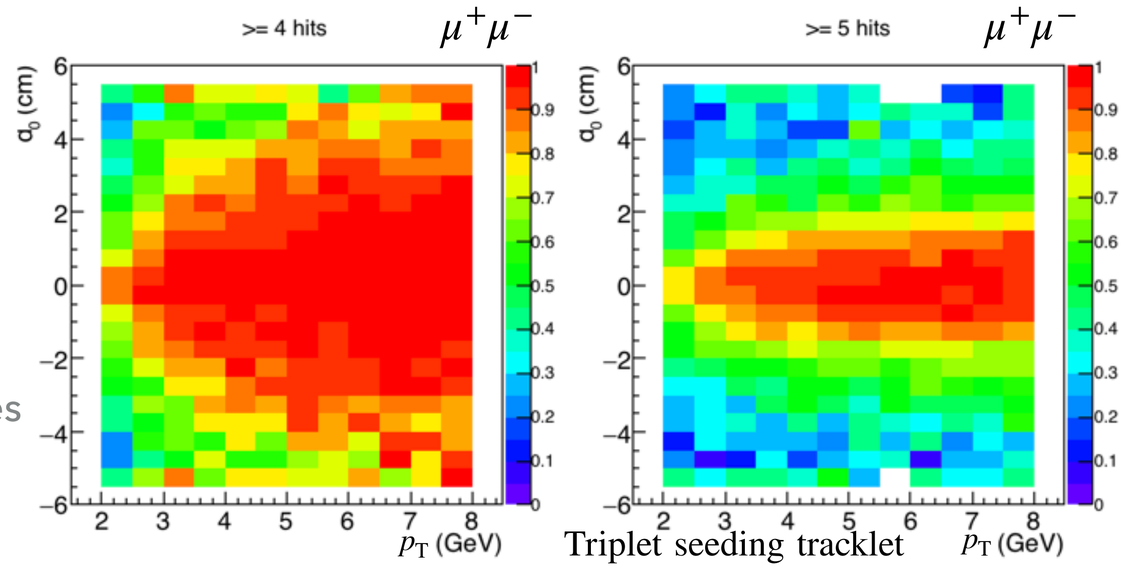
DISPLACED TRACKING

- Possible with both HT+KF and tracklet algorithms, up to ~5 cm
- **Motivation**
  - Lots of **interesting physics** with displaced tracks e.g rare Higgs decay to a long lived (dark matter) φ (~no background)
  - Alternative to **expensive dedicated experiments**



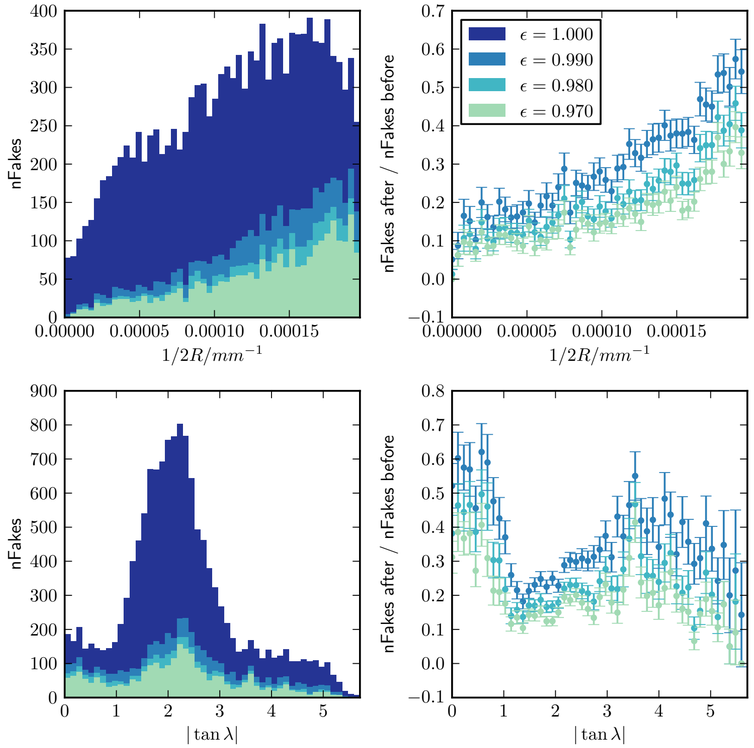
- **Challenges**
  - No beam point constraint -> higher (but manageable) fake rates
  - **Increased processing requirements** - truncation vs FPGA resources
- **Adaptations**
  - Size of HT cells must be increased
  - Tracklet must seed with stub triplets
  - Fitters do 5 param fit (d_0)

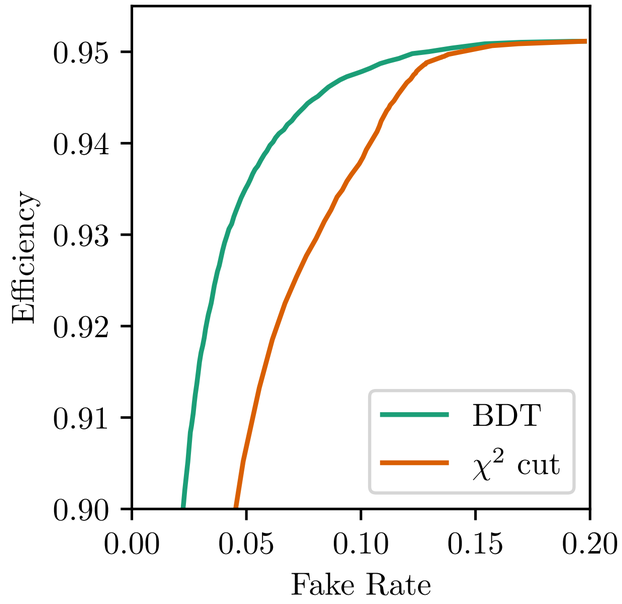




BDT FOR FAKE TRACKS

- **Gradient boosted decision tree**, implemented in FPGA logic, to select and remove fake tracks after the track fit
  - Make a static, fully pipelined implementation of a **pre-trained** BDT ensemble
  - Train ensemble on a CPU (using scikit-learn)
  - Export trained ensemble to JSON file
  - Read by firmware



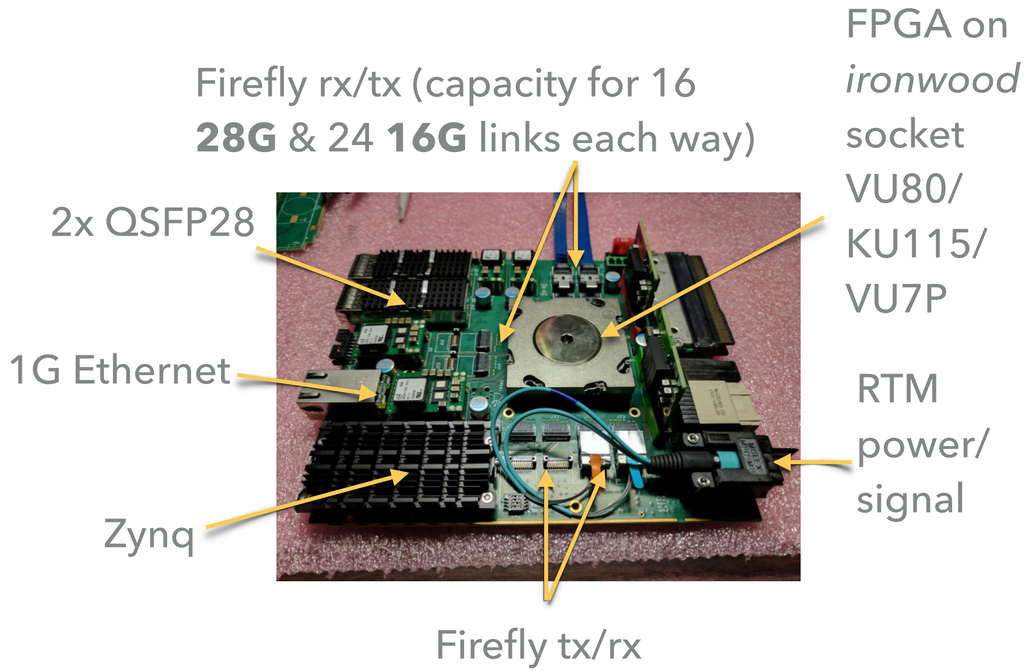


- 4 integer features
  - χ^2, $|1/p_T|$, $|\tan\lambda|$, num. skipped layers
- 100 trees, depth 3
- **Tuneable** on eff. vs fake rate curve
- Latency ~30 ns only!

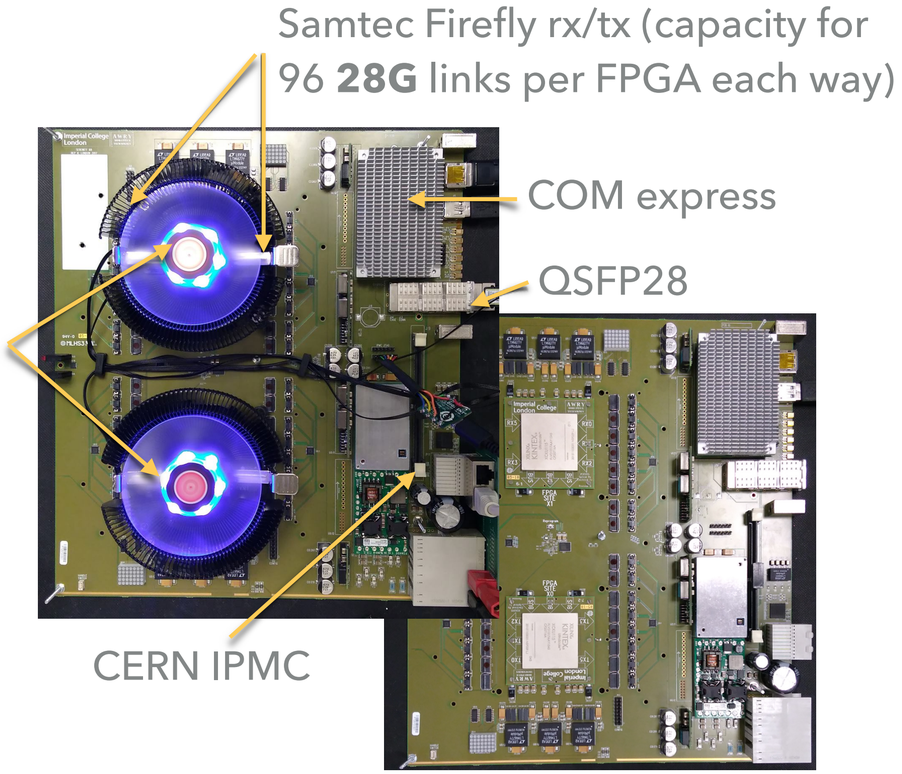
efficiency loss [%]	**1.0**	**0.5**	**0.1**
fake rate reduction [%]	70	50	35

HARDWARE R&D

- **YUGE (uTCA):**
  - VU080/KU115/VU7P FPGA variants
  - Zynq used for slow control
  - Evaluation of 16-25 Gb/s links



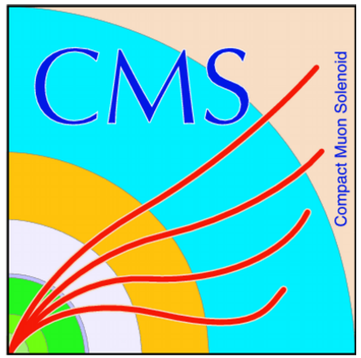
- **SERENITY (ATCA):**
  - Carrier card provides common board-level services e.g power, clock, monitoring, control
  - Daughter card on interposer hosts data-processing FPGA(s)
    - Cards for KU115, KU15P, VU9P available/in development
  - Control via an on-board PC, COM express
  - Generic and flexible fw & sw development



SUMMARY

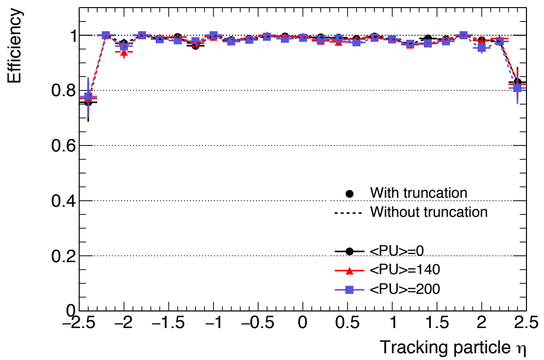
- CMS needs tracks at L1 for HL-LHC pileup conditions
- **Highly flexible** track-finder/pattern recognition algorithms demonstrated in hardware
- **Highly scalable,** time/physical segmentation could be as large/small as required based on data rates

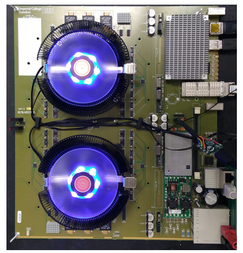
- **Proven** with **currently available hardware**, that a level-1 track-trigger based on **FPGA** processing boards is a **feasible** and **safe** solution
- Adapting to latest trends in the community: BDTs and displaced tracking
- Lots of flexibility with an all-FPGA solution
- Plenty of **time to improve and optimise** algorithms for global trigger requirements



Thanks for listening

I look forward to answering your questions





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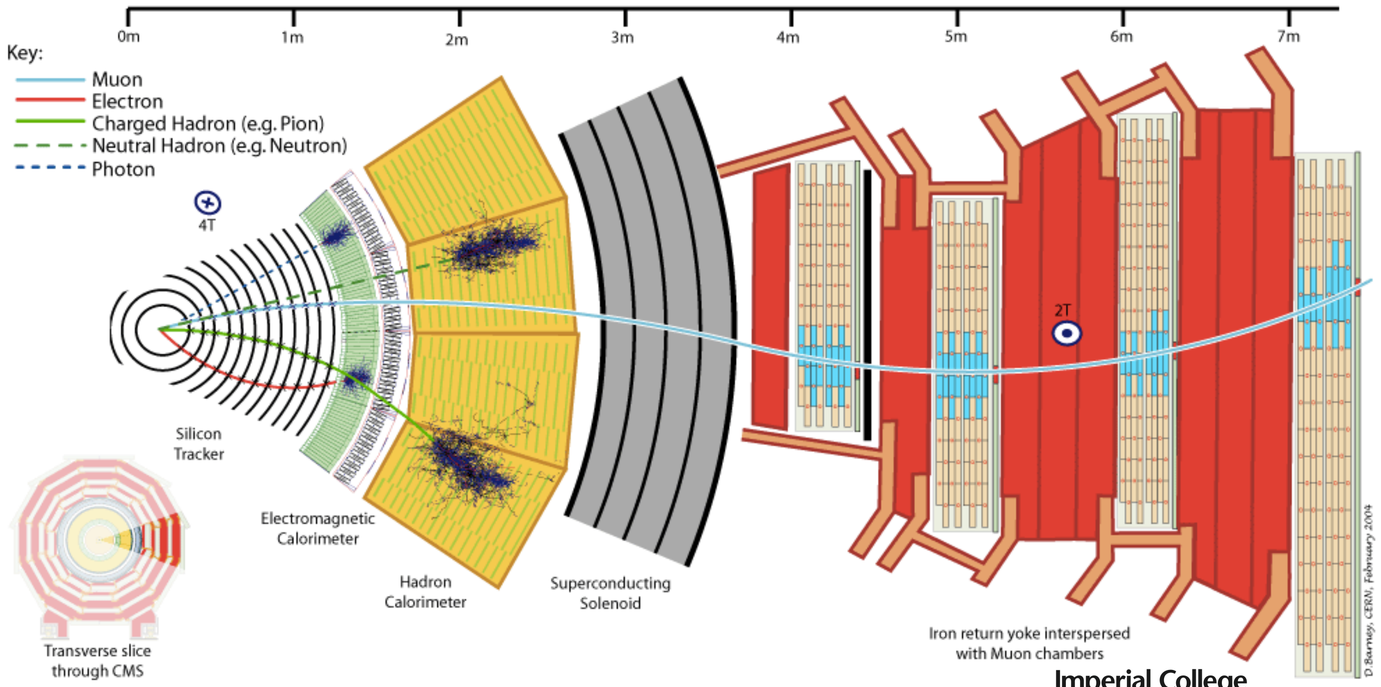
INTRODUCTION TO COMPACT MUON SOLENOID (CMS)

- **Large, all-purpose detector**, designed to investigate a **wide range of physics** (Higgs, Supersymmetry, Dark Matter). 20-40 **simultaneous collisions (pileup)** at 40 MHz

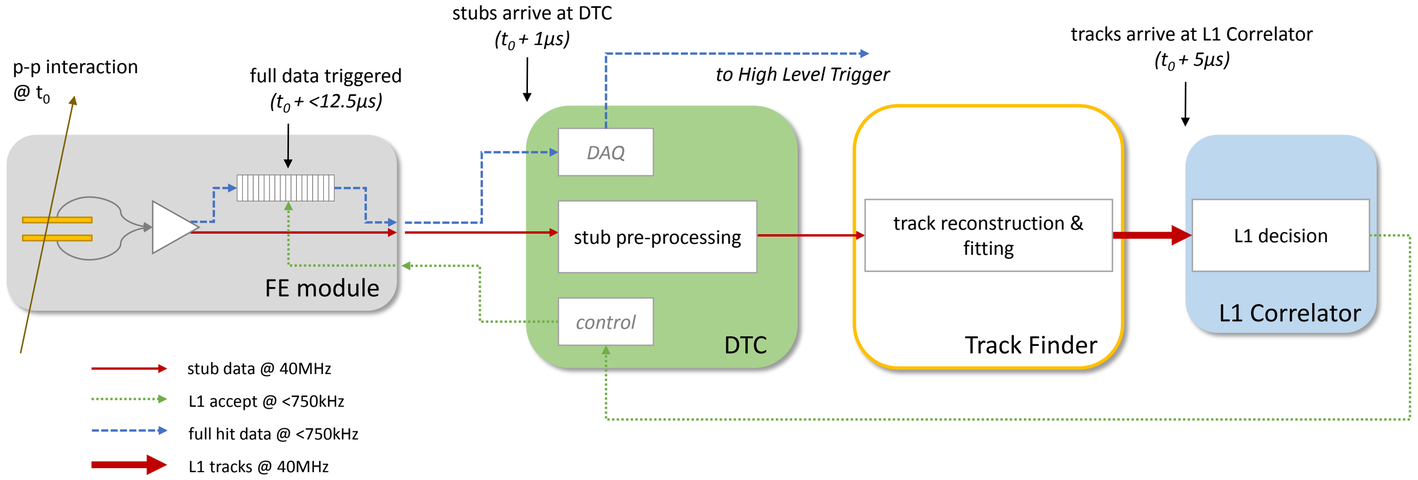
1. **Silicon strip tracker** (~1.2m radius, 200 m^2 area), largest silicon tracker in operation
2. Within **3.8 T** superconducting solenoid. **Transverse momentum (p_T)** measured with curvature in B-field
3. **Level-1 (L1) trigger**, latency O(3-4 μs), rejects uninteresting events, rate reduction O(x400)
4. Data size/rate from tracker **too large** to use in L1-trig



LEVEL-1 TRACK FINDING

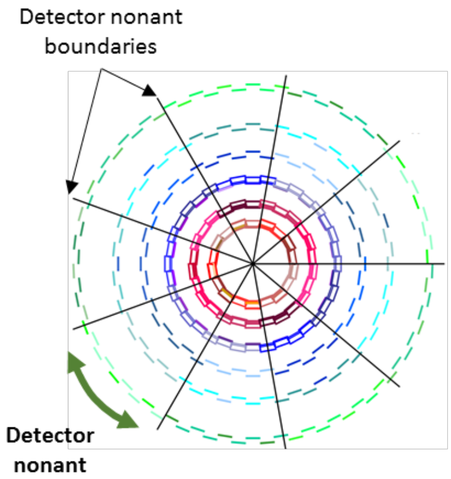
ARCHITECTURE

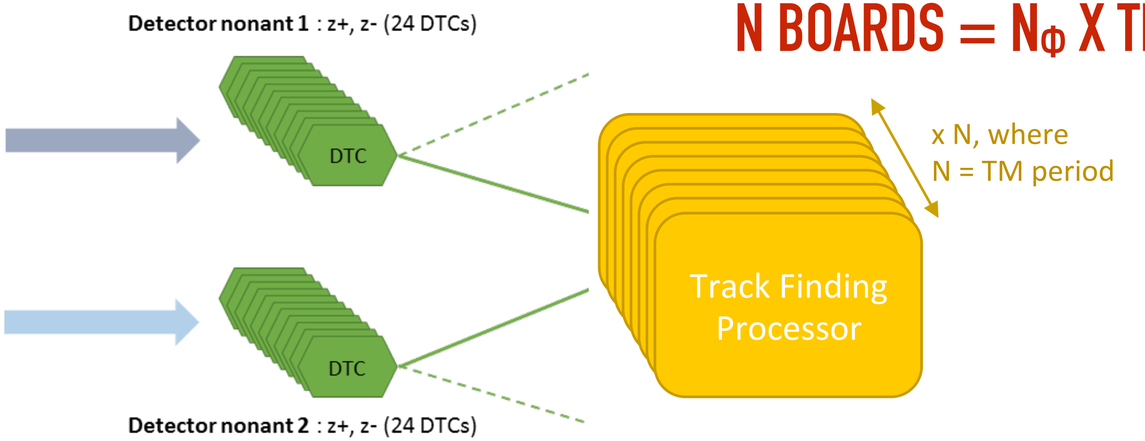
- ~4 μs available for track finding (~12.5 μs total @ L1)
- Proposal: Two layers of processing
- DAQ, Trigger and Control (DTC) layer
- Track Finding Processor (TFP) layer
  - Data-stream FPGA-based processing board
  - Processes up to $1/N_{\varphi}$ of tracker in φ and 1/(time multiplex period)



- TFP receive data links from adjacent detector regions in φ
- Processing of subsequent events done on parallel independent nodes

Choice of physical/time segmentation dictated by data rates out of the detector and into FPGA (possible options are 9x18, 18x6 …)





N BOARDS = N_{Φ} X TMP

- Time-multiplexed system
- Each TFP operates independently
- One TFP demonstrates full functionality