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Level-1 track finding with an all-FPGA system at CMS for the HL-LHC

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The CMS experiment at the LHC is designed to study a wide range of high energy physics phenomena. It employs a large all-silicon tracker within a 3.8 T magnetic solenoid, which allows precise measurements of transverse momentum (pT) and vertex position.

This tracking detector will be upgraded to coincide with the installation of the High-Luminosity LHC, which will provide up to about 10^35 cm^2 /s to CMS, or 200 collisions per 25 ns bunch crossing. This new tracker must maintain the nominal physics performance in this more challenging environment. Novel tracking modules that utilise closely spaced silicon sensors to discriminate on track pT have been developed that would allow the readout of only hits compatible with pT > 2-3 GeV tracks to off-detector trigger electronics. This would allow the use of tracking information at the Level-1 trigger of the experiment, a requirement to keep the Level-1 triggering rate below the 750 kHz target, while maintaining physics sensitivity.

This talk presents a concept for an all FPGA based track finder using a time-multiplexed architecture. Hardware demonstrators have been assembled to prove the feasibility and capability of such a system. The performance for a variety of physics scenarios will be presented, as well as the proposed scaling of the demonstrators to the final system and new technologies.

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