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A pixel detector readout circuit with digital charge sharing compensation hit allocation algorithm

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This paper presents a design of a pixel readout circuit implementing an charge sharing compensation method based on an algorithm for asynchronous approximation of a center of gravity –Cogito [1]. In contrary to the former published methods, developed by Medipix Colaboration [2] and C8P1 algorithm by AGH-Fermilab [3], which rely on analog properties of the observed signals, the presented solution bases only on the shape of the area of an array which has detected the fractional charge. The hit allocation process is carried out entirely in the digital domain, while the analog front-end is responsible only for signal summation and amplitude discrimination.
The digital part, responsible solely for the algorithm operation, has been experimentally verified [1]. The measurement results showed that the hit allocation process can be completed in time on the order of tens of nanoseconds. This work presents the design of a pixel readout circuit implementing the Cogito algorithm, complemented by the analog front-end block. The input charge sensitive and shaping amplifier's cores are based on a modified inverter circuit. The feedback circuits of both amplifiers have been optimized for linearity, which is required to correctly reconstruct a full charge of a charge-shared event. The design is implemented in 40 nm CMOS process. Its details, backed-up by comprehensive simulation results will be presented during the conference.

Fig. 1. Schematic of a hybrid pixel detector with the COGITO algorithm [1].

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[1] P. Otfinowski et al., "Asynchronous Approximation of a Center of Gravity for Pixel Detectors' Readout Circuits,"IEEE Journal of Solid State Circuits, in print.
[2] R. Ballabriga, et al., "The Medipix3RX: a high resolution, zero dead-time pixel detector readout chip allowing spectroscopic imaging", 2013 JINST, 8, C022016, pp 1-15.
[3] G. W. Deptuch, et al. "An Algorithm of an X-ray Hit Allocation to a Single Pixel in a Cluster and Its Test-Circuit Implementation,"IEEE Trans. Circuits Sys. I, Reg. Papers, vol. 65, no. 1, 2018, pp. 185-197.

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