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A Comparative Study of the TID and SEE Radiation Effects on ASICs Manufactured in 180 nm Commercial Technologies

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Radiation damage is a widely studied topic for its effects on semiconductor sensors and front-end electronics used in medical and aerospace applications. Radiation tolerance and stability of the detector properties are critical issues for many applications.

Presented study compares the effects of radiation on circuit structures manufactured in a standard 180 nm CMOS [1] and, in addition, on a 180 nm SOI [2] technology. These ASICs are ongoing R&D in the field of radiation detectors and apart from transistor testing matrices for TID measurements, they contain analog and digital circuits with different transistor sizes useful for SEE measurements.

The TID study was performed using a high flux Co-60 source in charged particle equilibrium conditions, where test structures on ASICs were irradiated up to a total absorbed dose of 100 Mrad.

The test structures in both technologies consist of transistors of different width to length ratios, polarities and placement in deep insulation wells, as shown in Figure 1. The irradiation was performed in several steps and, after each step, the IV characteristics of the transistors in test structures have been measured. After irradiation, test structures were left to anneal at room temperature and their parameters have been monitored periodically. The measurement results are expressed in the form of transistor IV characteristics, threshold voltage shifts and a relative leakage current increase. In addition, the integral power consumption of the whole analog and digital part was measured and compared to the transistor level measurements.

Concerning the SEE measurements, the digital registers of the ASICs were used to study the bit flip cross sections, measured for different LET values by beams of protons, He-4 and C-12 ions at several energies delivered by a combination of cyclotron and tandem accelerators.

References

- [1] Z. Janoska et al., The PH32 Readout Integrated Circuit, in Proceedings of the 10th International Conference on Measurement, Bratislava: VEDA, 2015, pp. 207-212. ISBN 978-80-969672-9-2
- [2] M. Havranek et al., 2017 MAPS sensor for radiation imaging designed in 180 nm SOI CMOS technology, proceeding from IWORID 2017, submitted to JINST

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