Fast Readout Logic Interfacing a 256-PixelMatrix of a Dual-Layer 3D Device

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Outline

- Chartered-Tezzaron consortium

- Italian VIPIX project

- The TOP layer of a 3D ASIC design

See also talks by F. Giorgi and V. Re

Consortium

- To join
  - NDA with Tezzaron
  - LOI to Fermilab asking to participate in MPW run
  - Only cost is for MPW space
- Members receive from Tezzaron
  - Cadence PDK for Chartered 0.13 um
  - Calibre DRC/LVS/PEX(XRC) deck for Chartered 0.13 um CMOS with correct process options
  - Calibre DRC deck for Tezzaron 3D design rules
    - Cu-cu bond interface
    - Via formation
  - Information for fabrication of 2D and 3D I/O pads
  - ARM Artisan library (separate NDA)
    - Full-layout views
  - Also available but not used (separate cost for each)
    - MicroMagic 3DMax (alternative to Virtuoso)
    - Magma (working on 3D LVS)

Italians
  - University at Bergamo
  - University at Pavia
  - University at Perugia
  - **INFN Bologna**
  - INFN at Pisa
  - INFN at Rome

Problems with the digital Design-KIT from ARM

Subreticules E & F
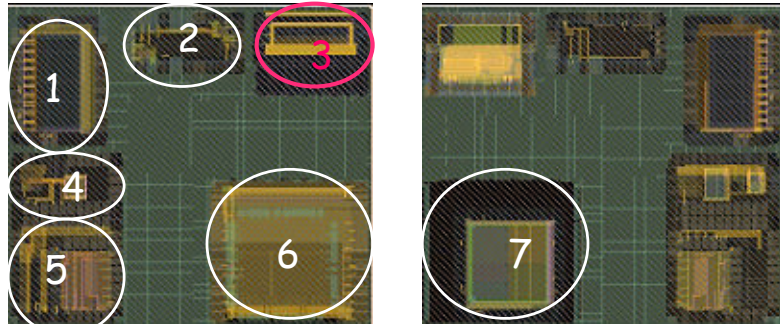
- **Subreticule E** – 7 sub-circuit areas
  - 1) 3D MAPS with 32 x 64 array of 25 um pixels with DCS, 3T FE, discriminator, auto-zeroing. All control logic in digital tier. (Roma)
  - 2) 3D MAPS test structures - Two 3 x 3 40um pitch arrays. One with shaperless preamplifiers. Other is designed with ELT input devices. (Pavia/Bergamo/Pisa)
  - 3) 3D MAPS test structure with 8 x 32 array of 40 um pixels, DNW sensors, data push architecture (Pavia/Bergamo/Pisa/Bologna)

  - 4) Two test structures for the subreticule F DNW MAPS device (Pavia/Bergamo)
    - 16 x 16 array of 20 um pixels with inter-train sparsified readout
    - 8 x 8 array of 20 um pixels with selectable analog readout of each pixel
  - 5) Two 3D test structures
    - 3 x 3 array of 20 um pixels and 4 single channels for DNW MAPS (Pavia/Bergamo)
    - 3D RAPS structures including single ended I/O buffer, two single addressable 3T pixels with small and large area detecting diodes.
      - 5x 5 and 16 x 16 pixel matrices, each one featuring small and large detecting diodes (Perugia)
  - 6) **2D** version of 3D MAPS device in subreticule F, 64 x64 array of 28 um pixels (Pavia/Bergamo)
  - 7) **2D** sub-matrices with 10 and 20 um pixels to test signal to noise performance of MAPS in the Chartered process (Roma)

V.Re N02-3 and G. W. Deptuch N27-1 @ NSS 2009 Orlando

By R. Yarema @ TWEPP 09 Paris

Italian VIPIX project
(**INFN** collaboration: BO, PI, PV, BG, MI, TN, TS, PG, RM-III)

Aim

Improve the state-of-the-art of slim tracking system construction for high-energy physics applications

Applications

Low material budget silicon tracking systems (detector/mechanics/cooling) relevant for the future experiments (SuperB) to reduce multiple scattering

Good candidate technology for the innermost layers of the vertex detectors

Bologna involved in the design of a

2-layer project for a matrix of 256 pixels with fast readout capabilities:
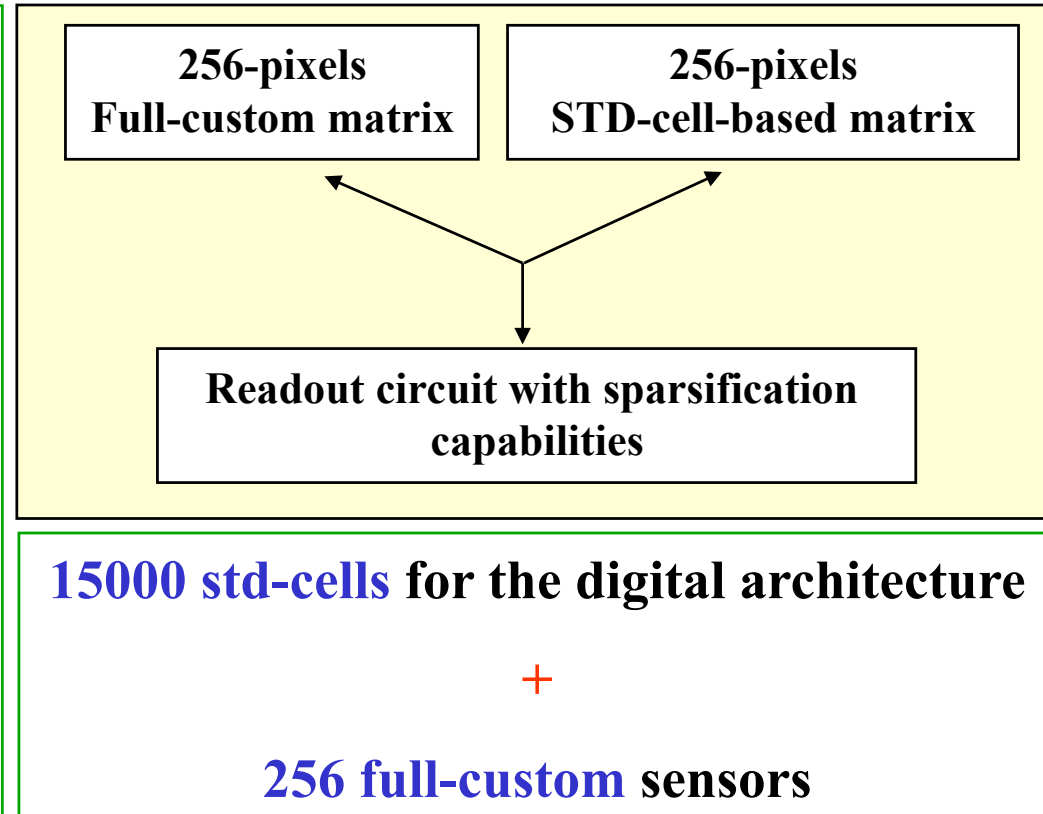- BOTTOM   for the sensors and the first stage of signal processing
- TOP   for the readout logic of the entire matrix

ASIC designed and submitted
The Matrix Readout

Main Features

- Pixels grouped and addressed as MacroPixels, which are a 4 x 4 groups of pixels
- **2 matrixes of 256 pixels** each
  - **1** made of sensors $40\times40\mu m^2$ from the top layer,
  - **1** based on digital std-cells,
  - to be used one at a time,
- **Slow-Control** for configuration,
- on-line data sparsification,
- **1 readout clocks** @ 100 MHz,
- 1 slow-control clock,
- **Stand_By** in case of over-hit-rate

256-pixels Full-custom matrix	256-pixels STD-cell-based matrix

Readout circuit with sparsification capabilities

15000 std-cells for the digital architecture

+

256 full-custom sensors

Concept of Macro-Pixel; 4x4 pixel cluster

ASIC designed and submitted
The Matrix Readout

The 256-pixel matrix is arranged in:

- **32** columns × **8** rows,

- **8** MacroColumns (MC) × **2** MacroRows (MR),

- **16** MacroPixels composed of **8 × 2** pixels

The pixels, the MCs, the MRs and the MPs are numbered to define the **17-bit** formatted output data

The hits are on-line associated with a **8-bit Time-Stamp**
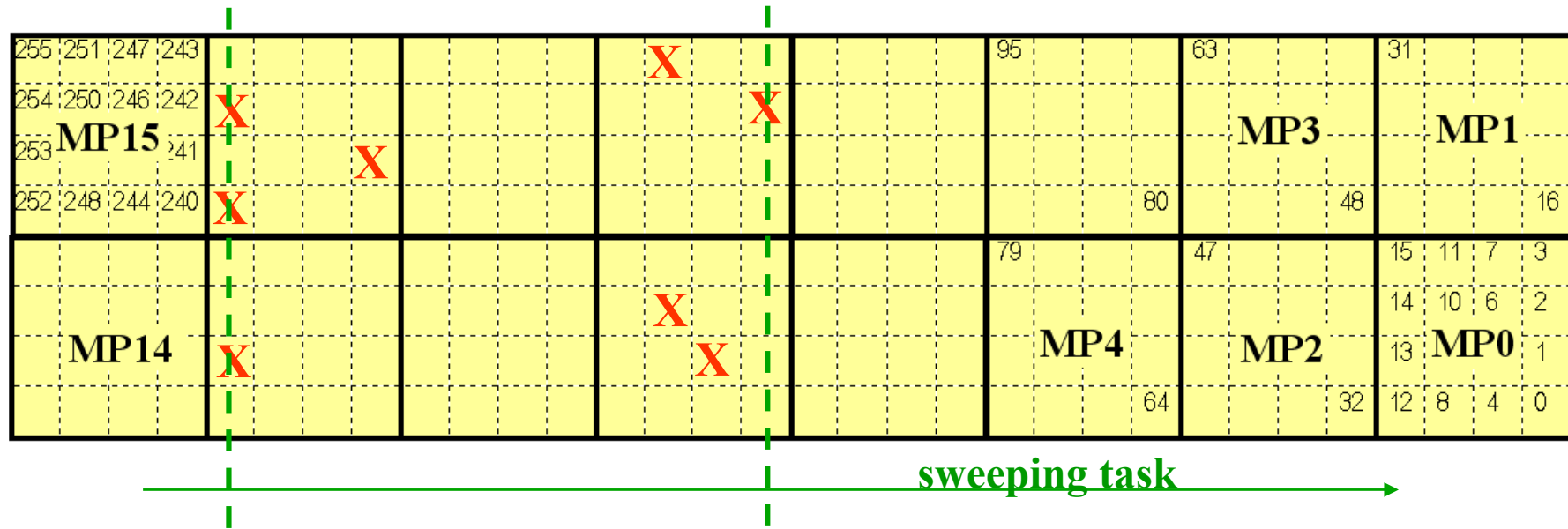
Pixel-Column inside a MC/MP

Macro-Column address

ASIC designed and submitted
The Matrix Readout

At each clock cycle, a full column (1-to-8 hits) is readout in parallel….

… then each hit is associated with its Time-Stamp and the information …

… is sent to a FIFO-like BARREL output to queue the dataflow

**Each MC readout requires 4 cycles + 1 to reset the MPs. Empty MCs are skipped**

Example above requires 10 (2 MC × 5) cycles to readout 8 hits. Then the 8 hit words are packed into the BARREL and sent to ASIC's output in 8 clock cycles

ASICs designed and submitted
## Queued output dataflow

The output BARREL:

- is circular and **16-word deep**,

- has **24-bit words** (now redundant) ,

- **never shifts** data (low power),

- uses pointers to identify the state,

- **reads 1 to 8 words** at a time,

- **writes 1 word at a time** to the ouput port,

- **empties** its words if in **Stand_By** status

15   0

24-bits

1

2

READ Pointer

WRITE Pointer
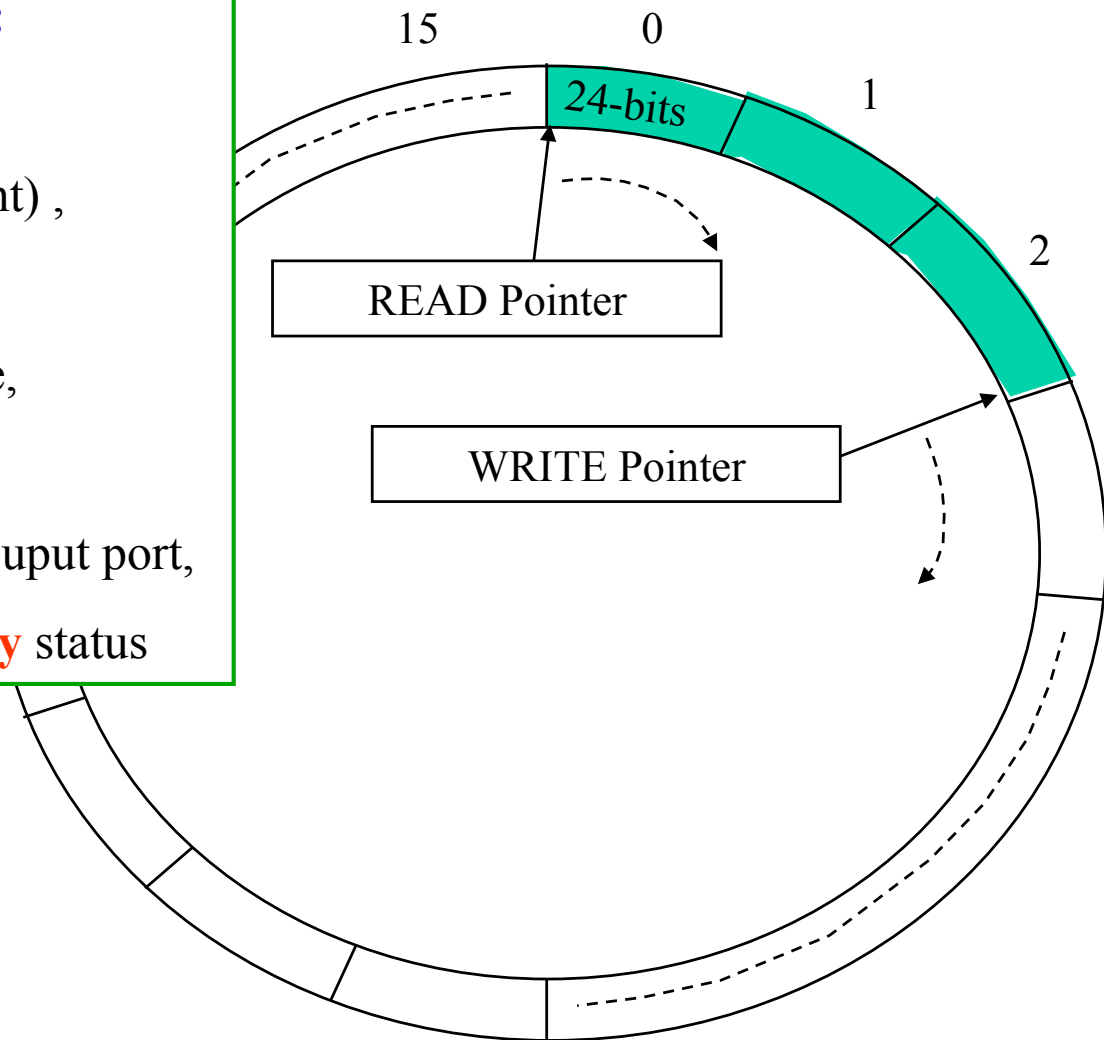
ASIC designed and submitted
The Matrix Readout

Pixel-Column inside a MC/MP
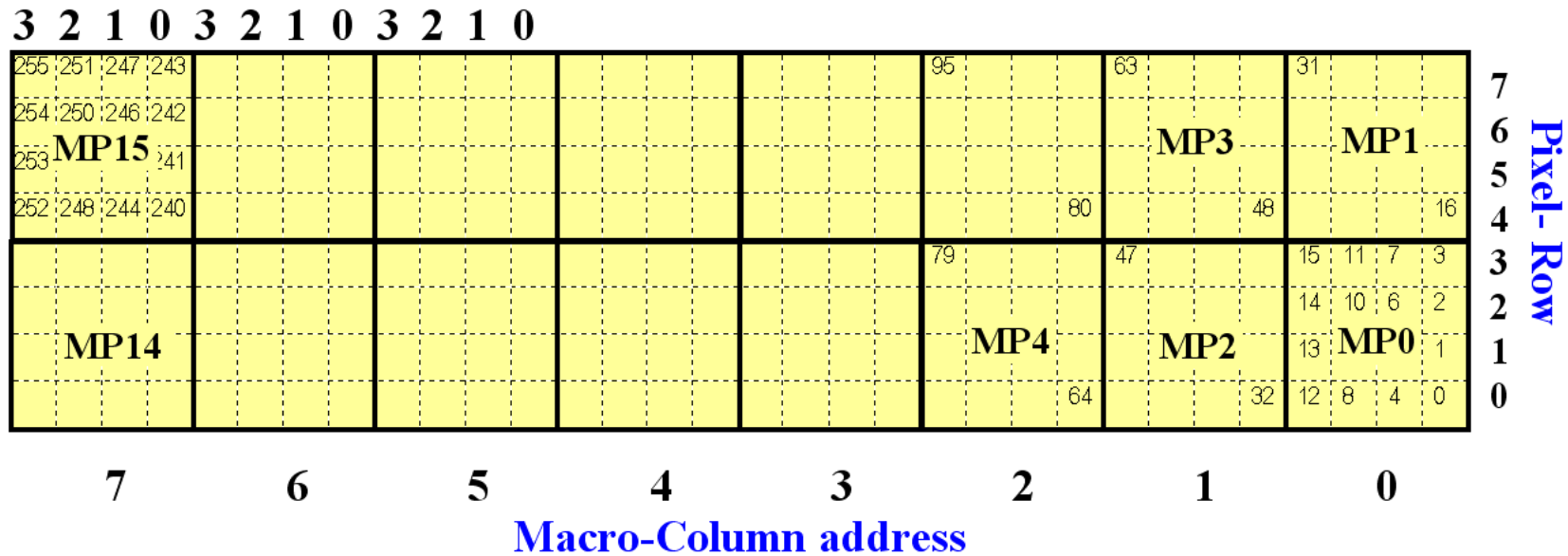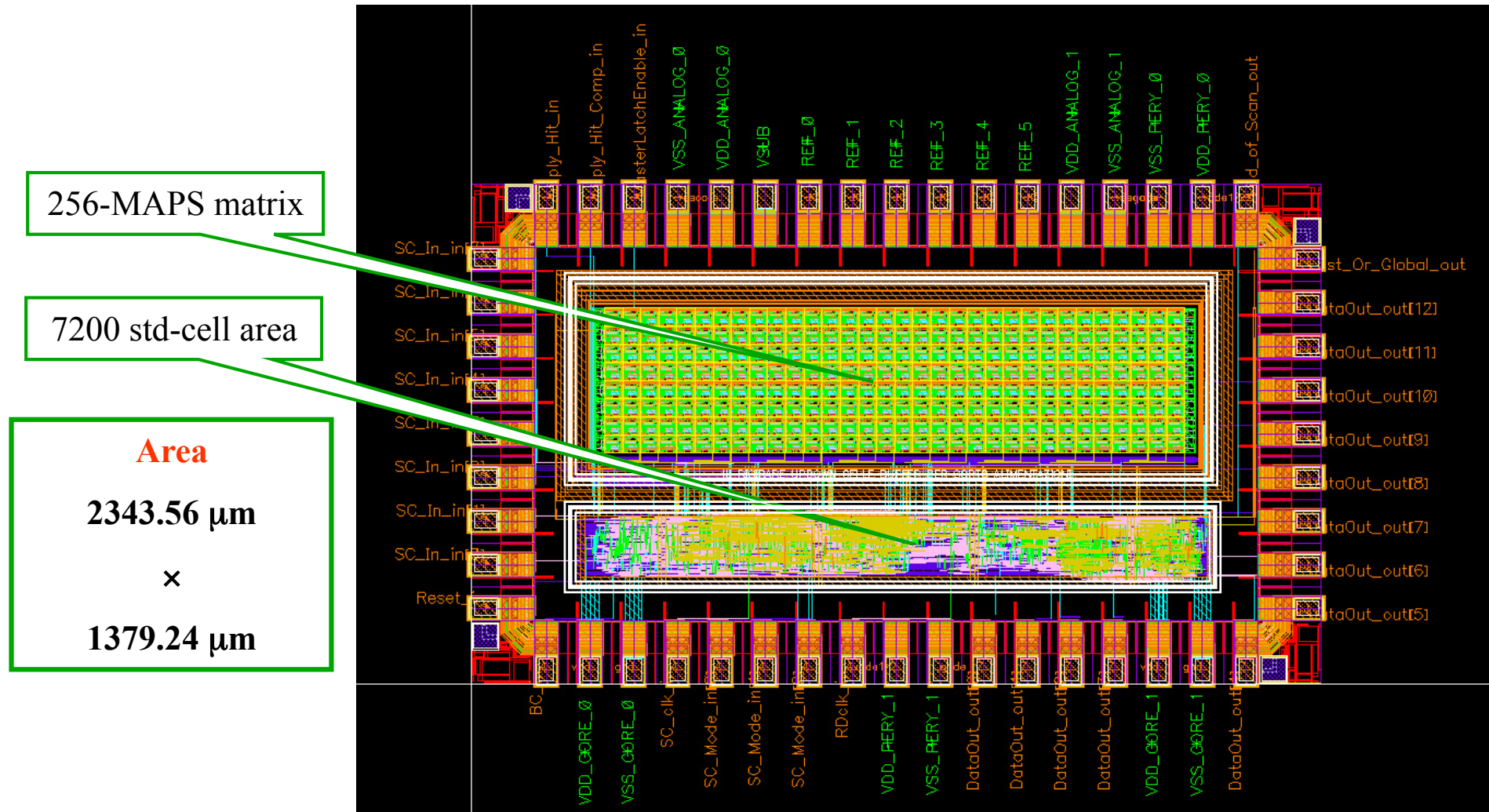

FORMATTED OUTPUT (1+3+2+3+8 = 17 bits)
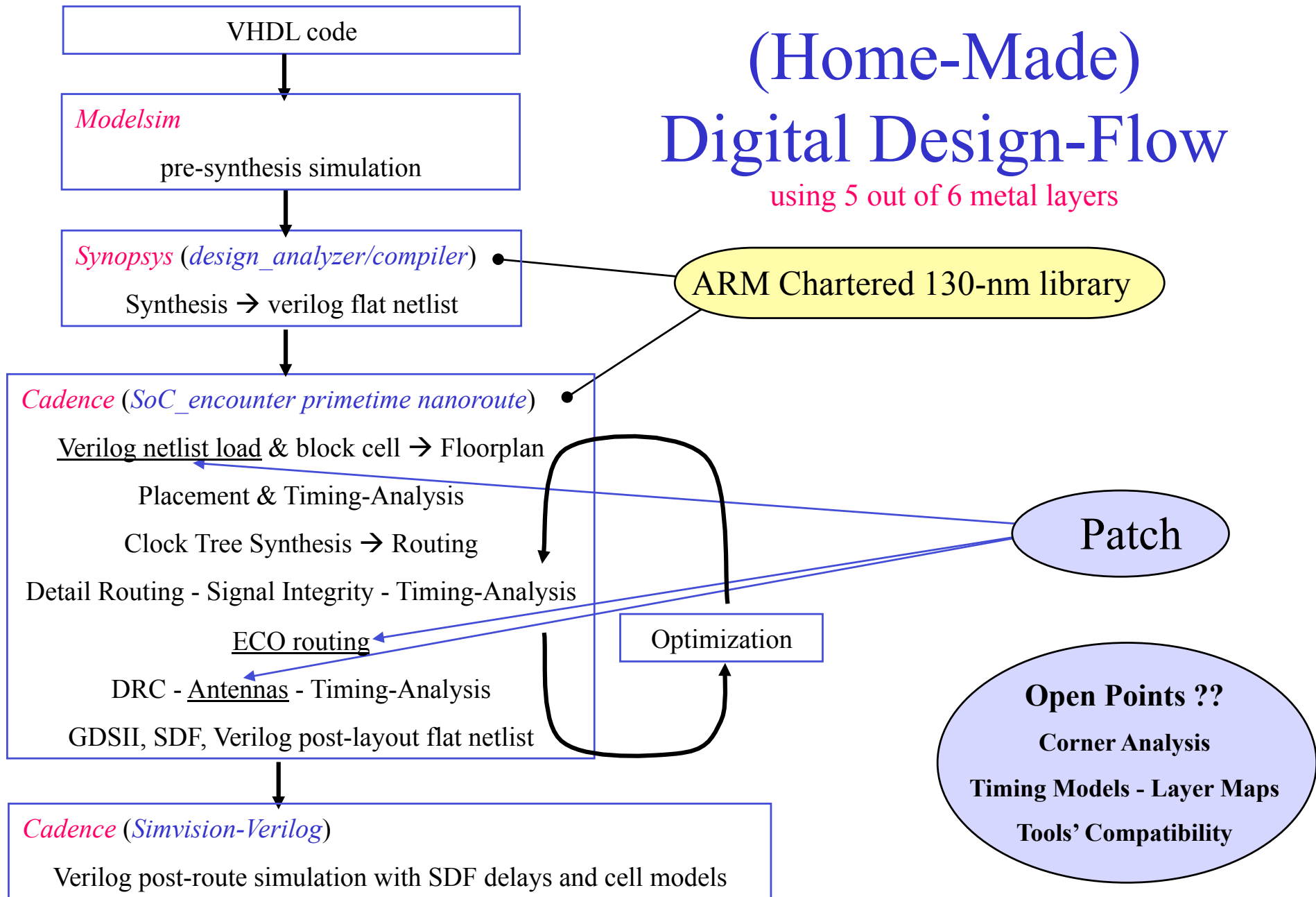<Data Valid><Pixel Row><Pixel Column within MP><MC Address><Time Stamp>

ASIC submitted on 2007 via CMOS ST130nm
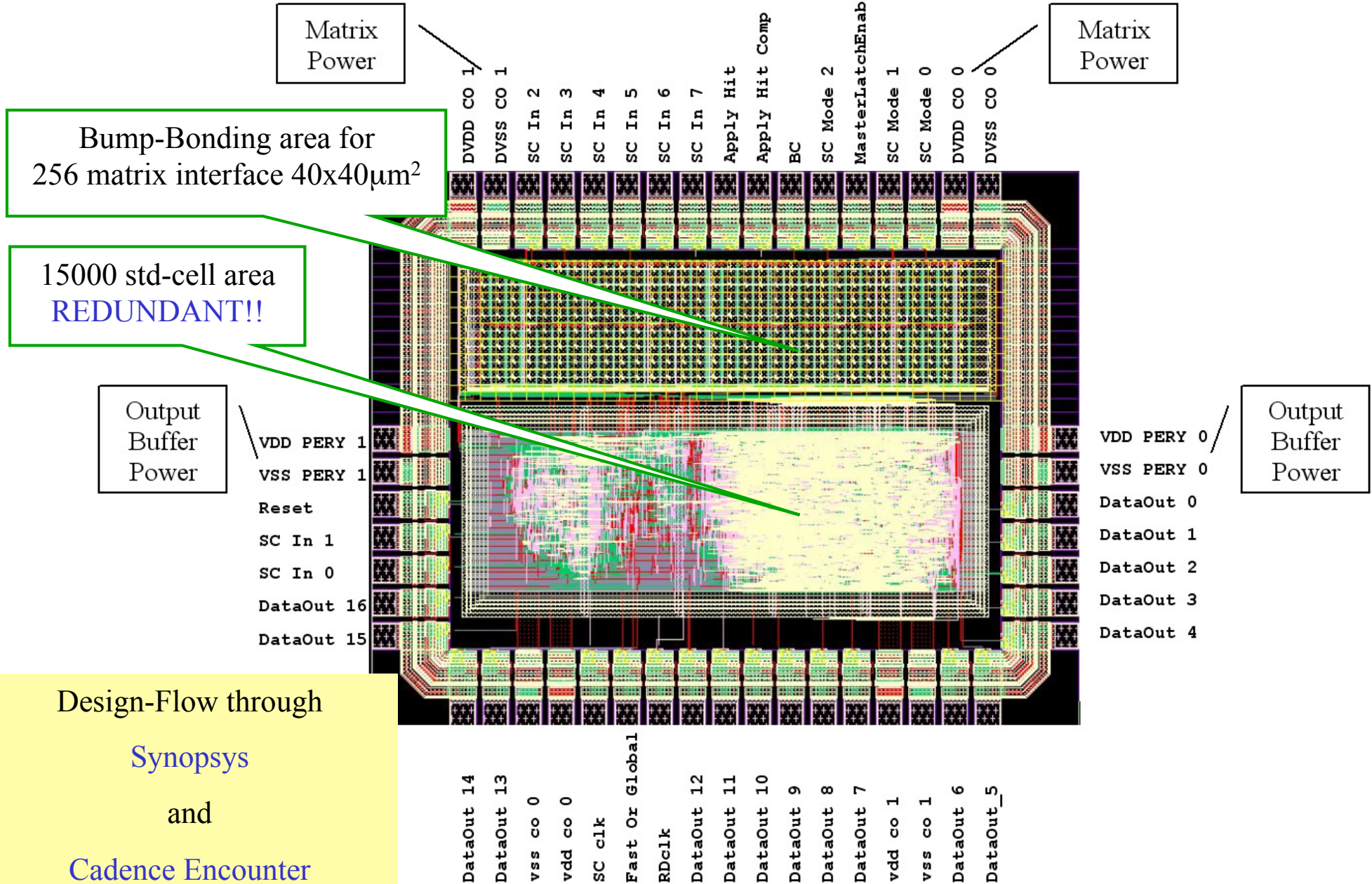## Digital Design-Flow has primarily be re-used

256-MAPS matrix

7200 std-cell area

Area

2343.56 μm

×

1379.24 μm

(Home-Made) Digital Design-Flow

using 5 out of 6 metal layers

VHDL code

Modelsim

pre-synthesis simulation

Synopsys (*design_analyzer/compiler*)

Synthesis → verilog flat netlist

ARM Chartered 130-nm library

Cadence (*SoC_encounter primetime nanoroute*)

Verilog netlist load & block cell → Floorplan

Placement & Timing-Analysis

Clock Tree Synthesis → Routing

Detail Routing - Signal Integrity - Timing-Analysis

ECO routing

DRC - Antennas - Timing-Analysis

GDSII, SDF, Verilog post-layout flat netlist

Optimization

Patch

Cadence (*Simvision-Verilog*)

Verilog post-route simulation with SDF delays and cell models

Open Points ??

Corner Analysis

Timing Models - Layer Maps

Tools' Compatibility

ASIC designed and submitted TOP Layer

Matrix Power

Matrix Power

Bump-Bonding area for 256 matrix interface 40x40μm^2

15000 std-cell area REDUNDANT!!

Output Buffer Power

Output Buffer Power

Design-Flow through

Synopsys

and

Cadence Encounter

CONCLUSIONS

The work is aimed at testing the Tezzaron-Chartered facility and at

- fabricating a first "large-size" prototype,

- sparsifying on-line the hits,

- matching the requirements of future HEP experiments.

GOOD practice with the Consortium and see what happens….