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FF-LYNX: protocol and interfaces for the control and readout of future silicon detectors

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Future High Energy Physics experiments will have similar requirements with respect to latency, bandwidth, robustness against transmission errors and component failures, radiation hardness and power dissipation of hardware components. The FF-LYNX project started from the assumption that a general purpose flexible protocol implemented in IP cores available to future ASIC designers can fit these requirements. It can also address new requirements related to the low and fixed latency transmission of data to be used in embedded or remote trigger processors, providing a "standard"solution with obvious advantages in terms of development and production costs and homogeneity among the different experiments. The project is a collaboration among INFN-Pisa, University of Pisa, Department of Information Technology, and UCSB, Department of Physics. The project targets are:

-) development of an Integrated Simulation Environment (ISE) for the validation and characterization of protocols and interfaces;

-) definition of a protocol for the data acquisition and the distribution of the TTC signals;

-) implementation of the protocol in radiation tolerant and low power interfaces designed and developed in standard CMOS technologies (130nm, 90nm) and available to the designers of the integrated circuits for the future experiments.

We started from a detailed analysis of the requirements in the scenario of the LHC upgrades in collaboration with several groups involved in the design of future pixel and strip detectors and Front-End electronics. High level (System-C) models of the links have been developed to validate and characterize different protocols and interface implementations. Error injection in physical links and interfaces due to noise or radiation has been simulated and figures of merit (e.g.: Trigger Loss Rate, Frame Loss Rate) have been evaluated in different operating conditions. These models are the first building blocks of the ISE: sensors, Front-End ASICs, electrical and optical links DAQ and control systems and, possibly, embedded or remote trigger processors will be modelled and simulated together. The ISE will provide a powerful tool to evaluate the impact of any choice in terms of protocols, algorithms, architecture or technology on the overall detector performance.
The first version of the FF-LYNX protocol was released in July 2009 and will be described in detail. Key features are the integrated distribution of TTC signals and DAQ, the robustness of triggers and frame headers against transmission errors and the general structure of data frames, transparent with respect to different data types. Interfaces can be easily coupled to the core of the host circuits. They are compatible with different architectures of the control and readout systems and with different link technologies and speeds. Two channels multiplexed in the time domain are used for triggers and frame headers (THS channel) and data frames (FRM channel) supporting different data types. Different speed options (4xF, 8xF, 16xF; F = frequency of the reference clock) are foreseen. VHDL models of transmitter and receiver interfaces implementing the FF-LYNX protocol have been developed, simulated and synthesized in one high performance FPGA (Altera Stratix III). The design of a test circuit with interface prototypes in a commercial 130nm CMOS technology will start in March 2010 and a submission is scheduled for spring 2010.
A second version of the protocol supporting the transmission of data frames with low and fixed latency has been defined, it is currently under validation in the ISE and it should be released in January 2010. Simulation results will be presented on latency and efficiency in the "trigger"data transmission in different scenarios

w.r.t. occupancy and link speed and possible architectures to readout “trigger”and “raw”Silicon data in future Trackers will be proposed.

Primary author: MAGAZZU, Guido (INFN - Section of Pisa / UCSB - Department of Physics)

Co-authors: AMENDOLA, Antonio (University of Pisa - Department of Information Technology (DII-EIT)); TONGIANI, Claudio (University of Pisa - Department of Information Technology (DII-EIT)); BIANCHI, Giovanni (University of Pisa - Department of Information Technology (DII-EIT)); INCANDELA, Joseph (UCSB - Department of Physics); FANUCCI, Luca (University of Pisa - Department of Information Technology (DII-EIT)); MINUTI, Massimo (INFN - Section of Pisa); VERDINI, Piero Giorgio (INFN - Section of Pisa); CASTALDI, Rino (INFN - Section of Pisa); ROSSIN, Roberto (UCSB - Department of Physics); SAPONARA, Sergio (University of Pisa - Department of Information Technology (DII-EIT))

Presenter: MAGAZZU, Guido (INFN - Section of Pisa / UCSB - Department of Physics)

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