Contribution ID: **15** Type: **Oral presentation**

A high efficiency readout architecture for a large matrix of pixels.

Thursday, 4 February 2010 11:15 (25 minutes)

Based on the requirements of new generation vertex detectors, we present an innovative readout architecture for a large matrix of pixels (A>1.2 cmˆ2) capable to sustain high data rates (˜100 MHz/cmˆ2) with high efficiencies (> 97%).
The readout is based on the parallel sparsification of one entire matrix column per clock cycle. The scan logic activates in sequence only the columns that present hits. Time labeling is performed by the central logic that divides the incoming hits into precise time windows defined by a dedicated clock. The column scan algorithm preserves the time sorting of the hits during their extraction from the matrix, allowing a simple integration in a triggered system, though considering the data-driven nature of the chip. In this architecture, which is strongly horizontally parallelized, we introduced an additional parallelization subdividing the matrix into 4 vertical sub-matrices, each one provided with its own readout. A unique output stage implements a data compression algorithm based on the time&space sorting of the hits and it has been optimized for clustered events. The architecture has been described in synthesizable (Synopsys) and highly parameterized VHDL code. The validation process passed through several simulations. The efficiency results obtained by these simulations are presented.

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Session Classification: Coupled layer and monolithic architectures II

Track Classification: Coupled layer and monolithic architectures