Towards a high performance vertex detector based on 3D integration of Deep N-Well MAPS

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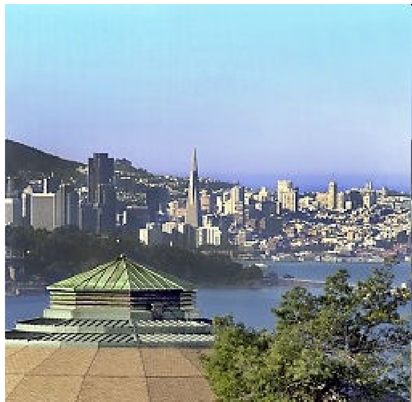
on behalf of the VIPIX collaboration



WIT2010 – Workshop on Intelligent Trackers

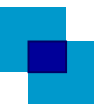
February 3-5, 2010, Lawrence Berkeley National Lab

Outline

- Deep N-Well MAPS from 2D to 3D: putting more intelligence

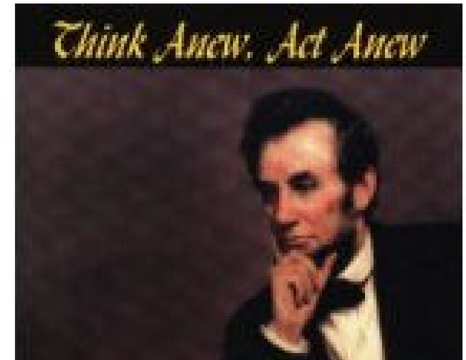
  - in the pixel
  - in the chip
  - in the system

- Perspectives & SuperB Silicon Vertex Tracker



New concepts enabled by 3D integration of readout chips and sensors

- "The occasion is piled high with difficulty, and we must rise with the occasion. As our case is new, so we must think anew, and act anew"



- Physicists and IC designers have to think in a 3D fashion

Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential

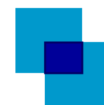
SHAPER
PREAMPL
DISC
LATCH

Digital section
NMOS
NMOS
p–well
PMOS
PMOS
Analog section
deep n–well
n–well
p–substrate

A classical optimum signal processing chain for capacitive detectors can be implemented at pixel level:

- Charge-to-Voltage conversion done by the charge preamplifier

- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located

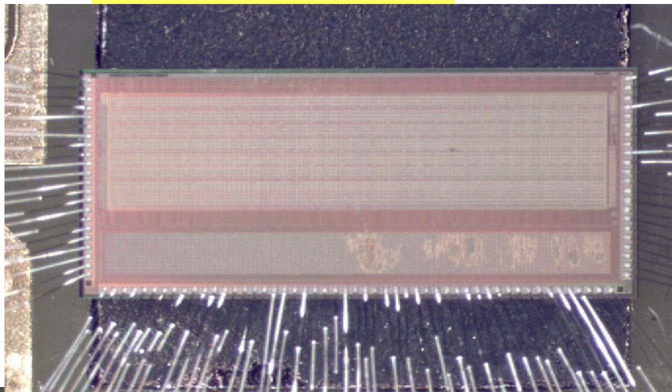


Development of "intelligent " Deep N-Well MAPS

- Key points:
  - Develop **a light tracking system** for the next generation of experiments
    - MAPS with small pitch, capable of handling high data rates by pixel-level data sparsification and time stamping
  - Develop a **trigger system able to identify tracks online**
    - Data-push MAPS readout architecture
    - Associative memories $\Rightarrow$ Level 1 trigger on tracks with low latency

First generation of 130 nm CMOS DNW MAPS sensors with in-pixel sparsification and time stamping

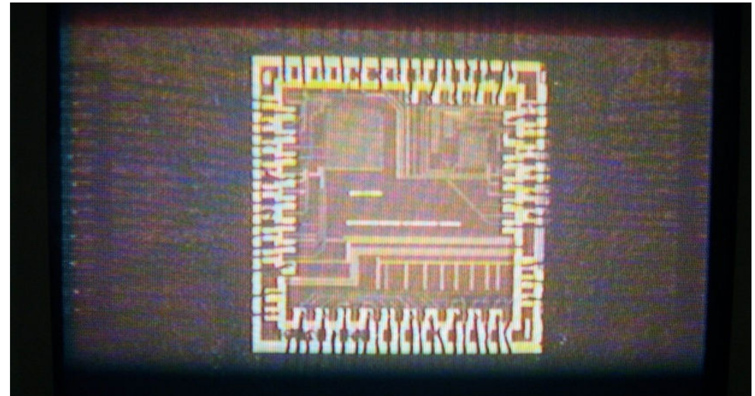
APSEL4D



32x128 matrix.
Data Driven, continuously operating sparsified readout
Beam test Sep. 2008

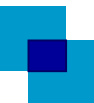
50x50 μm pitch

SDR0



16x16 matrix + smaller test structures.
Intertrain sparsified readout

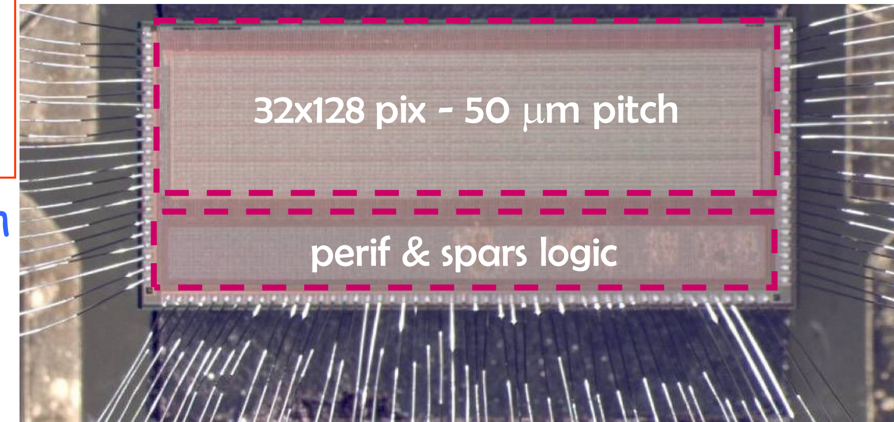
25x25 μm pitch



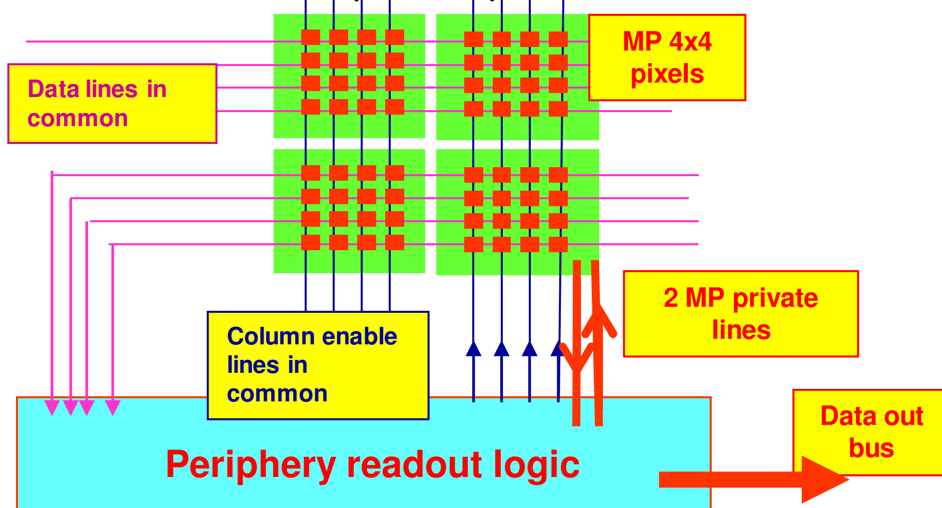
APSEL4D

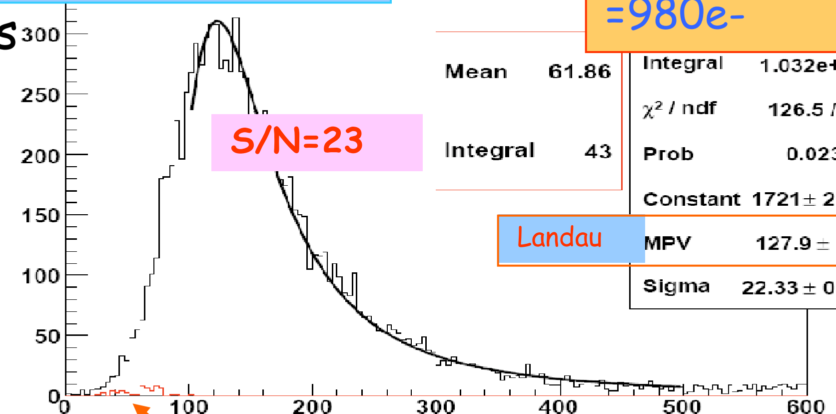
In the active sensor area we minimized:

- logical blocks with PMOS to reduce the area of competitive n-wells
- digital lines for point to point connections to allow scalability of the architecture with matrix dimensions



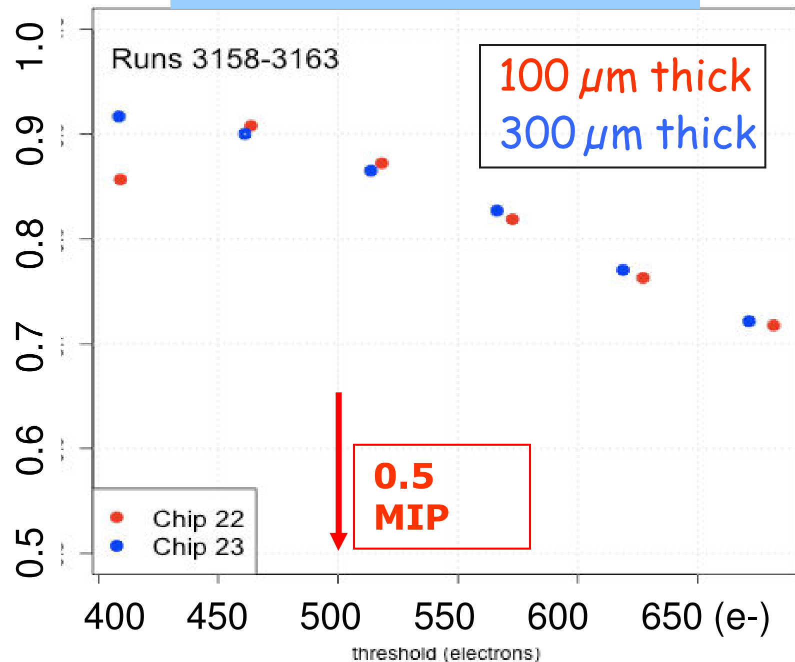
- S/N up to 25 with power consumption ~ 30 μW/ch
- 4K(32x128) 50x50 μm² matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:
  - Register hit MP & store timestamp
  - Enable MP readout
  - Receive, sparsify, format data to output bus





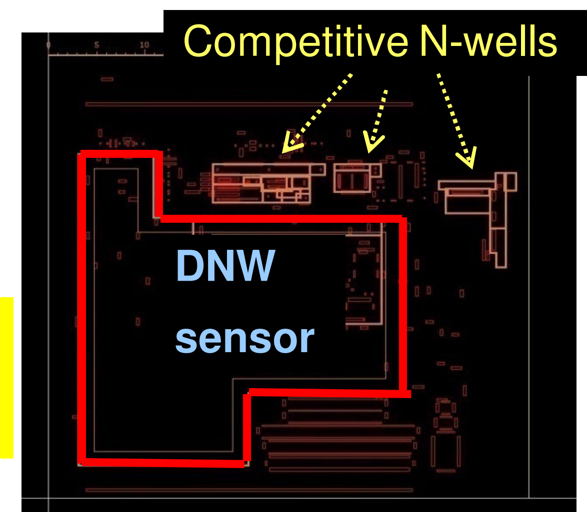
Threshold dispersion = 60 e   Average gain = 860 mV/fC

DNW MAPS Hit Efficiency measured in a CERN beam test (APSEL4D)



Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

- MAPS hit efficiency up to 92 % with threshold @ 400 e- (~ 4σ_noise+2σ_thr_disp)
- 300 and 100 μm thick chips give similar results
- Intrinsic resolution ~ 14 μm compatible with digital readout.

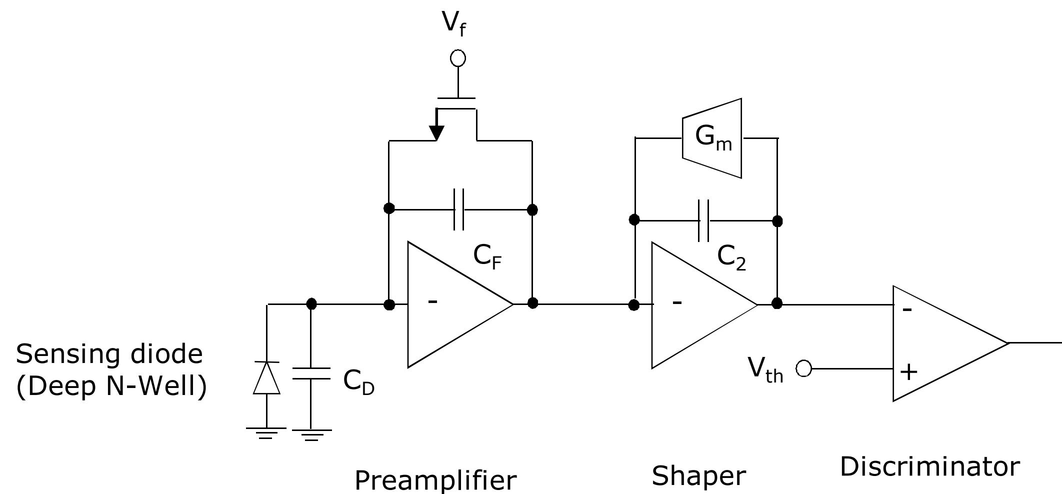


- Competitive N-wells (PMOS) in pixel cell can steal charge reducing the hit efficiency

The analog section in the pixel cell

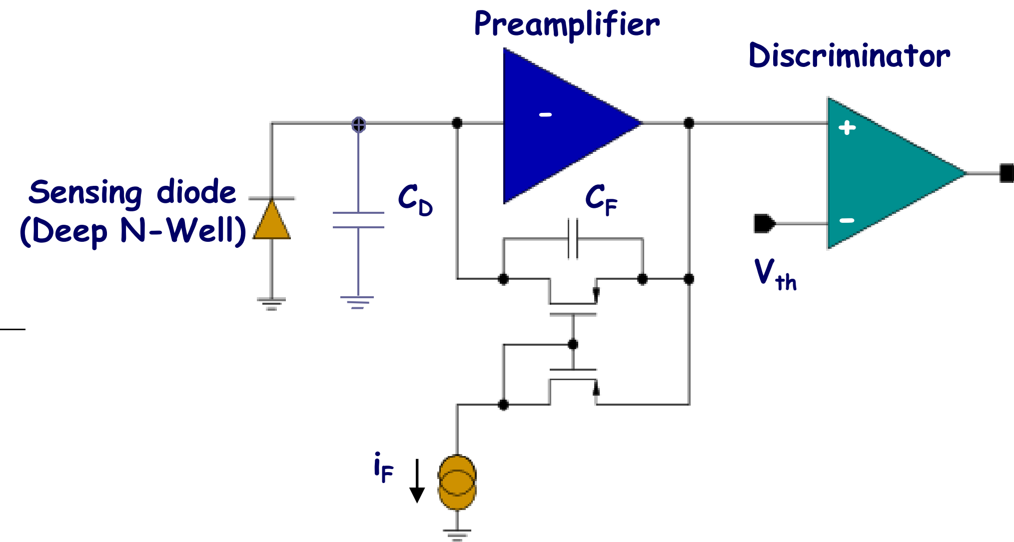
- A new design ("shaperless" analog front-end) and layout (charge collecting electrode with satellite N-wells) of the pixel cell was successfully tested in small test structures (APSEL5T)

APSEL4D

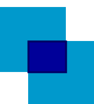


- Pixel cell: 50x50 μm^2
- Sensor capacitance: 400 fF
- Power dissipation 30 μW
- ENC = 60 e rms

APSEL5T



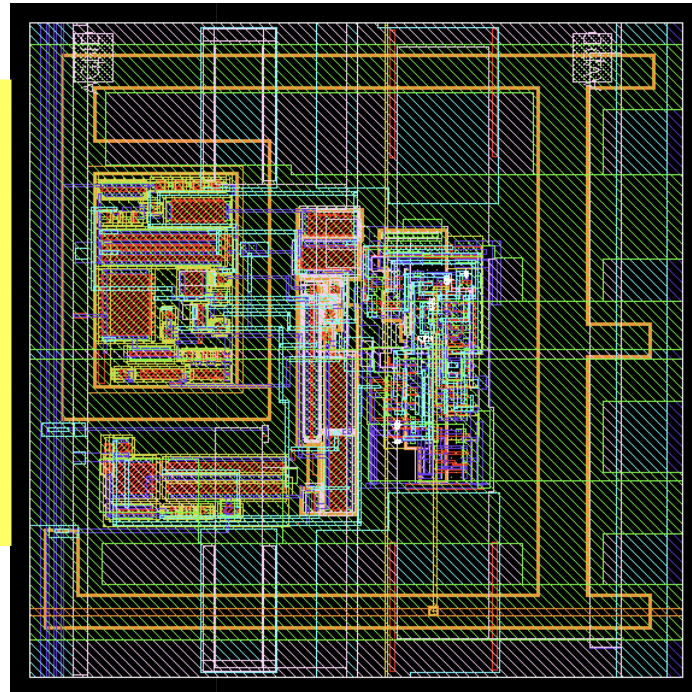
- Pixel cell: 40x40 μm^2
- Sensor capacitance: 270 fF
- Power dissipation: 20 μW
- ENC: 55 e rms



Optimization of sensor layout

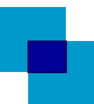
- Small size prototype module with functionalities and cooling/mechanics close to SuperB specifications needs a **128x128 (or 320x80) MAPS chip (APSEL5D)** with 40μm x 40μm pixel cells
  - With respect to APSEL4D, scaling to larger matrix size dictates to remove the shaper stage to make room for additional macropixel private lines and to reduce the pixel pitch
  - Inside the pixel cell, sensor layout has to be changed to increase detection efficiency (→ 99%)

- Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- Optimized cell with satellite N-wells (right): efficiency ~ 99% from TCAD, promising results from laser tests

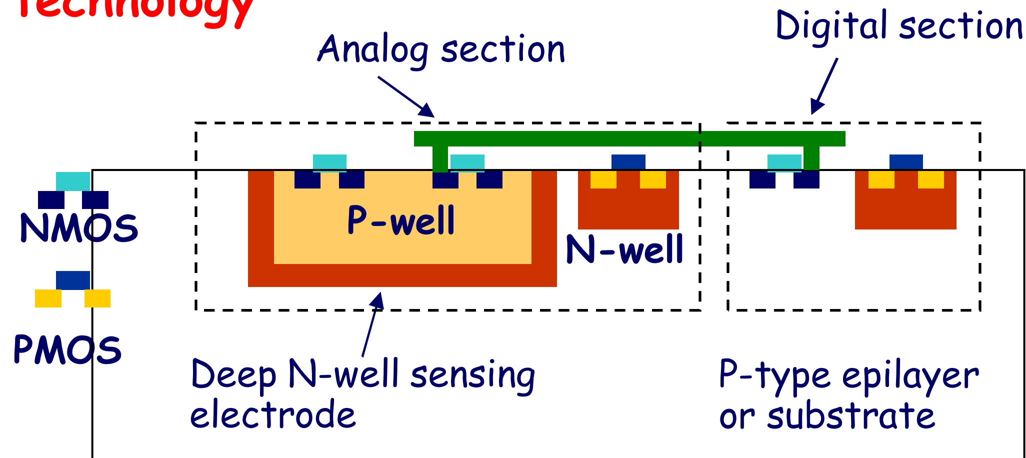


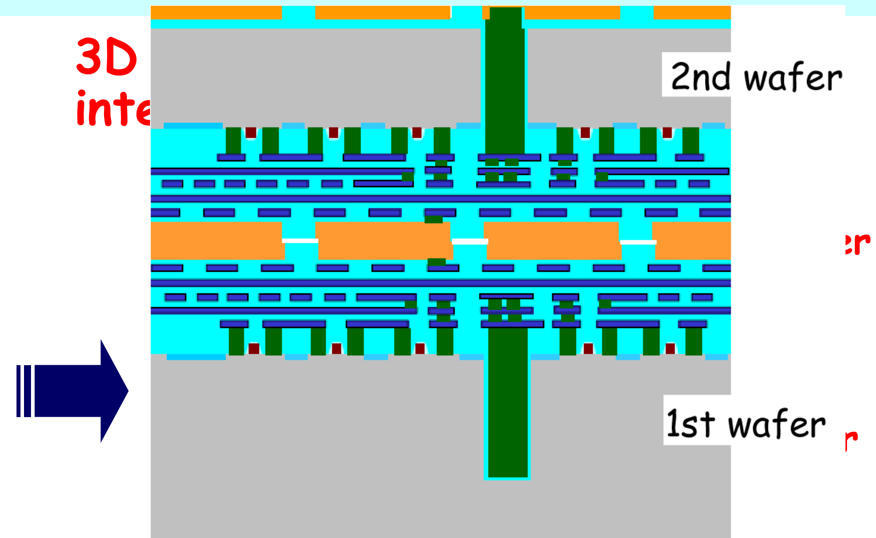
Charge collecting electrode with annular shape

Sensor area: 480μm²
NW-PMOS area: 70μm²
Fill Factor: 0.87



The first 3D CMOS MAPS in the APSEL family

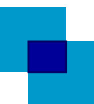




Tezzaron/Chartered technology
(Fermilab MPW run)

- **3DIC Consortium:**
  hosted by Fermi National Accelerator Laboratory, focused on vertical integration, about 15 institutions from U.S., France, Germany, Italy, Poland.

- This Consortium, as a first step, is going to investigate 3D devices based on two layers (“tiers”) of the 130 nm CMOS technology by Chartered Semiconductor, vertically integrated with the Tezzaron interconnection technology.



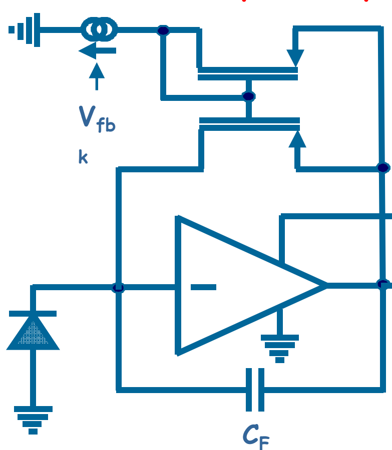
Readout electronics in a 40 x 40 μm² 3D MAPS pixel cell

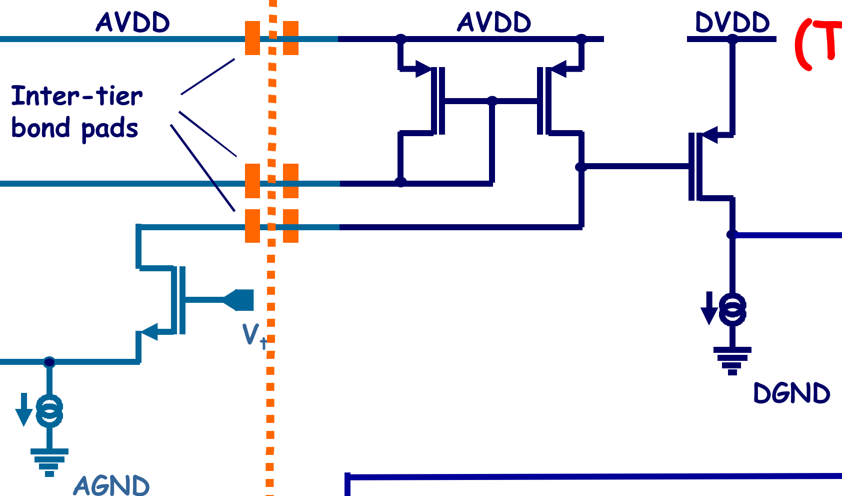
Sensing diode and charge sensitive preamplifier

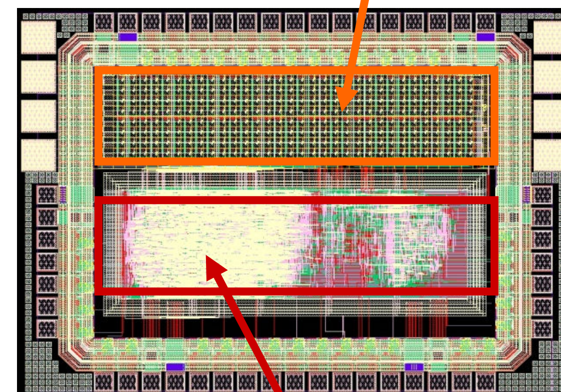
discriminator

TIER 2 (TOP)

Pixel-level digital front end



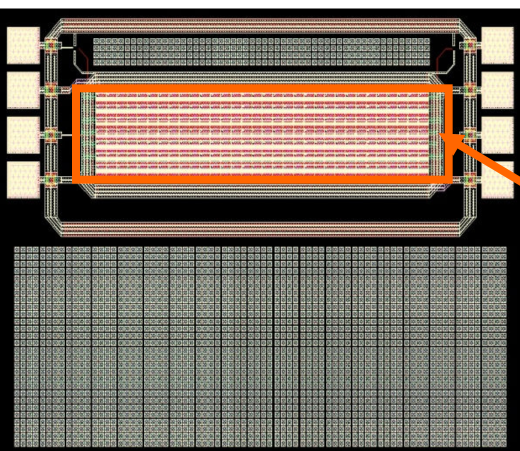




Digital readout electronics

from the discriminator

TIER 1 (BOTTOM)



8x32 pixel matrix

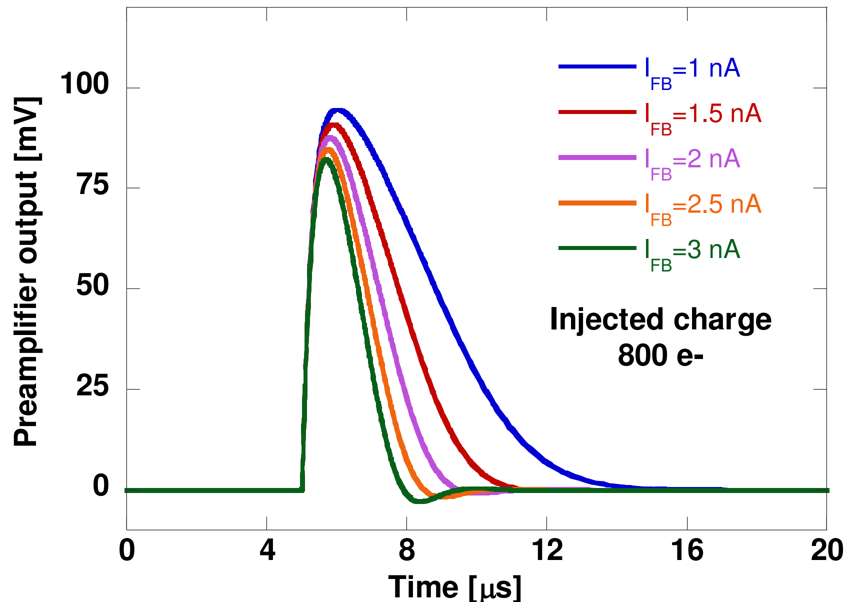
Pixel-level sparsification logic

3D integration removes layout constraints and will allow for an improved readout architecture (no macropixel) in future chips

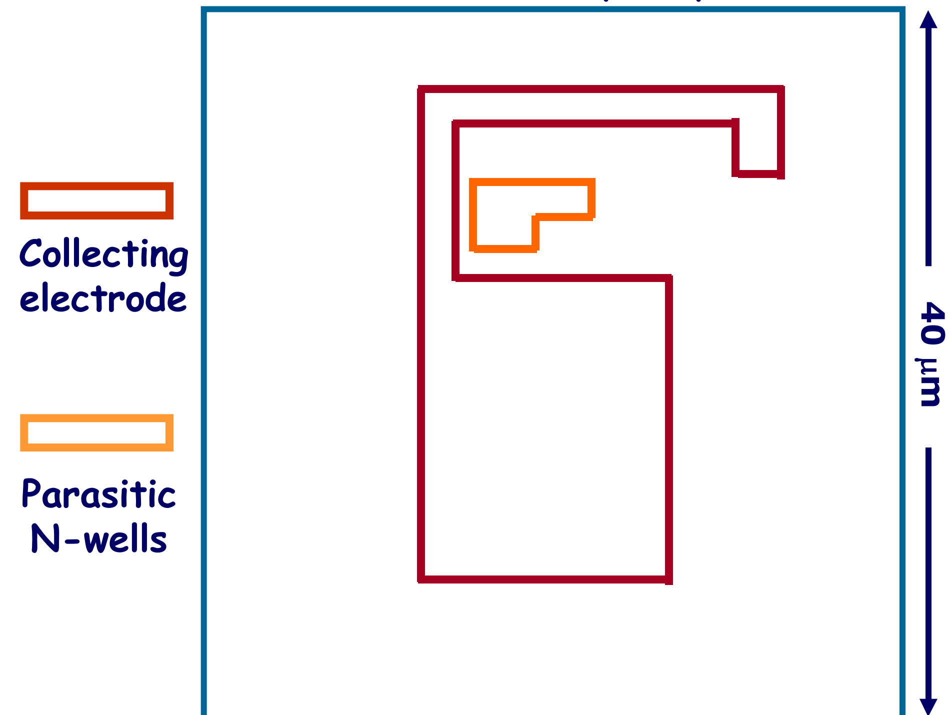
Exploiting 3D integration: pixel pitch and sensor efficiency

Main design features and simulation results

- W/L=30/0.3
- C_D=250 fF
- ~1 μs peaking time
- Charge sensitivity: 750 mV/fC
- Equivalent noise charge (ENC): 33 e rms
- Threshold dispersion: 40 e rms



A three-dimensional technology makes it possible to significantly reduce the area of charge stealing N-wells → significant improvement in charge collection efficiency expected



Sensor area: 346μm²
NW-PMOS area: 22μm²
Fill Factor: 0.94 (0.87 in the "2D" version)

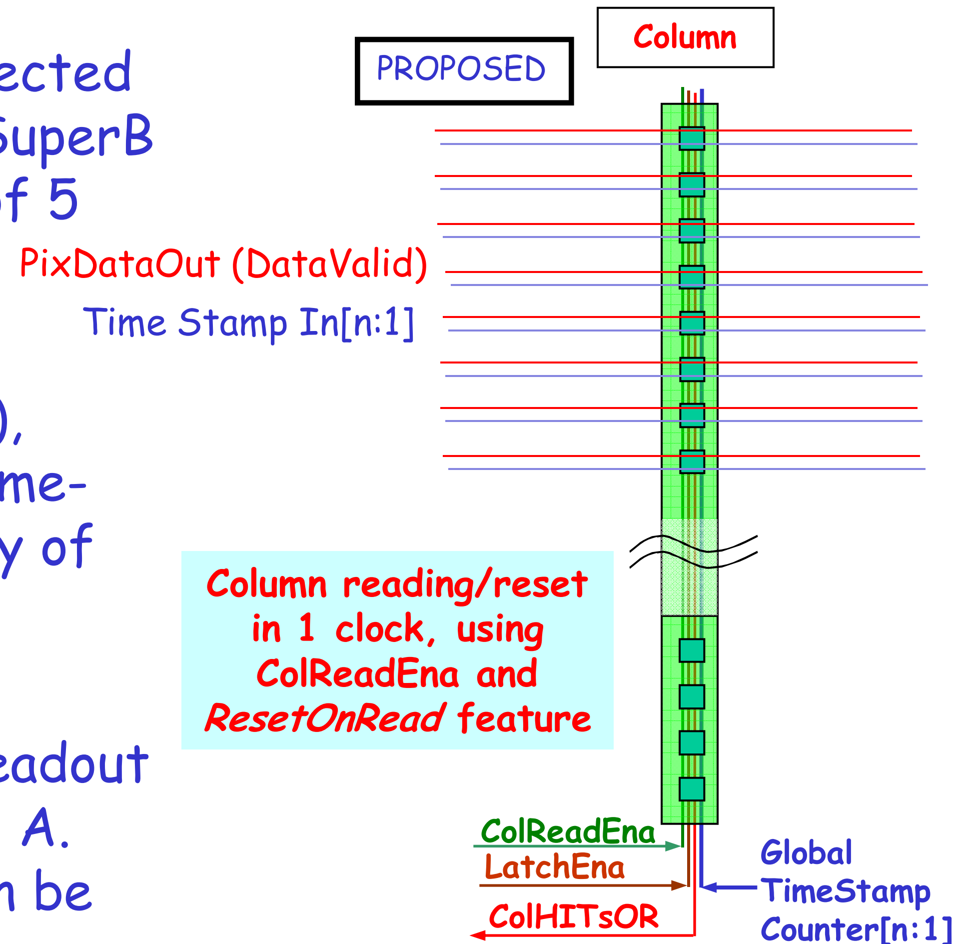
Exploiting 3D integration: readout architecture without MacroPixel

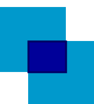
- The MacroPixel arrangement was adopted to reduce the pixel-level logic (limiting the area of competitive N-wells) and the digital switching lines running above pixel columns
- Reasons to eliminate the MacroPixel architecture:
  - **The routing of private lines (FastOR, Latch Enable) scales with matrix column dimension**
  - **Inefficiency due to dead time (freezed MP) depends on MP dimensions**
  - **Not-fired MP columns of fired MPs are also scanned (time consuming) by the sparsification logic**
  - **Only MP masking level can be reasonably implemented**
- Matrix readout speed can increase, also carrying along a readout logic simplification
- Removing the MacroPixel and implementing timestamp latching at the pixel level appears possible with 3D integration, without reducing the pixel efficiency

Exploiting 3D integration: readout architecture

Main goals:

- handle a hit rate of 100 MHz/cm^2 (expected background rate in the Layer0 of the SuperB Silicon Vertex Tracker, with a factor of 5 safety factor)
- In a large MAPS matrix (e.g., 320x216), perform data-driven hit readout in a time-ordered fashion, with a time granularity of 100 ns
- For a discussion of the global matrix readout architecture, see talks by F. Giorgi and A. Gabrielli. Readout efficiency > 98 % can be achieved at a readout clock of 60 MHz

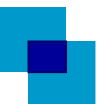




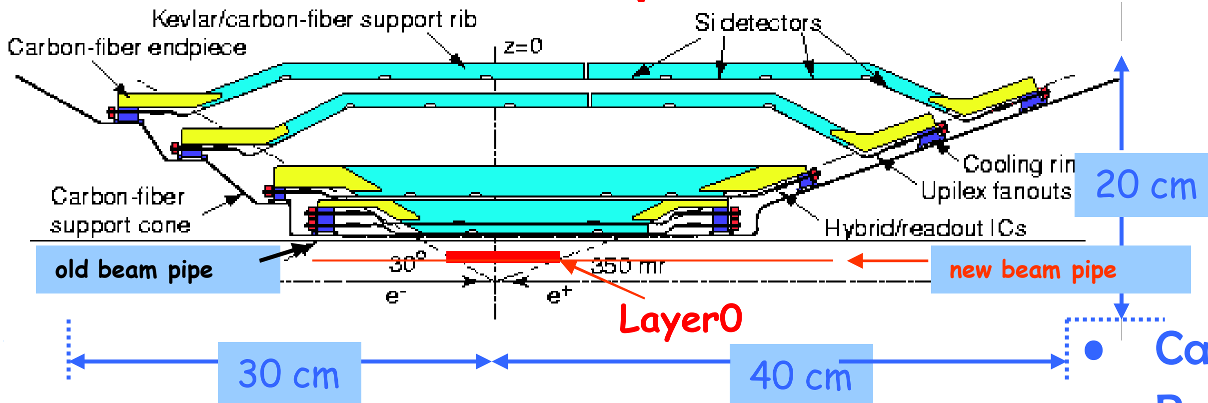
Exploiting 3D integration: pixel-level logic with time-stamp latch and comparator for a time-ordered readout

- A readout time stamp enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that time stamp.
- A column is read only if HIT-OR-OUT=1
- DATA-OUT (1 bit) is generated if the active column has hits associated to a selected time stamp

COL READ ENA
MASK COL SEL
PIXEL BASIC LOGIC
HIT
LATEN
RST
TRANSP LATCH1
TRANSP
LATCHED HIT
TimeStamp
HIT OR IN
TRANSP
TRANSP LATCH2
TS Comp.
TRNSP LATCH
TRNSP
MASK WRITE
READOUT TS BUS
DATA
HIT OR OUT



A possible application of DNW MAPS: the SuperB Silicon Vertex Tracker

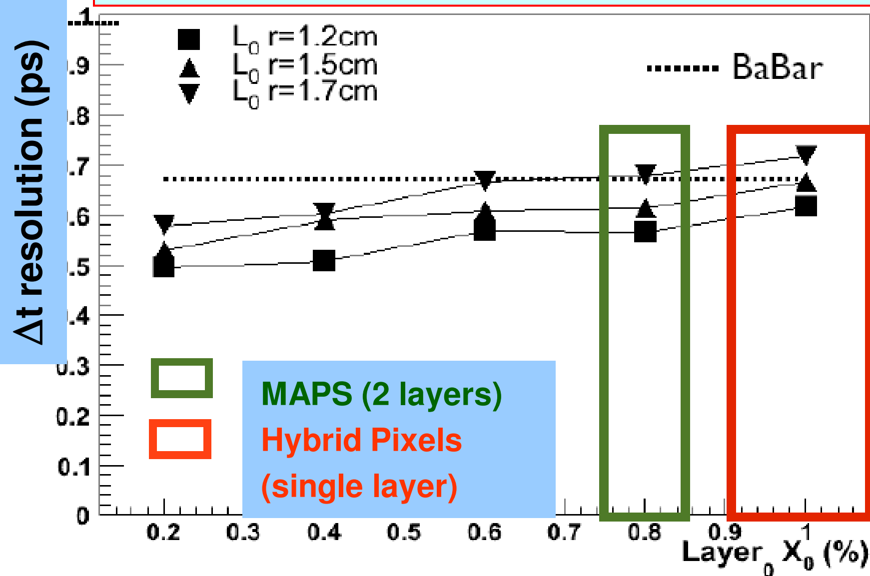


BaBar SVT

- 5 Layers of double-sided Si strip sensor
- Low-mass design. (P_t < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15μm at normal incidence

- Can use Babar SVT design for R>3cm
- Reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) requires improved vertex resolution
  - Layer0 very close to the IP (R~ 1.5 cm) with low material budget
- Background levels depends steeply on radius
  - Layer0 needs to have fine granularity and radiation tolerance

B→π π decay mode, βγ=0.28, beam pipe X/X0=0.42%, hit resolution =10 μm



- Layer0 subject to large background and needs to be extremely thin:

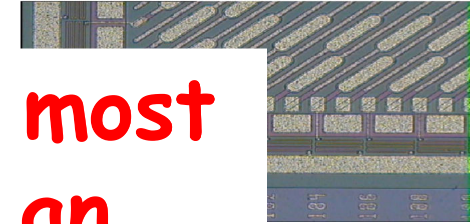
> 5MHz/cm^2, > 1MRad/yr, < 1 %X_0

SuperB SVT Layer 0 technology options

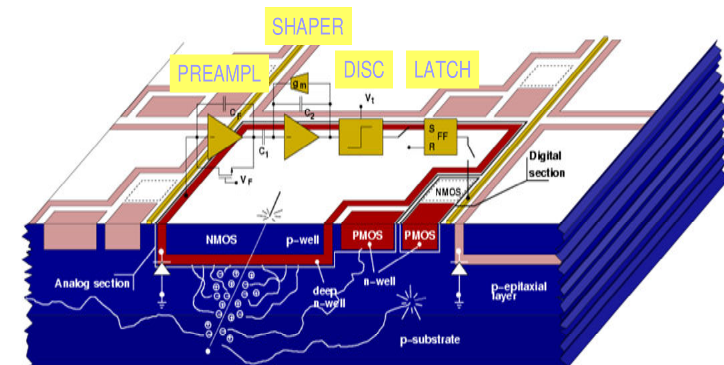
- **Striplets option:** mature technology, not so robust against background

2D and 3D MAPS are the two most advanced options (possibly for an SVT upgrade):

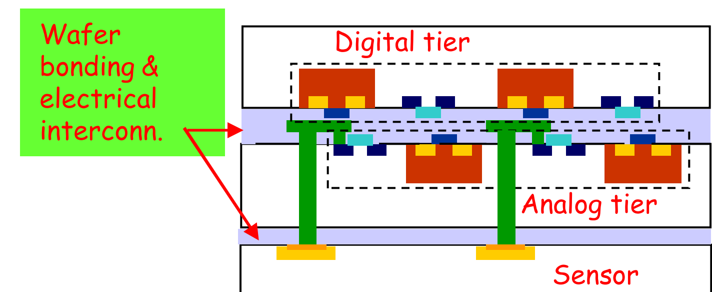
Complexity



- readout developed for CMOS DNW MAPS.
  - First prototype FE chip submitted by the end of 200
- **CMOS MAPS option:** new & challenging technology:
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-Collaboration) on
    - Deep N-well devices 50x50μm² with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS with 4k pixels successfully tested with beams.



- **Thin pixels with Vertical Integration:**
  - Reduction of material and improved performance possible with the technology leap offered by vertical integration.
  - DNW MAPS with 2 tiers (Chartered/Tezzaron 130 nm) submitted in August 2009.

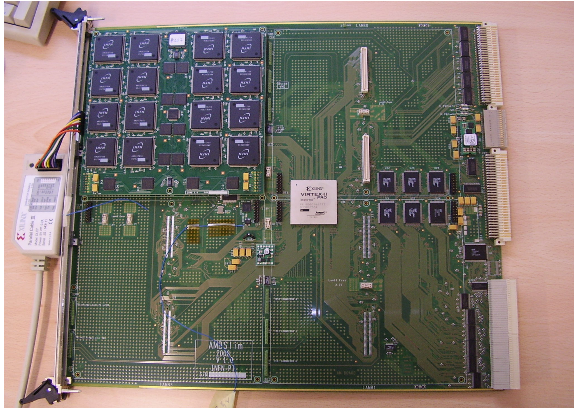


DNW MAPS in an intelligent tracking system: data-push readout and level 1 tracking trigger with associative memories

- In future experiments with increased particle density and number of channels, the data push readout scheme of DNW MAPS makes it possible to use pixel data for the generation a flexible level 1 track trigger based on associative memories, with short latency (< 1 μs) and high efficiency.

- Generation of a Level 1 track trigger information with associative memories was tested in a beam at CERN for the first time in 2008 by the Italian SLIM5 collaboration.

Level 1 tracking with Associative Memories

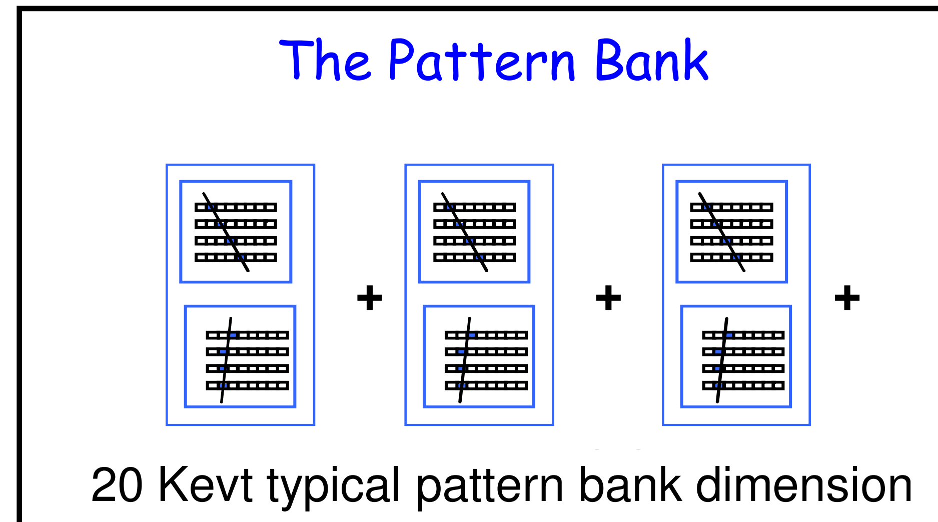


All tracks of physical interest correspond to bit patterns (hit in different detector layers) that are stored in a data bank. An input set of hits is compared in parallel with all stored patterns, and a trigger is fired in case one or more matching patterns are found.

A time-ordered hit readout from pixel sensors would simplify the logic that feeds events to the AM.

The pattern matching can be very fast for online track reconstruction thanks to the Associative Memory (AM) parallelism (all stored patterns are compared to the event at the same time).

Trigger latency below 700 ns

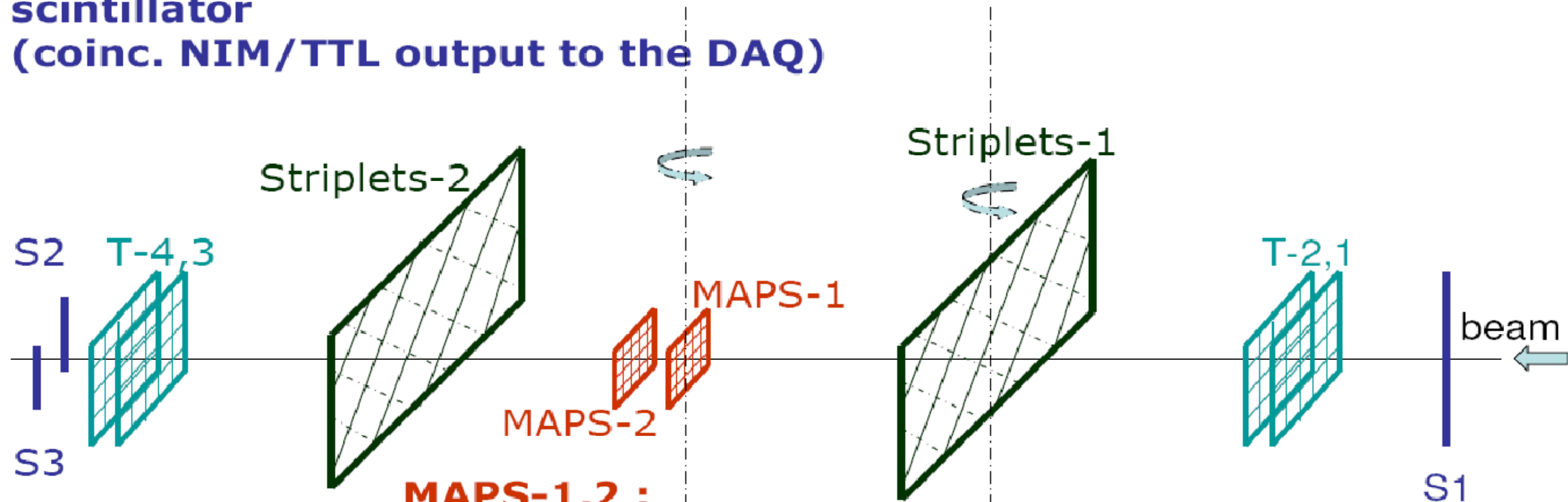


SLIM5 CERN beam test with APSEL4D

The "DEMONSTRATOR"

(conceptual)

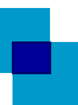
S-1,2,3
scintillator
(coinc. NIM/TTL output to the DAQ)



MAPS-1,2 :
active area ~10 mm²
Cell:50x50 μm² (300→100 μm-thick)

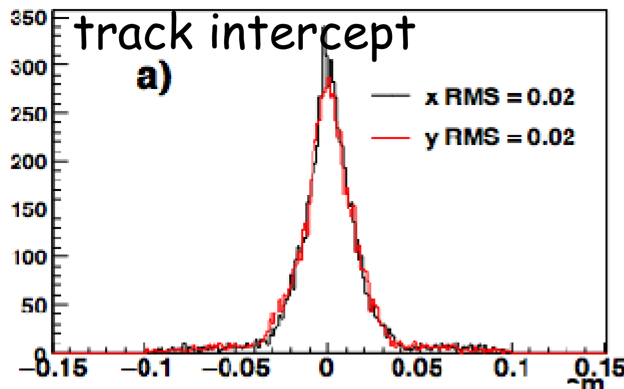
Reference telescope T-1,2,3,4:
area~2x2 cm²
DSSD 300μm thick
25 p-side, 50 n-side μm pitch
50 μm r.o. pitch
(3 chips FSSR2/side)

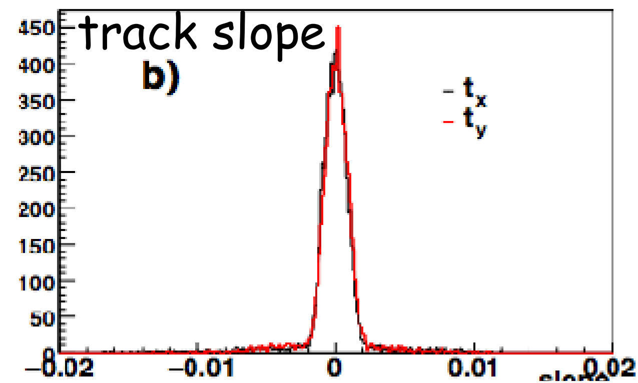
Striplets-1,2:
area 1.29x6.0 cm²
DSSD 200μm thick (∠45°)
25 p-side, 50 n-side μm pitch
50 μm r.o. pitch
(3 chips FSSR2/side)

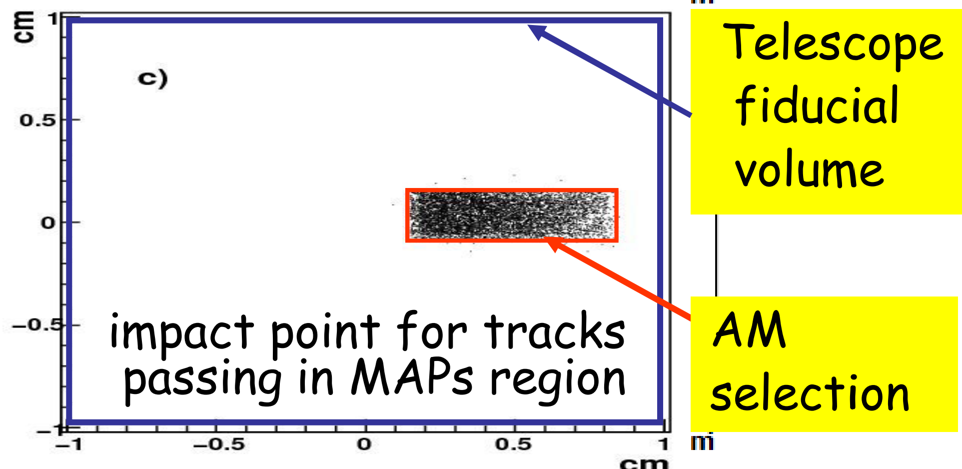


Beam test results for L1 trigger with associative memories

Data from telescope layers were sent to an associative memory board, with pattern banks requiring tracks to pass through the MAPS region. The comparison between offline tracks and online-identified tracks yields a difference in track parameters compatible with the patter bank resolution.







- Associative memories L1 trigger based on tracker information has been successfully operated!
- Low latency (about 700 ns).
- Very low fake rate

Conclusions

- Deep N-Well MAPS have the ambition of being monolithic devices with similar functionalities as hybrid pixels (e.g., pixel-level sparsification and time stamping).
- Their performance can greatly benefit from 3D vertical integration in terms of both electronics and sensor
- They are candidates for the innermost layer of the Silicon Vertex Tracker at the high luminosity SuperB Factory
- The data-push architecture of DNW MAPS can be exploited to include the tracker information in the Level 1 trigger, using Associative Memories (which can also benefit from 3D integration* to store a larger number of patterns, increasing the efficiency in detecting tracks)

* L. Sartori, 11th ICATPP, 2009]

The INFN VIPIX collaboration

VIPIX - Vertically Integrated PIXels

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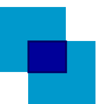
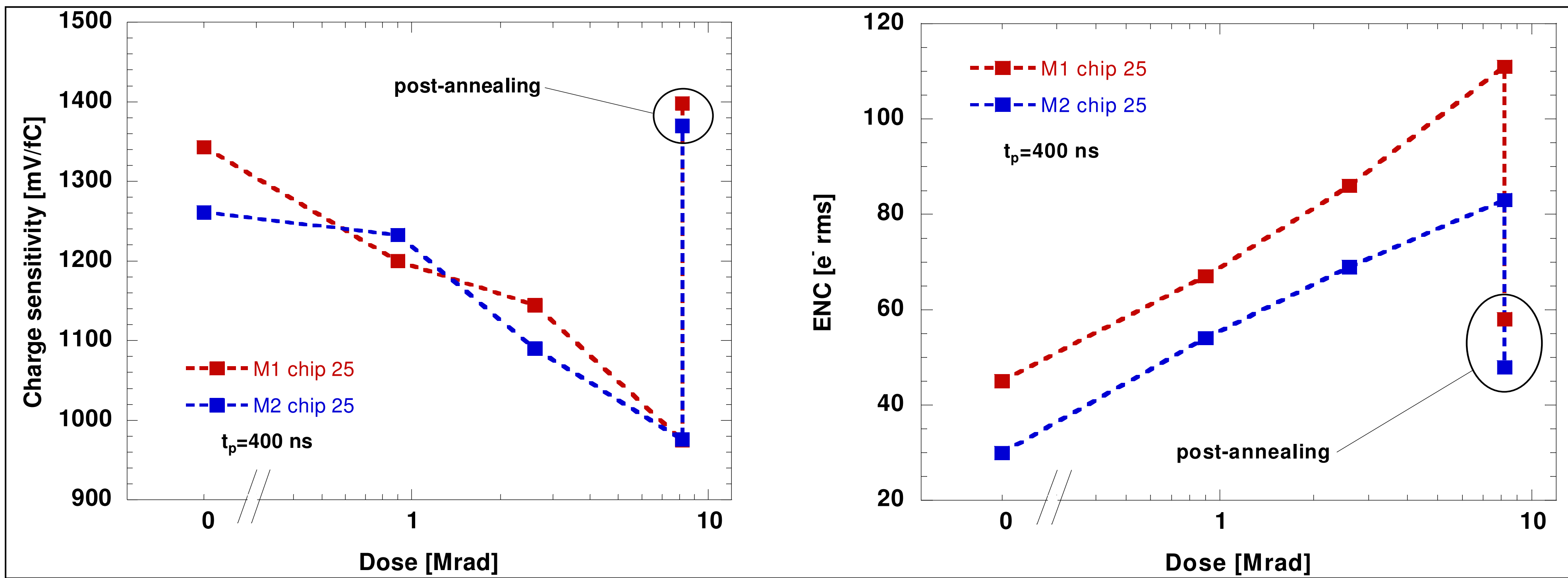
Backup slides



Radiation Damage Tests

- ^{60}Co γ-ray irradiation, 100°C/168h annealing
  - ~10 Mrad maximum integrated dose, 9 rad/s dose rate, MAPS biased as in real application

- Charge sensitivity G_Q decreases with dose; decrease after 900 krad is compatible with the decrease observed in Apsel2T after 1.1 Mrad
- ENC increases with dose; increase after 900 krad is larger than the increase detected in Apsel2T after 1.1 Mrad at similar peaking times (due to different W, finger number and drain current in the input device)
- Significant recovery after 100°C/168h annealing cycle



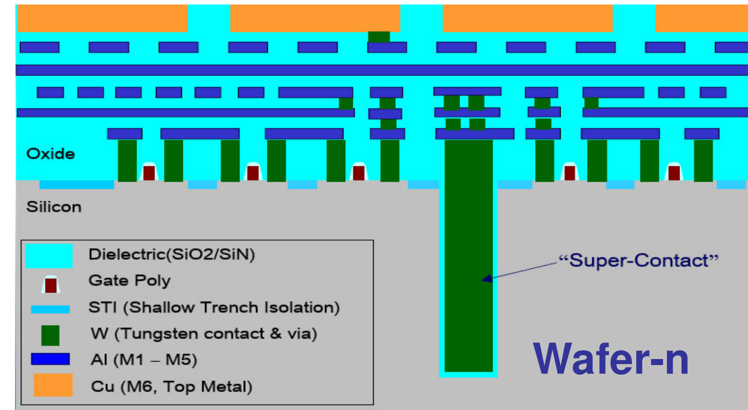
Tezzaron vertical integration process flow (VIA FIRST):

- multi-tier tier chip; Tezzaron includes standard CMOS process by Chartered Semiconductor, Singapore.

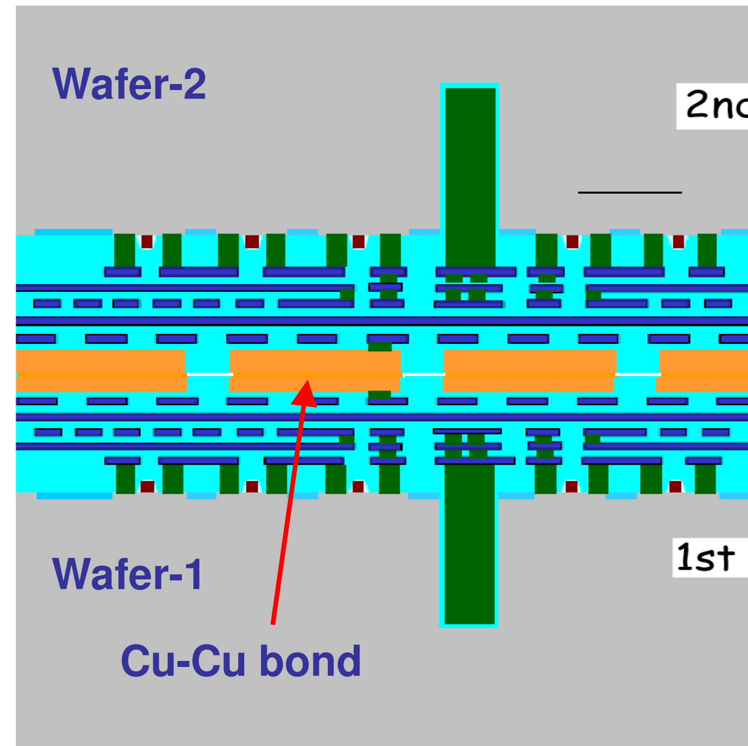
Step 1: Fabricate individual tiers; on all wafers to be stacked: complete transistor fabrication, form super via Fill super via at same time connections are made to transistors

Oxide
Silicon
Dielectric(SiO2/SiN)
Gate Poly
STI (Shallow Trench Isolation)
W (Tungsten contact & via)
Cu (M1 – M5)
Cu (M6, Top Metal)
“Super-Contact”
6 μm
Wafer-n

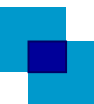
Step2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7 μm)



Step 3: Bond wafer-2 to first wafer-1 Cu-Cu thermo-compression bond

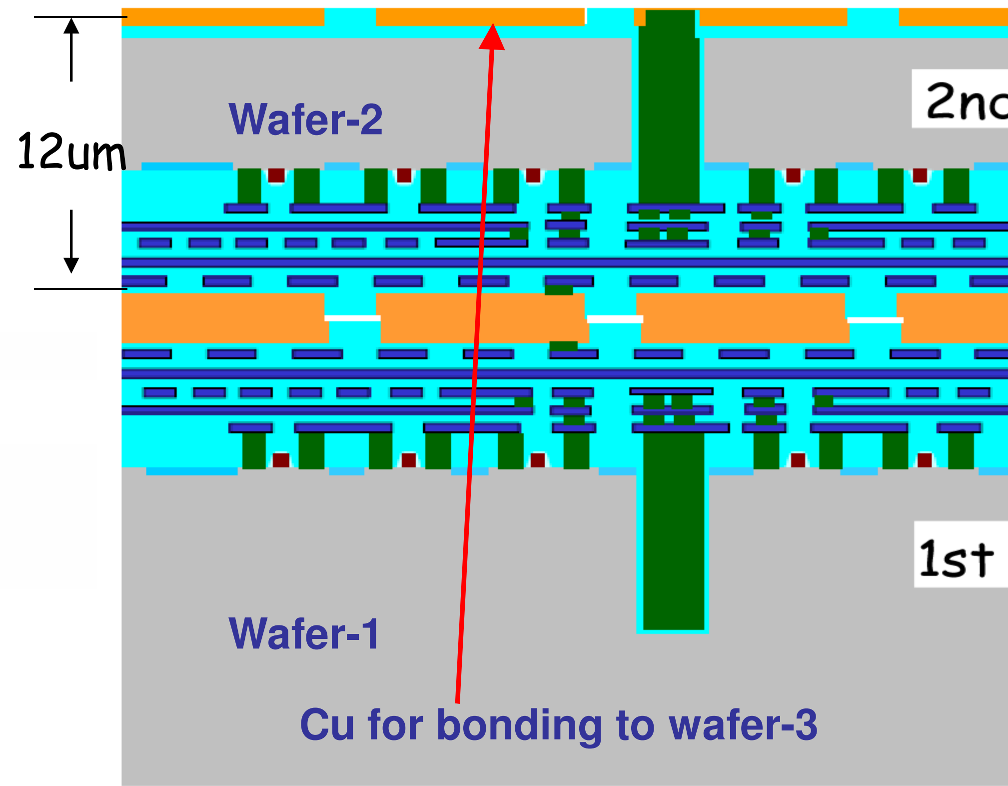


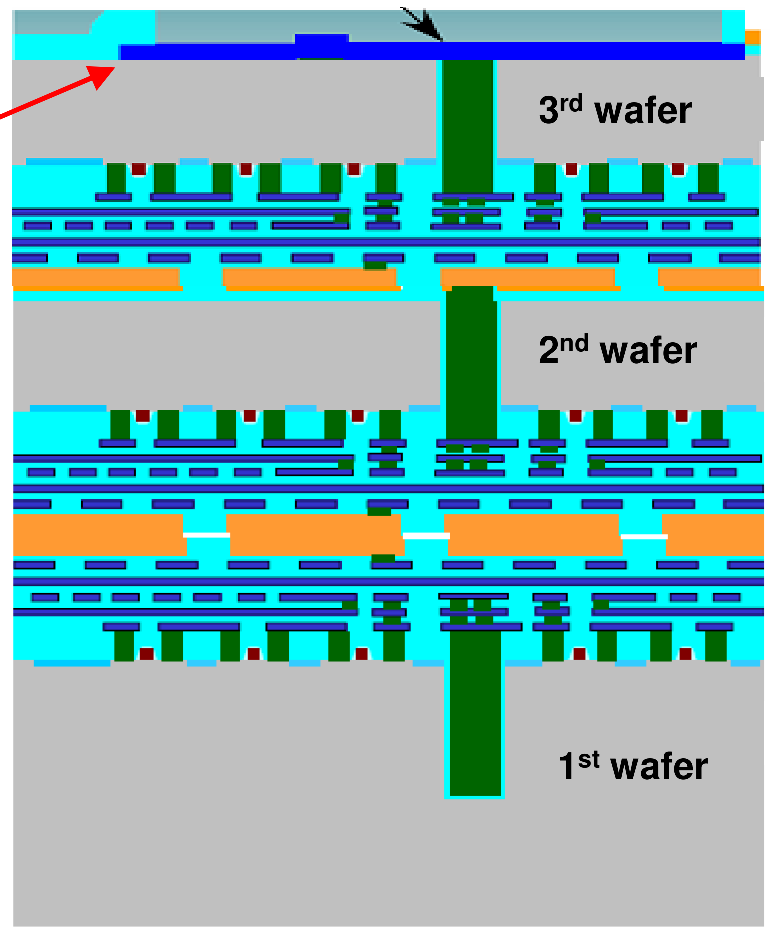
All wafers are bulk



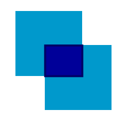
Tezzaron vertical integration process flow:

Step 4: Thin the wafer-2 to about 12 um to expose super via. Add Cu to back of wafer-2 to bond wafer-2 to wafer-3
OR stop stacking now! add metallization on back of wafer-2 for bump bond or wire bond



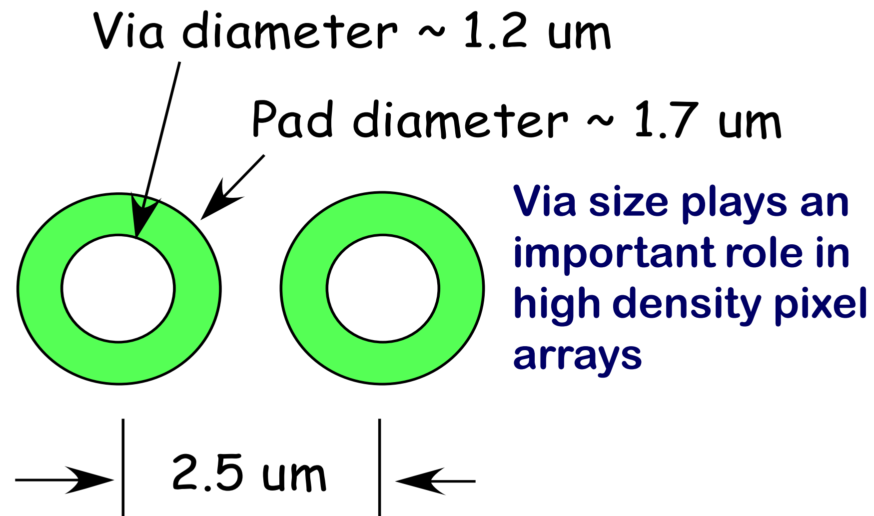


Step 5: Stack wafer-3, thin wafer-3 (course and fine fine grind to 20 um and finish with CMP to expose W filled vias)
Add final passivation and metal for bond pads



Advantages of Tezzaron process

- No handle wafers needed
- No extra space allotment in BEOL processing for vias
- Vias are very small
- Vias can be placed close together
- Minimal material added with bond process
  - 35% coverage with 1.6 um of Cu gives Xo=0.0056%
  - No material budget problem associated with wafer bonding.
- Good models available for Chartered transistors
- Thinned transistors have been characterized
- Process supported by commercial tools and vendors
- Fast assembly
- Lower cost



DAQ system for beam test

To DAQ

1.3 Gbit/s

8.6 Gbit/s

From Front End Chips

S-Link

EPMC1

VME

STRATIX II

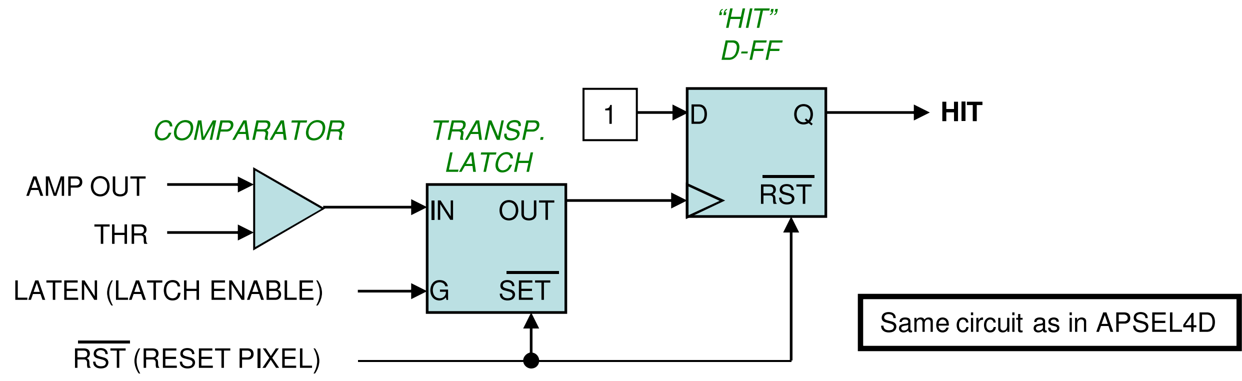
AM interface

1.2 Gbit/s

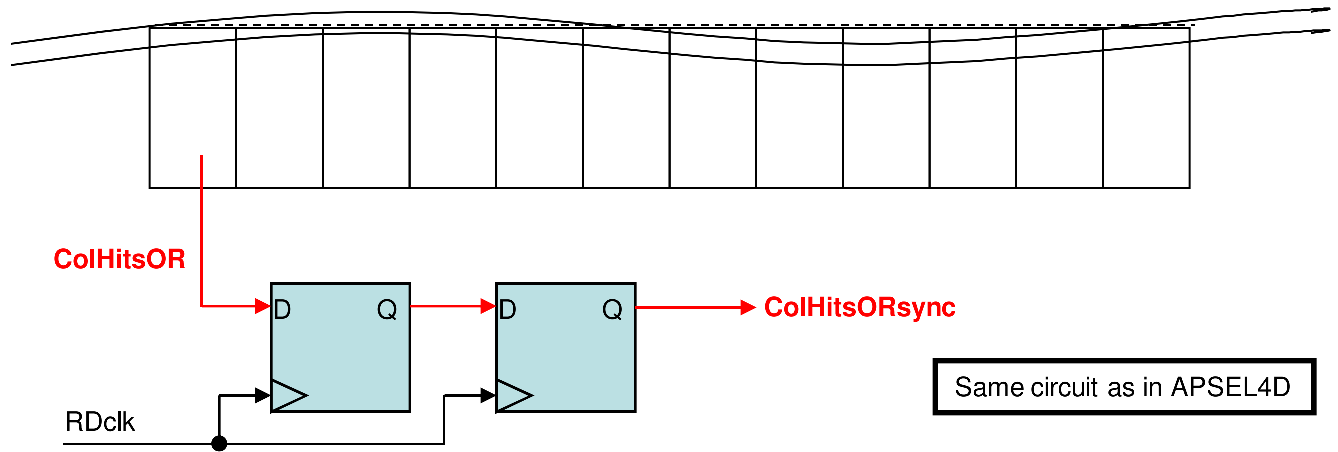
4.3 Gbit/s

- Few DAQ numbers:
- Readout clock 40 MHz
  - 20 MHz MAPS, 60 MHz FSSR2
- Peak L1 processing: 2.5 MHz
- DAQ rate 40 kHz
- 90 M events on disk (40 Gb)

Pixel basic logic and Column HITs OR synchronization



Same circuit as in APSEL4D



Same circuit as in APSEL4D

Macropixel structure in 2D DNW MAPS