Concepts for a Tracker Trigger based on a multi-layer layout and on-detector data reduction using a cluster size approach

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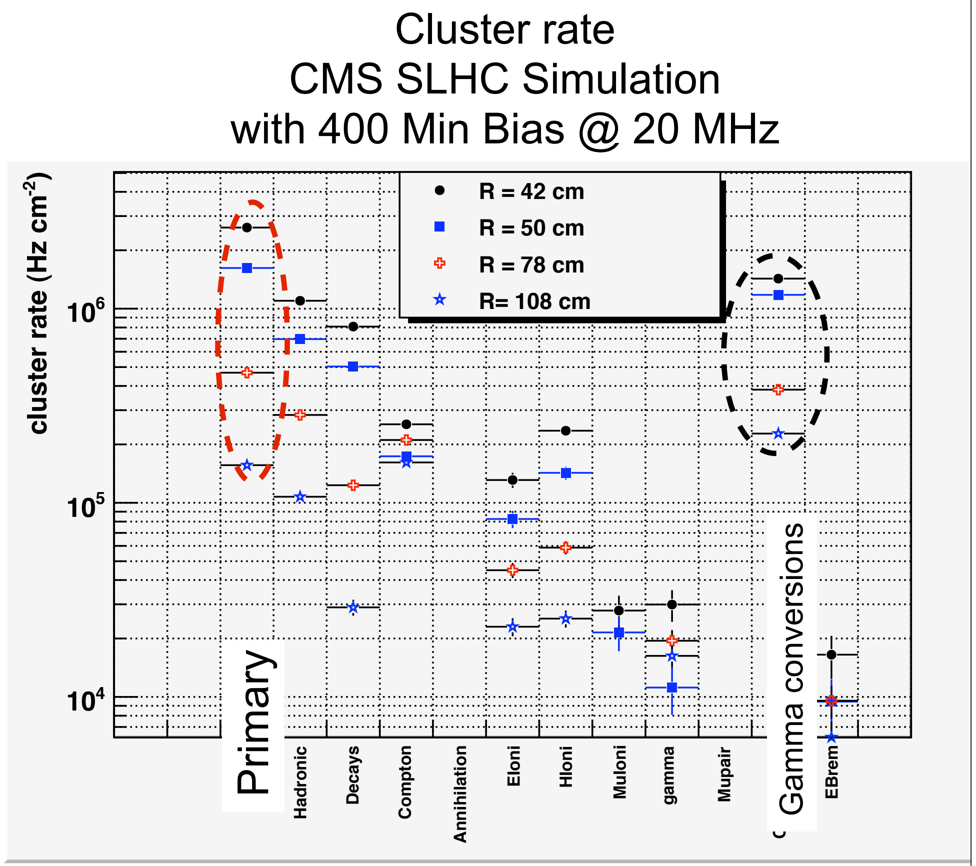
What an Intelligent Tracker for?

- Intelligent tracker: Fast, Efficient, Adaptive
  - Provide tracking capabilities with “extra” abilities - two models
    - Turing: can distinguish from a pure mechanical machine
    - Darwin: can react to unforeseen situations applying knowledge and skills
  - “Extra” is the Trigger: ability to highly reject non-interesting collisions while retaining ~all the good ones
- The presented solution:
  - Extract efficiently and fast the interesting data and process them off-detector
    - Off-detector technologies are intrinsically more flexible and evolve faster than on-detector ones: see CMS HLT example
    - Although the progress in high speed data transmission is fast, a Tracker design for SLHC limits the technology to that available at T_0-[a few years]
  - Rejection of spurious clusters is effective in the reduction of the data rate and the combinatorial background: Cluster width based approach

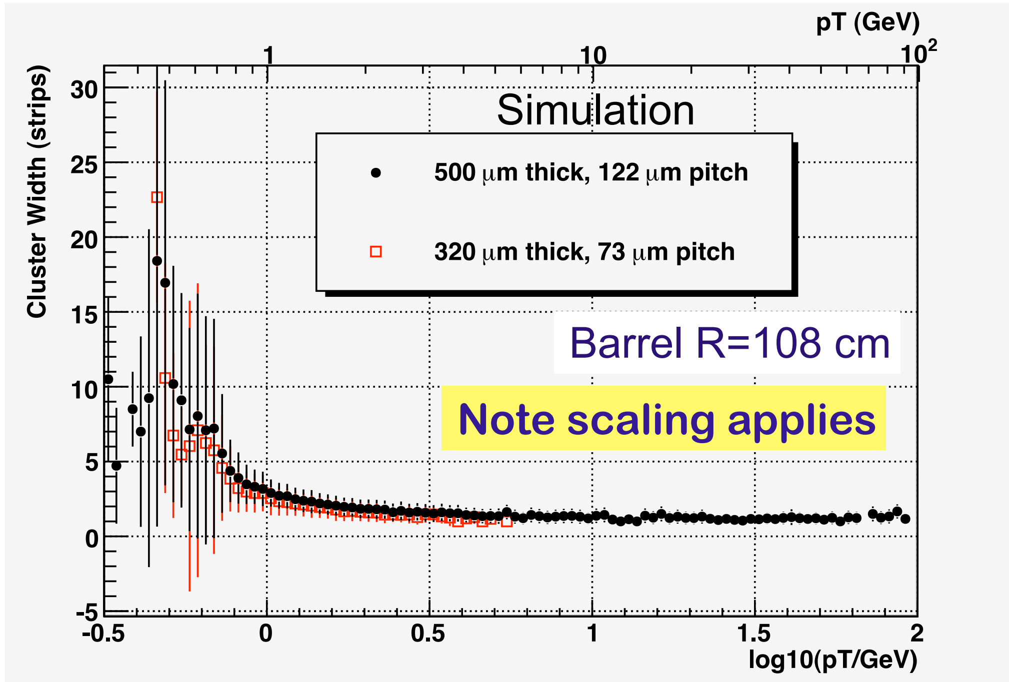
The size of the problem

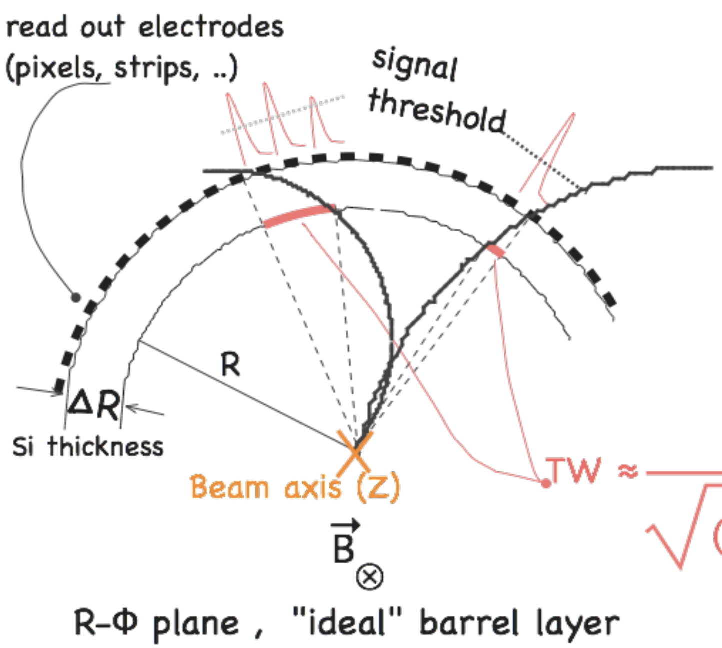
- **Huge data rate at 10^{35} cm^{-2} s^{-1}**
  - Even with a short strip length, that keeps the occupancy to ~1%, the data rate of the fired strips is large
    - R=50 cm: ~ 20 MHz cm^{-2}
    - R=70 cm: ~ 10 MHz cm^{-2}
    - R=100 cm: ~3 MHz cm^{-2}
      - ➨ This of course depends on the electronics details
    - Strips can be clustered to reduce the data rate, typically by a factor ~3, but still large
    - Note the large fraction of the hits coming from photon conversions and nuclear interactions
  - Select only the clusters from "high pT" tracks, based on their typical size



Data rate reduction on sensor

Select high p_T particles using their distinct cluster width (CW) patterns



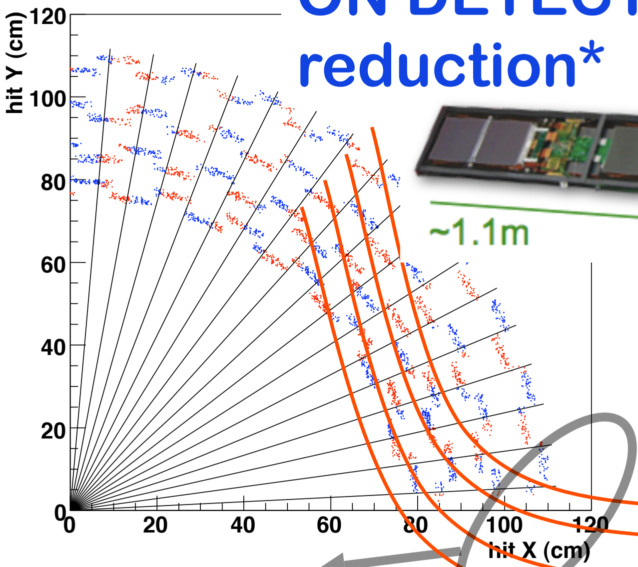


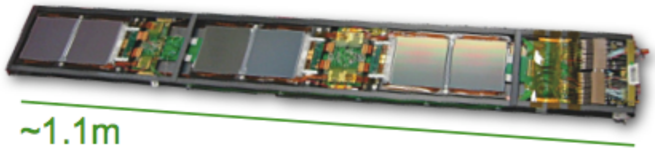
$$TW \approx \frac{\Delta R}{\sqrt{\left(\frac{p_T}{p_{T\,min}}\right)^2 - 1}} \approx \Delta R \frac{p_{T\,min}}{p_T} = 0.15\ B\ \Delta R \frac{R}{p_T}$$

see G. Parrini's talk

Trigger working principle

ON DETECTOR data reduction*

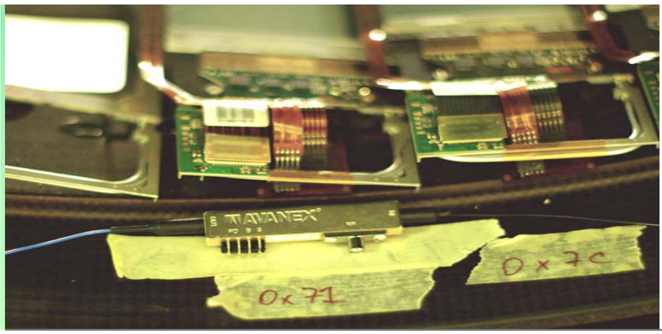




*See also
- G. Parrini's talk
- A. Messineo's talk

OFF DETECTOR
track segments with
fast addressable memories[§]

Fast - O(10-20 Gbps) data links[†]



[§]See U. Heintz talk

[†]See D. Janner's talk

Outline and goals

- Conceptual design of a Tracker with trigger capabilities
  - Case study using silicon strip detectors only
  - Barrel and Endcap coverage
  - Study data reduction using cluster width approach
  - Determine sustainable data rates and "tracking efficiency" for different set of the parameters
  - Estimate the power consumption
- Some electronics R&D in progress
- Validation the method using real data
  - p-p LHC collisions at 900 GeV
  - cosmic muons
- Conclusions

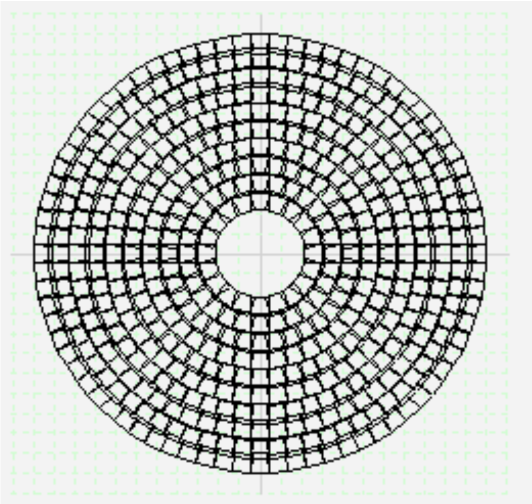
Full GEANT4 simulation

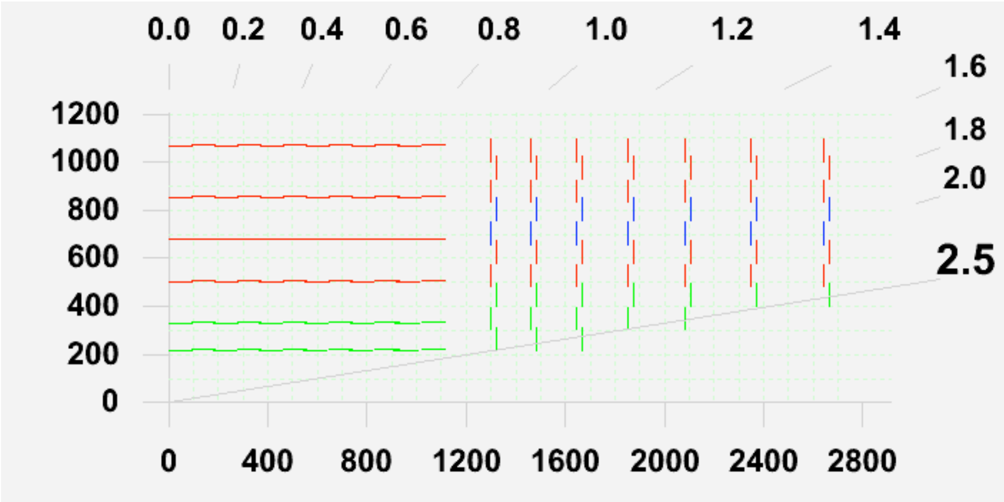
- **Modified Strawman A*:**

  *Dimensions constrained by the Strawman A simulation approach

  - 4 pixel layers (4, 7, 11 and 18 cm)
  - 2 silicon pixel "stacked layers" at 23 and 34 cm (see talk of M. Pesaresi)
  - Trigger layers at: 50, 70, 90, 110 cm (barrel) and 5 rings in the endcaps
    - 320 µm (290 µm active) thickness, n-type bulk, Noise ~ 800 electrons
    - Barrel: 4.72 cm strips length, AC coupling, 3% inter-strip couplings, no Lorentz angle compensation
    - Forward: 5 rings for triggers made of two sensor sandwiches (see A. Messineo and G. Parrini talks)
      - ➨ only fast simulation implemented so far

- **Goal: performance as a function of sensor properties and electronics**





Estimated p_T resolution (barrel)

- Using the above geometry compute the momentum resolution using single muons
  - using full cluster resolution we get ΔpT/pT~0.5% @ 10 GeV
  - However for trigger purposes, a coarser pitch can be used, thus saving bits

σ(pT)/pT with (1 mm)/without beam spot constraint

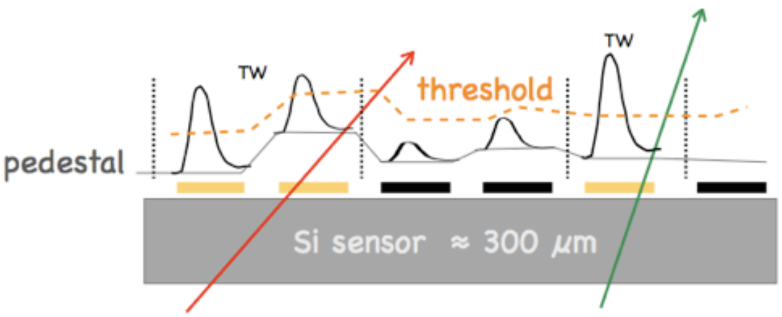
Pitch (μm)	pT=10 GeV	pT=40 GeV	pT=100 GeV
100	0.6%/2.5%	2.5%/8.5%	6%/21%
500	1.3%/11%	5%/42%	13%/105%
1000	2.3%/21%	9%/84%	23%/210%

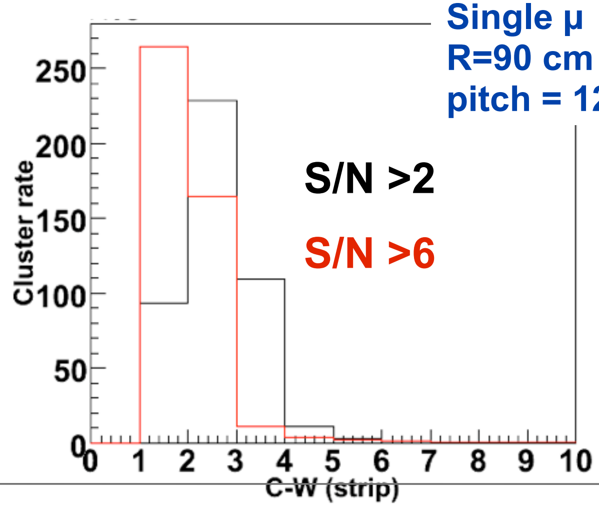
Optimization studies

- Compute cluster (and tracking) finding efficiency vs pT as a function of cluster thresholds and widths in each layer for muons

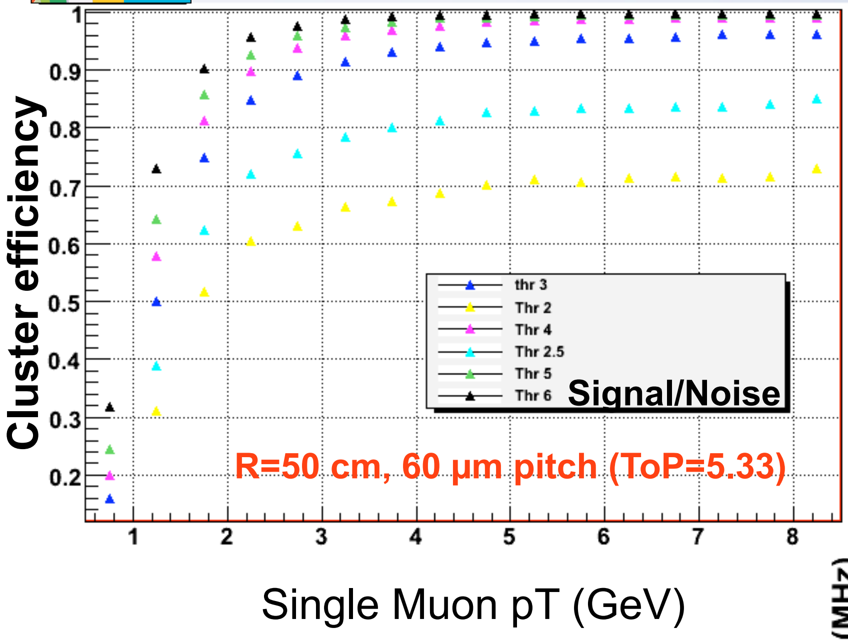
- Compute cluster occupancies, rejection rates for FE-chip and layers for several layer configurations and thresholds for MinBias events (x400 Pileup, 20 MHz LHC clock)

- Optimize the module layout for a given “track cluster efficiency” above a given pT and mean cluster rate per FE-chip





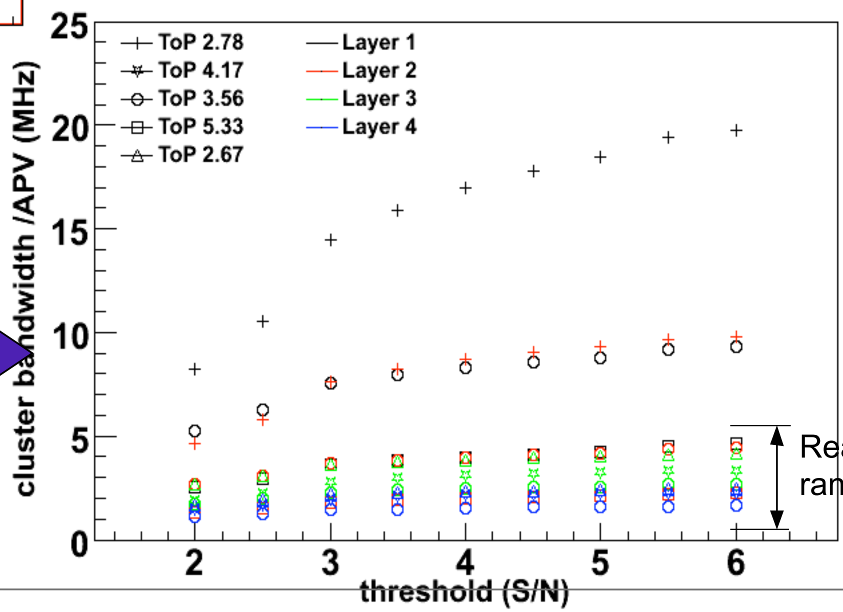
Cluster efficiency and data rate



Fraction of clusters with CW <3 in single muon events

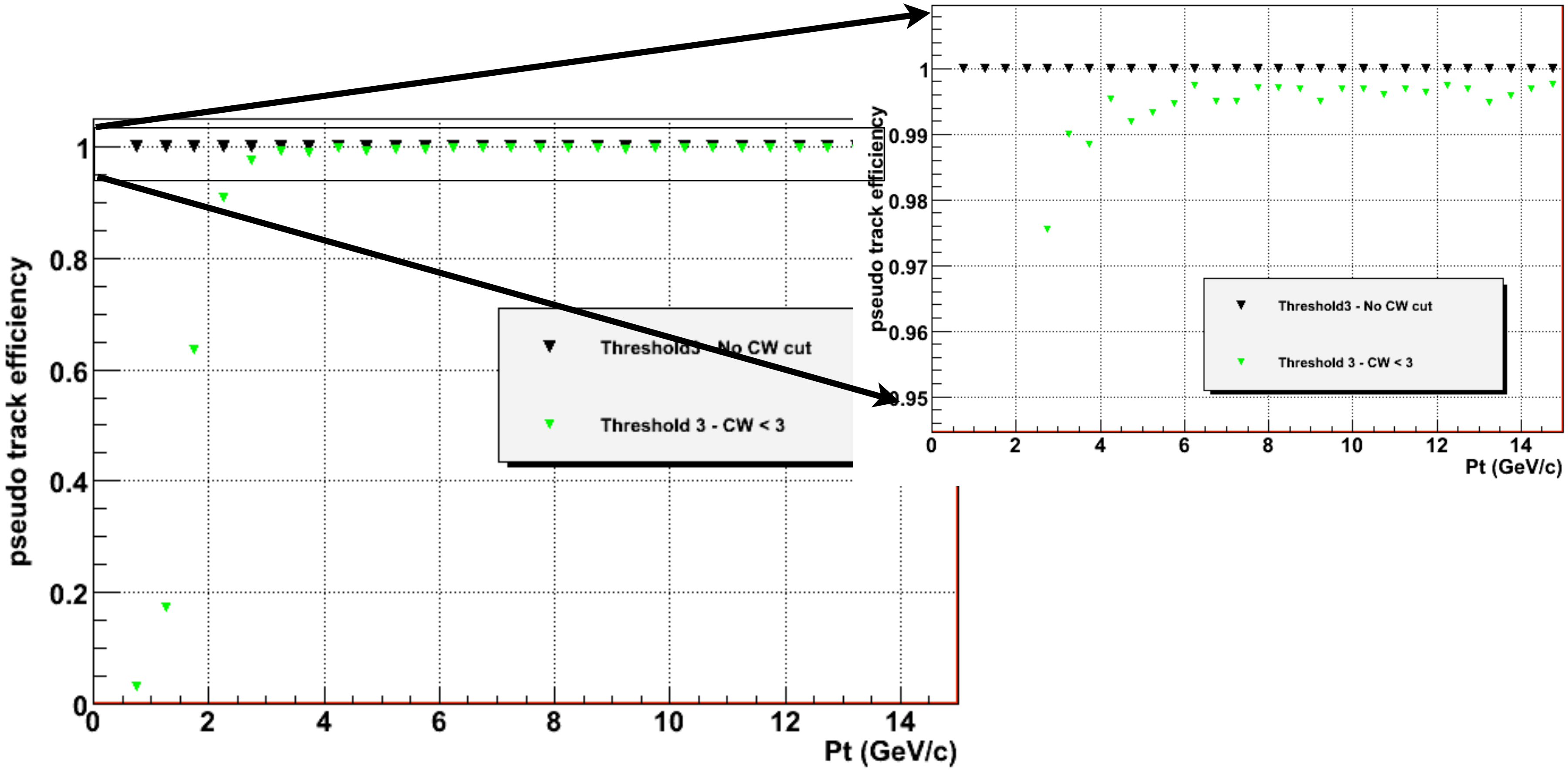
Cluster (CW<3) bandwidth per FE vs Signal/Noise threshold

Various Thickness over Pitch (ToP) in 400 MinBias events

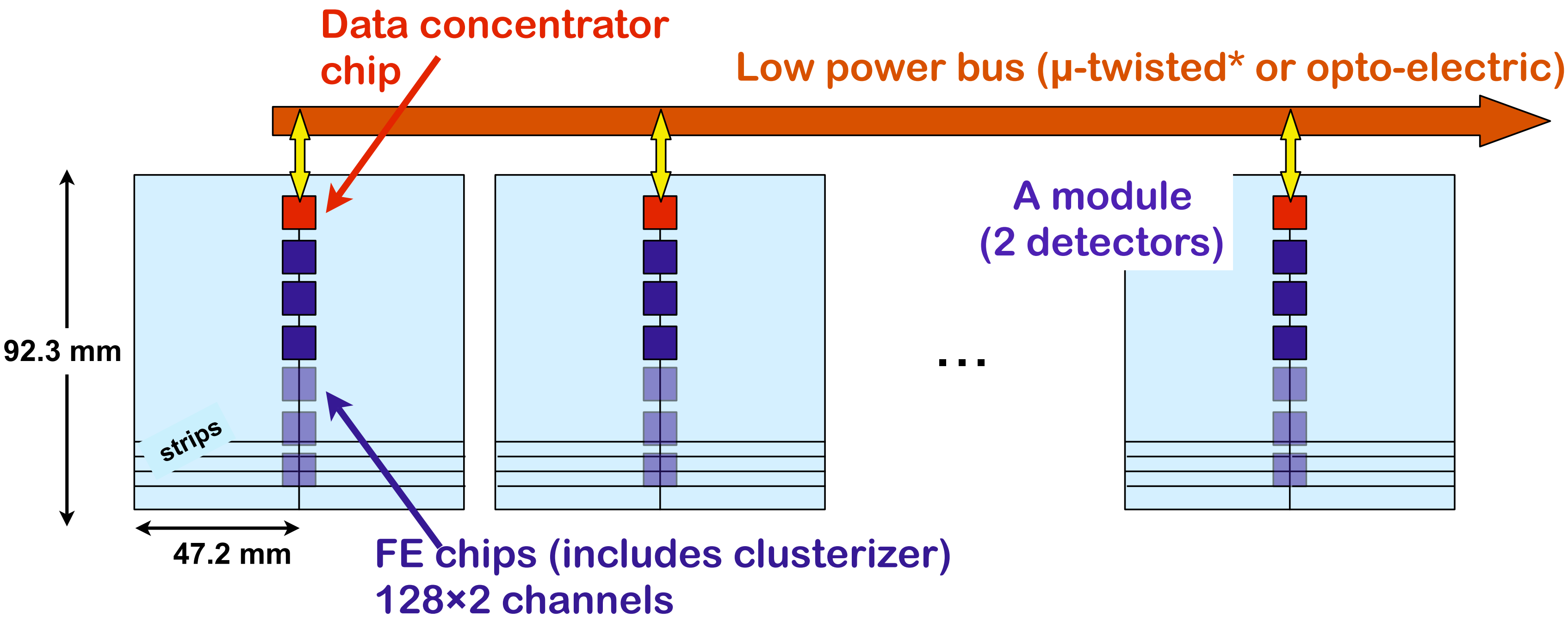


Pseudo-Track efficiency

- Fraction of muons with at least 3 out of 4 in the barrel trigger layers with a Cluster width <3

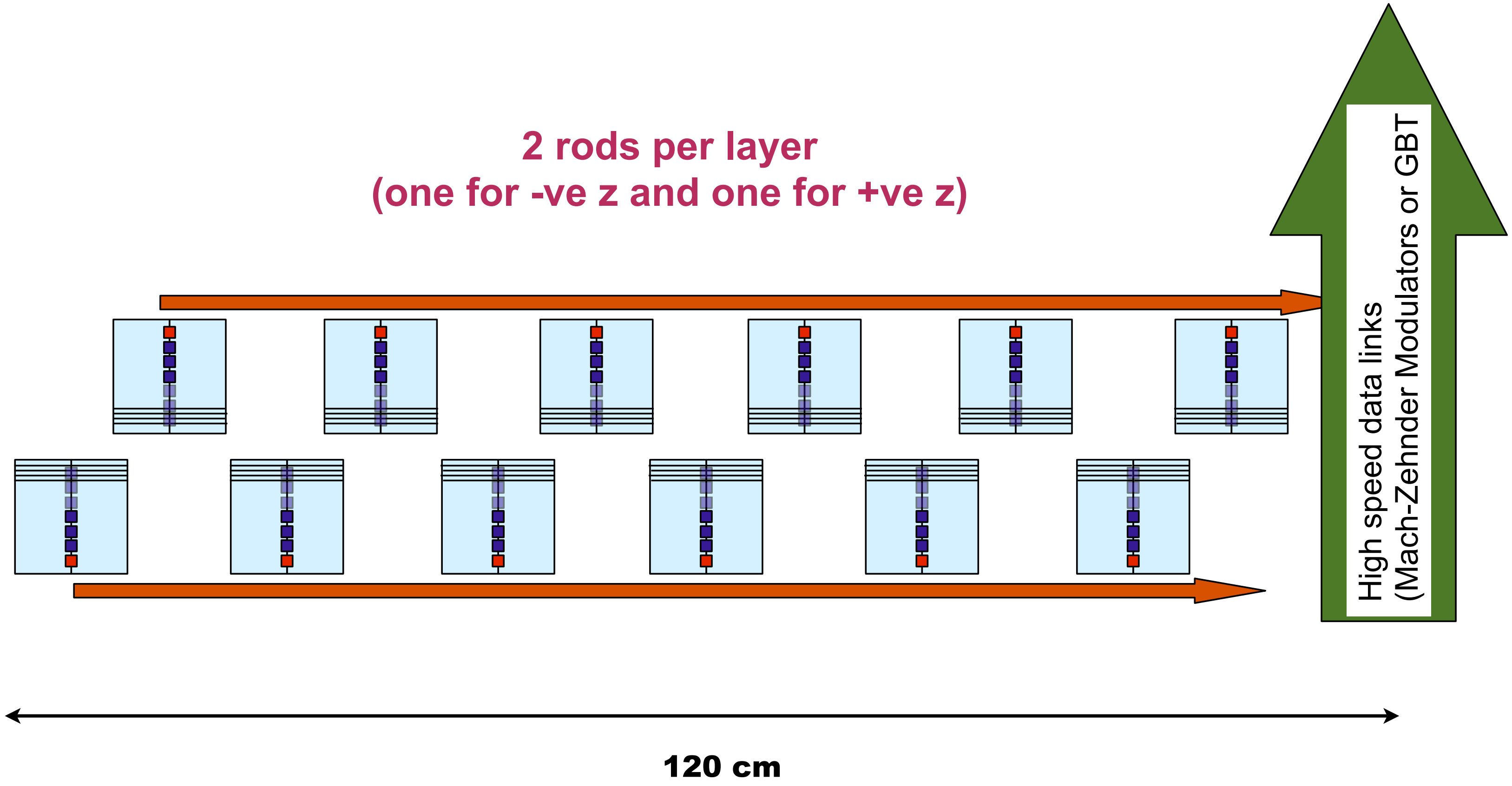


Conceptual readout block diagram



* see B. Meier at TWEPP 2009

A conceptual rod layout

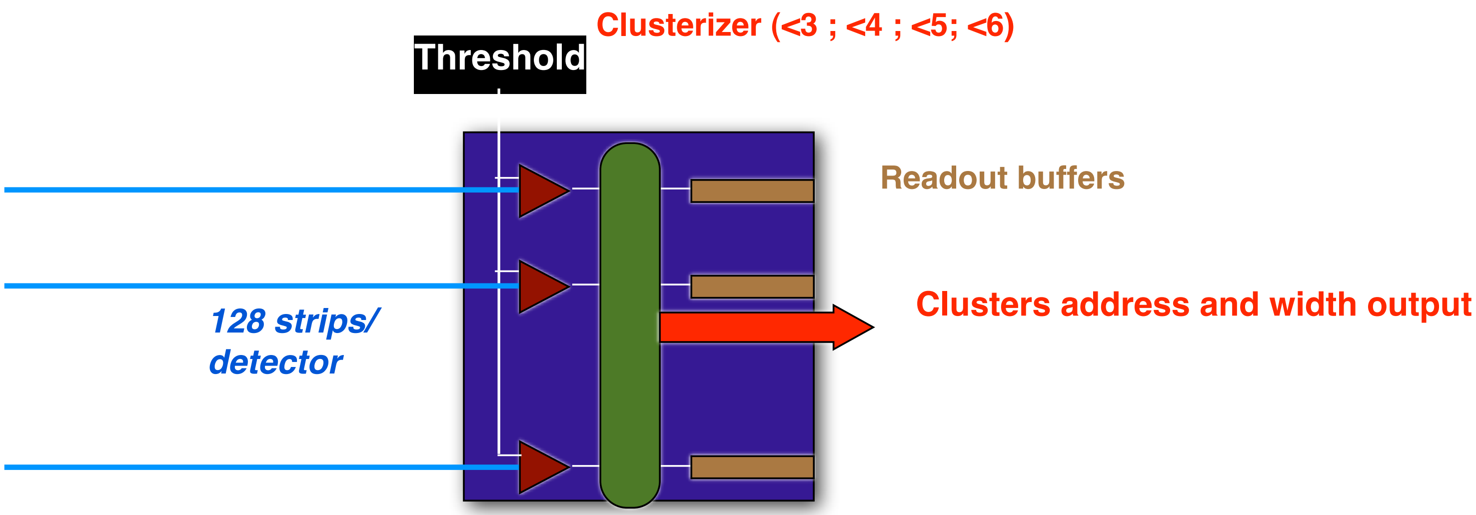


Two set of modules, internal and external to the same layer, staggered in z

Front End and clusterizer

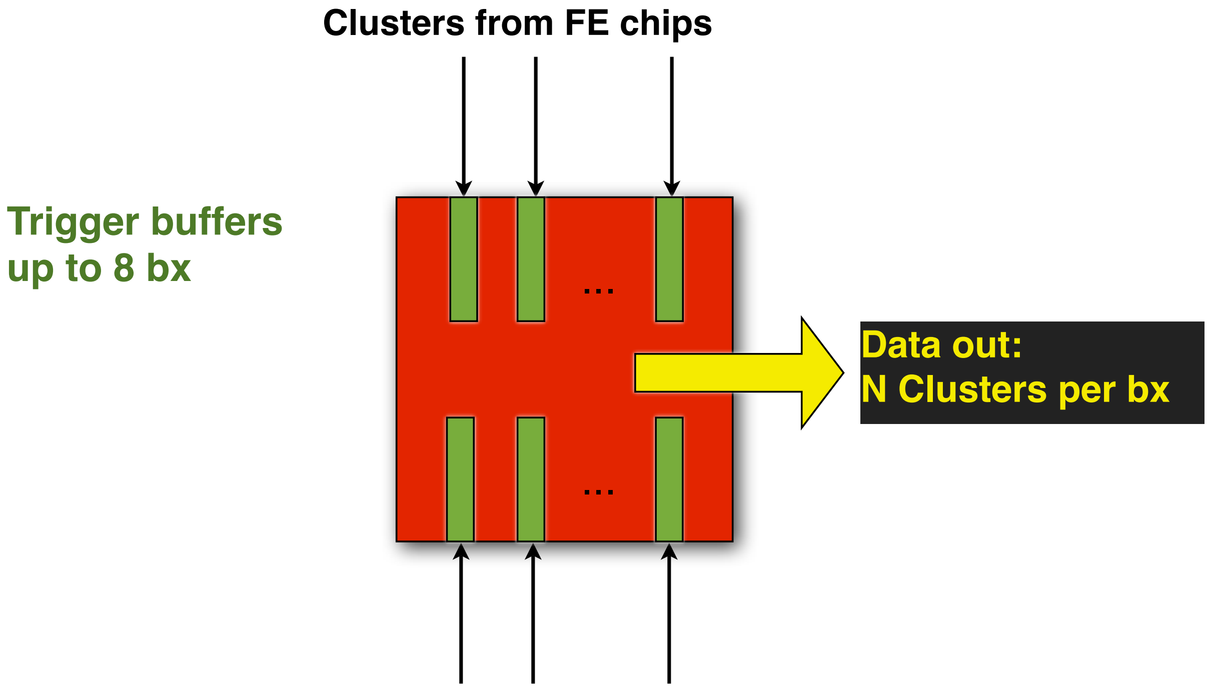
The FE is organized schematically as follows: it receives the input from 128 strips and a threshold is set to each comparator per each strip. It is assumed only one is needed. A width size selector receives in input the settings to select clusters whose width is smaller than a certain value (for instance <3 strips) among all the channels and outputs the clusters found together with their address and width.

The cluster width selector (<u>configurable</u>) also allows to work at different rate conditions (namely at lower luminosities).



Data concentrator chip

- **Clusters are routed from each FE to a data concentrator, in parallel.**
- **The data concentrator chip holds the clusters into buffers, to allow for the driver to pilot the data out of the module. Depending on the data rate it could also absorb local fluctuations, if the chip frequency is too slow. The length of such buffers will set the size of the chip and its final inefficiency. Given the above data rates, 8 bunch crossings will be sufficient**



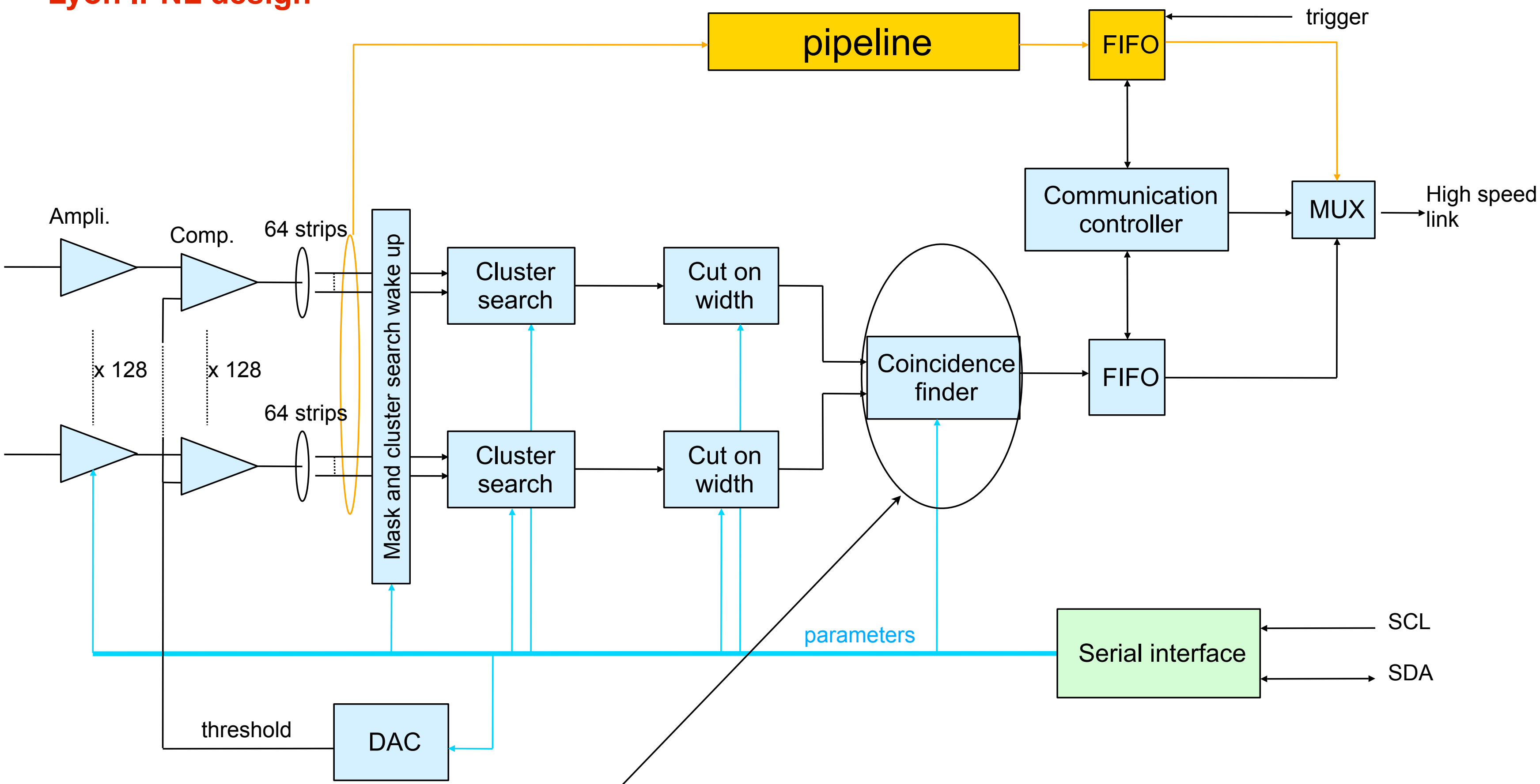
Data encoding*

- Estimate of the number of bits needed to encode the address
  - At the level of a module
  - 5 bits (Header) +[4 bits (cluster address) + 5 bits (chip ID)] x N + 3 bits (time stamp) + 2 bits (Trailer) = (10+ 9 N) bits
- At the level of rod need to add the module ID number: (15+9 N) bits

*see G. Magazzù talk

Front End ASIC architecture

Lyon IPNL design



Suitable to implement correlation in a "stacked" module

Main parts and plan

Cluster search logic

- Algorithm based on Look-up table (LUT) applied on 4 strips, that is then instantiated 32 times to perform the cluster search on 128 strips in one clock period.
- A second stage collects clusters information from all LUTs to compute the final data taking into account LUTs edges

Status

- VHDL design is done, now working on the synthesis.
- The goal is to submit before this summer (in June 2010) in a 0.13µm IBM technology.

A geometry for high efficiency

4 layer in trigger (L1/L2/L3/L4)

thresholds optimized for 96% hit efficiency for muons at pT>5 GeV/c ~ 99% of tracks with >=3 hits out of 4 layers

Layer radius (cm)	50	70	90	110
pitch (μm)	60	60	90	90
Total No. Strips/layer (Million)	3.1	3.5	3.2	3.6
Clusterizer S/N threshold	3	3	3	3
Cluster Rejection factor	4	4	2.9	2.7
Strip Rejection factor	11.6	12.6	6.8	6.0
Cluster Bandwidth (KHz/cm^2) [after cut]	1000	504	420	263
Cluster Bandwidth/module (Mbps)	983	595	529	406
Cluster Bandwidth/rod (Gbps)	13	8	10	7

A geometry optimized on lower bandwidth but with lower efficiency

Thresholds adjusted to 85% hit efficiency for muons with Pt>5GeV/c ~ 99% of tracks with >=2 hits out of 4 layers

(gain in bandwidth is small, but shows flexibility to adjust according to experimental conditions, to be completed by a S/N study)

Layer radius (cm)	50	70	90	110
pitch (μm)	60	60	90	90
Total No. Strips/layer (Million)	3.1	3.5	3.2	3.6
Clusterizer S/N threshold	2.7	2.7	2.5	2.5
Cluster Rejection factor	4.5	4.5	3.1	2.9
Strip Rejection factor	14	15	8	7
Cluster Bandwidth (KHz/cm^2) [after cut]	820	430	360	230
Cluster Bandwidth/module (Mbps)	842	537	482	380
Cluster Bandwidth/rod (Gbps)	11	8	9	7

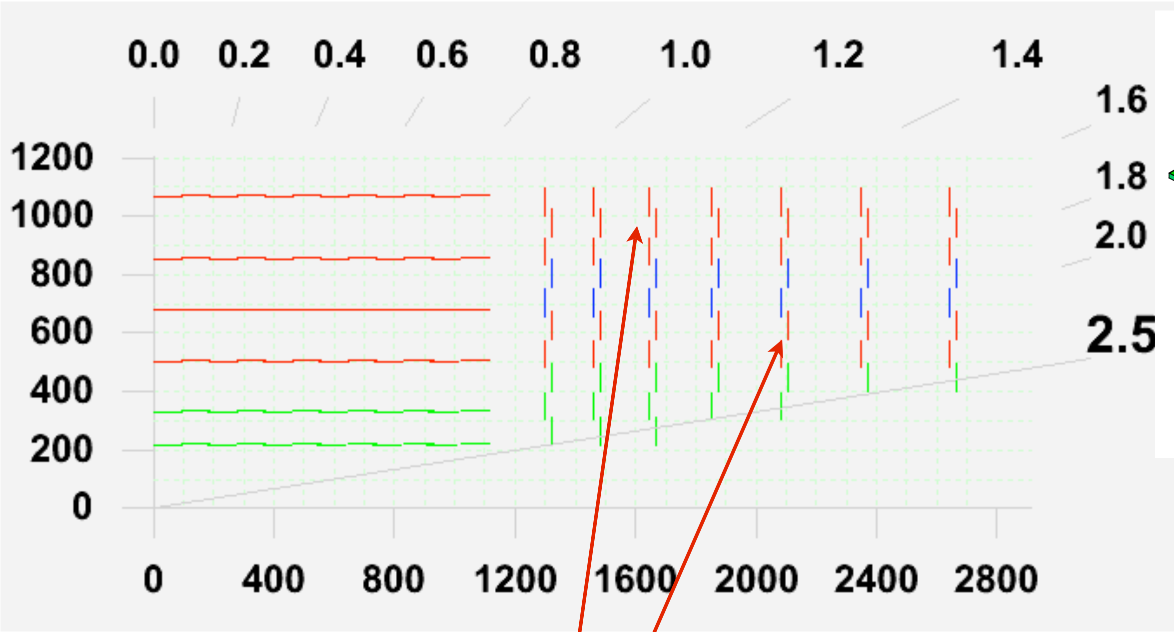
Estimate of the power - Barrel

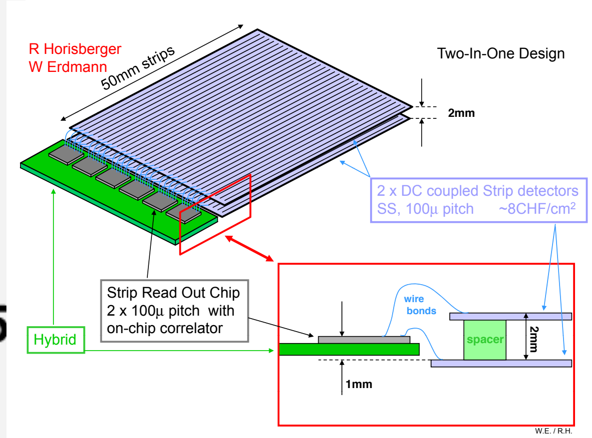
- We have made the following assumptions - 20 MHz LHC:
  a)**0.6 mW/strip in the Front End chip (0.50 mW/strip M. Raymond TWEPP 08 + 0.10 mW/strip due to clusterizer]**
  b)**20 pJ/bit per link and consumption weighted with average load. (conservatively a factor 2 larger than the estimate by B. Meier, TWEPP 08)**
  c)**power for Data Concentrator chip 100 mW - estimate**
  d)**external links two different solutions investigated:**
    i. **Standard GBT 5 Gbps (2.5 Gbps useful) 3 W power consumption:** 7 per rod at R<90 cm and 3 per rod for R>90 cm
    ii. **MZM (0.5 W) + data serializer (3W) - 15-20 Gbps - 3.5 W power consumption:** 1 per rod

Radius (cm)	Pitch (um)	No. detectors	No. strips (Million)	Power for Front End + clusterizer (kW)	Power for Data concentrator (kW)	Power for internal links (kW)	Power for external links - GBT (kW)	Power for external links - MZM (kW)
50	60	2016	3.097	1.86	0.20	0.02	1.76	0.29
70	60	2304	3.539	2.12	0.23	0.02	2.02	0.34
90	90	3168	3.244	1.95	0.32	0.02	2.77	0.46
110	90	3552	3.637	2.18	0.36	0.02	3.11	0.52
		11040	13.517	8.11	1.10	0.08	9.66	1.61

Configuration with 4 layers	Power (kW)
FE+DC+links+ GBT+20%	23
FE+DC+links+ MZM+20%	13

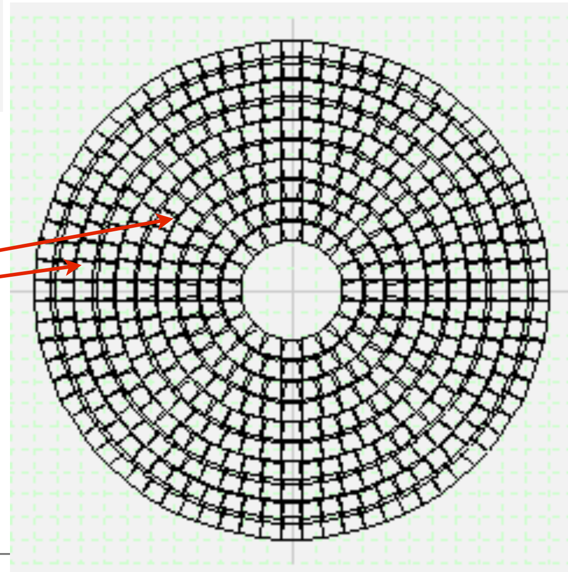
Endcap Geometry (fast simulation)





47 µm

Trigger rings



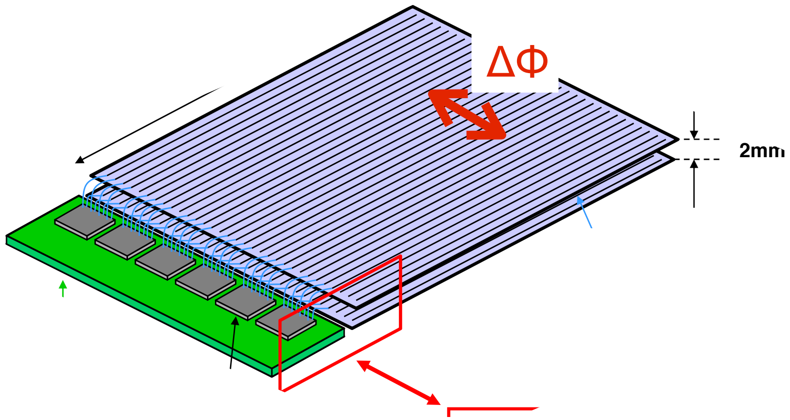
Modules and trigger variables

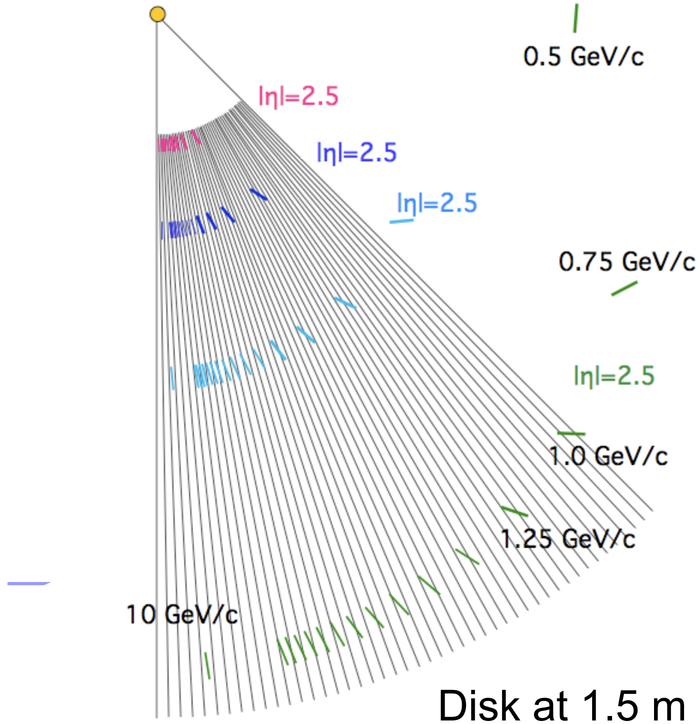
Geometries for endcap modules

- Rings at Radius<74 cm: Strips pitch 50µm and length 22 mm.
- Rings at Radius>74 cm: Strips pitch 100µm and length 44 mm.

Basic formula (see G. Parrini's talk)

$$\Delta\phi = \frac{0.3.r_{hit}.B.\Delta z}{2.p_T.z_{disk}}$$

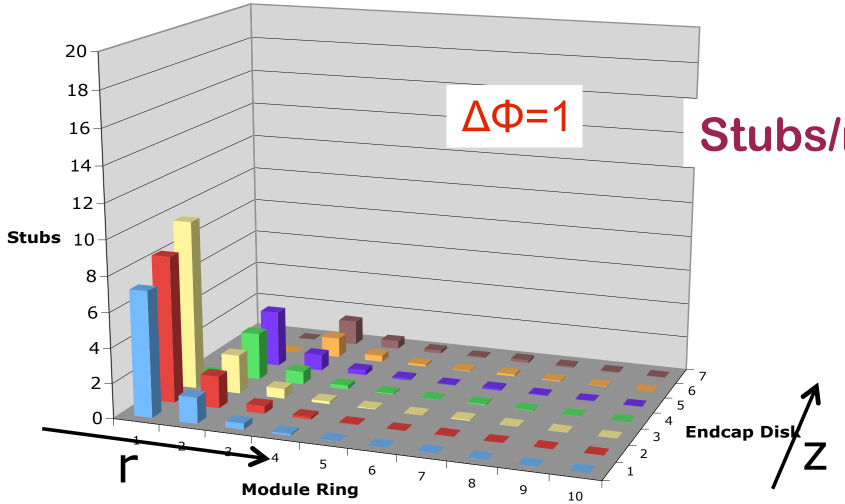


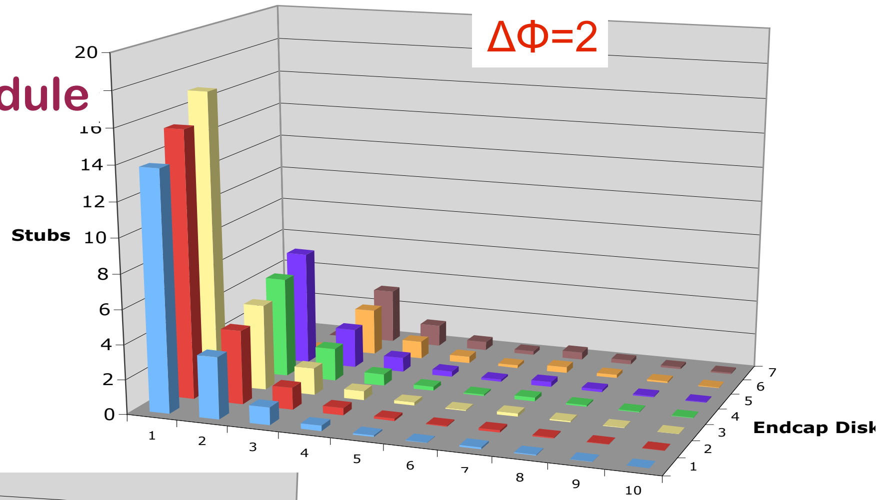


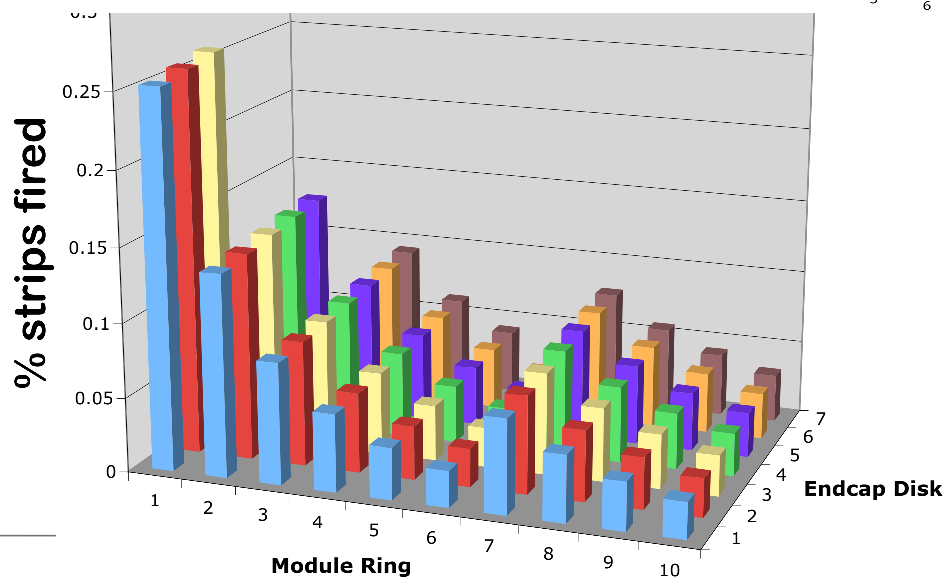
Strip doublet detector type: see A. Messineo's talk

No. of stubs and %strips at 200 PU

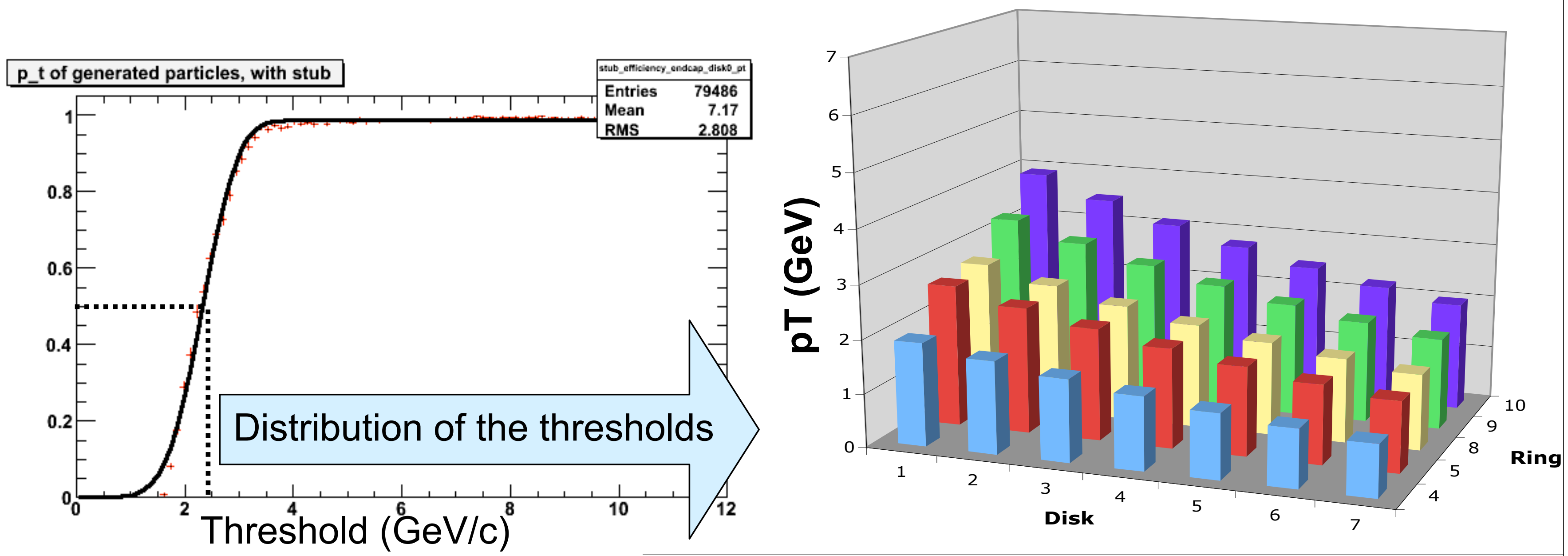
Stubs/module







R. Frazier

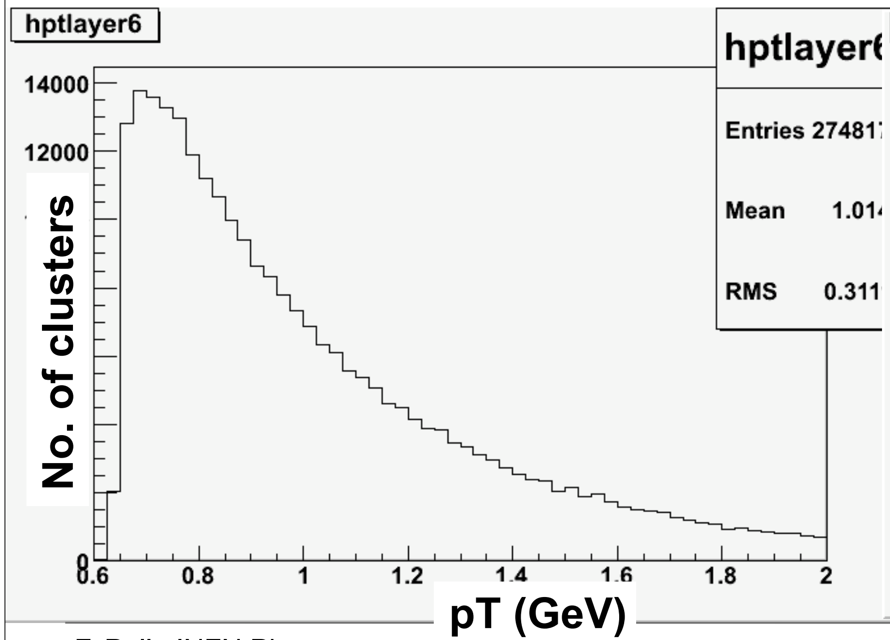


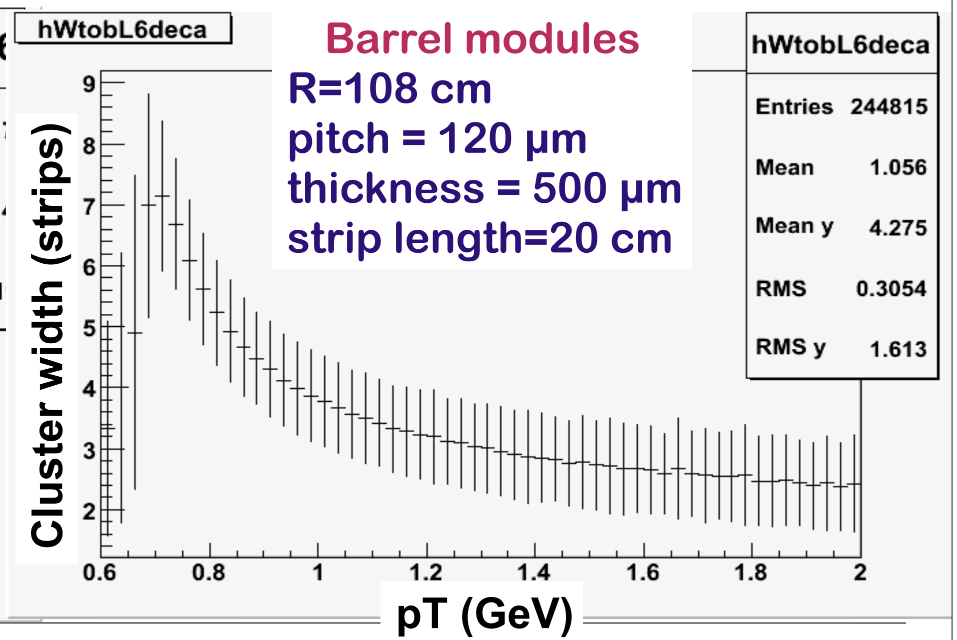
- **Quite promising results for rings>40 cm**
  - low occupancy
  - small number of stubs/module
  - relatively small pT threshold

R. Frazier

Validation of the method with CMS

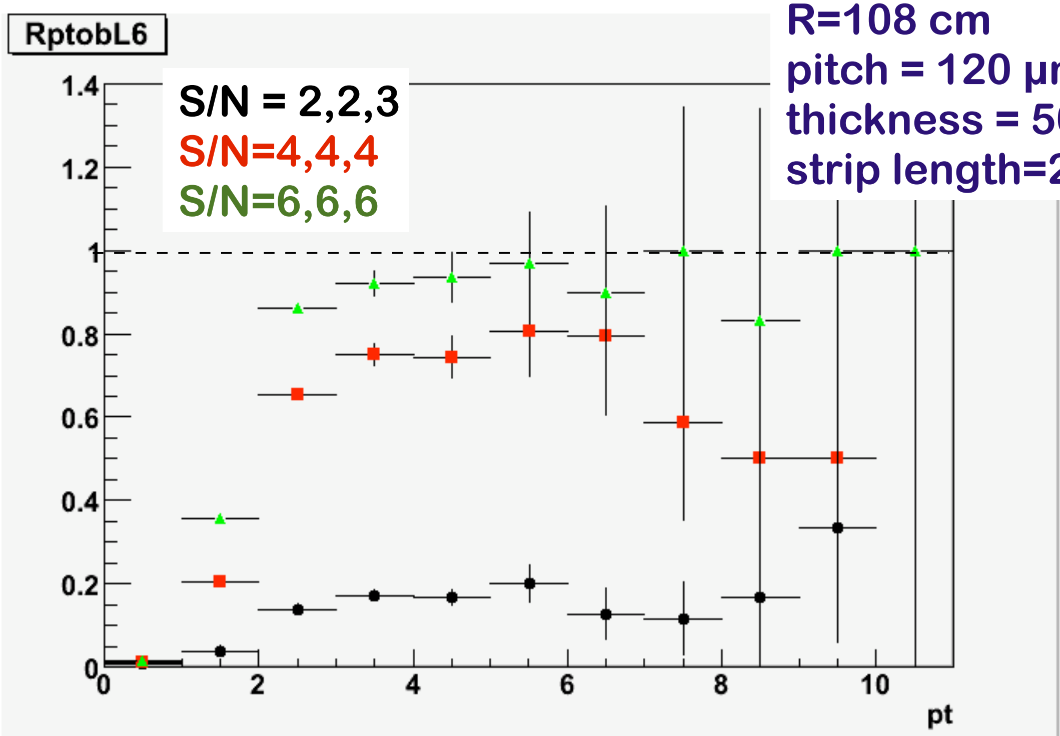
- Use 900 GeV LHC collision data using the current CMS Tracker (peak mode)
  - Reconstruct all tracks in the events
  - For each track use the clusters belonging to it plot
    - The cluster distribution as a function of the track pT
    - The cluster width distribution as a function of the track pT





Cluster efficiency LHC data

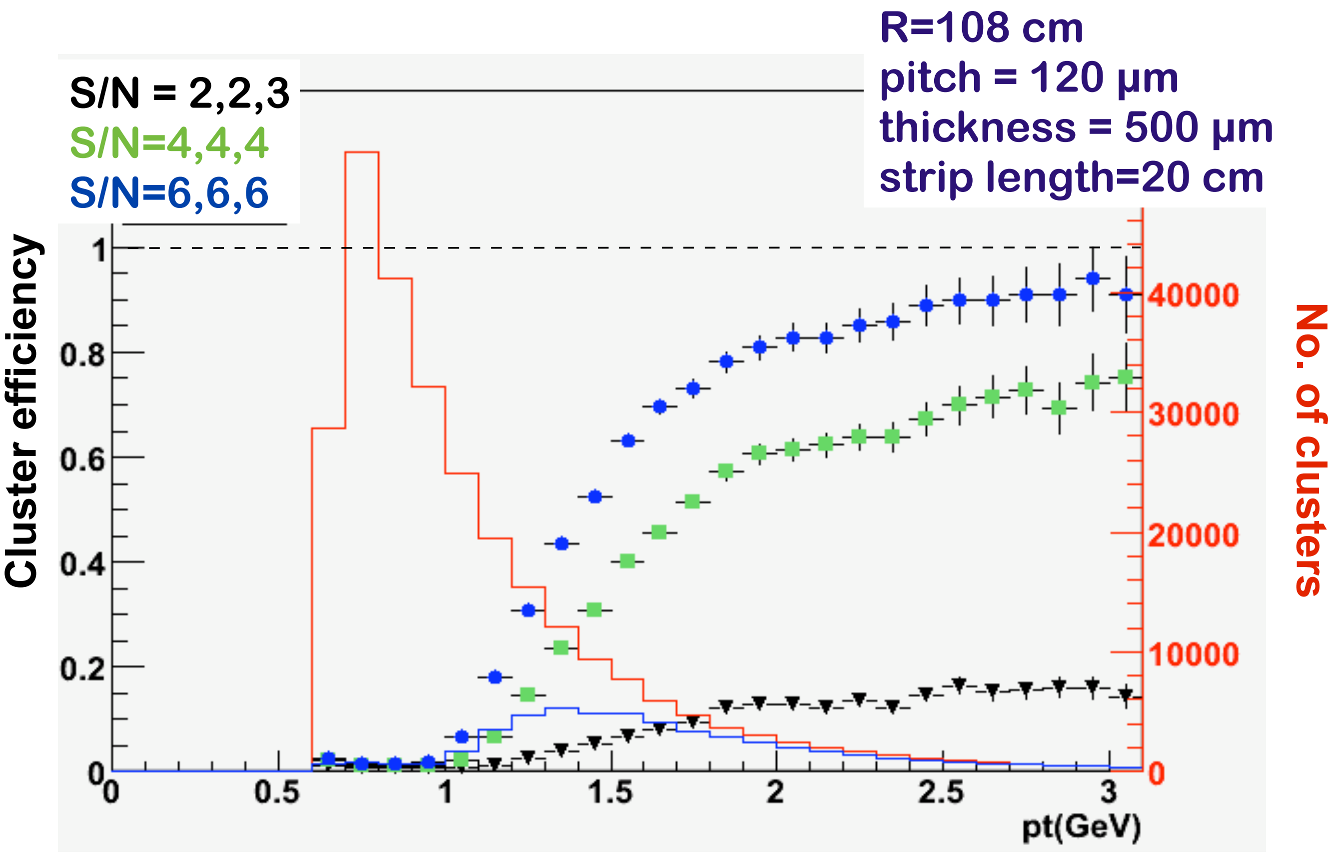
- **Cluster efficiency (for CW<3) as a function of the clusterizer thresholds**
  - **Number of clusters that survive the CW <3 cut per pT bin.**



R=108 cm
pitch = 120 μm
thickness = 500 μm
strip length=20 cm

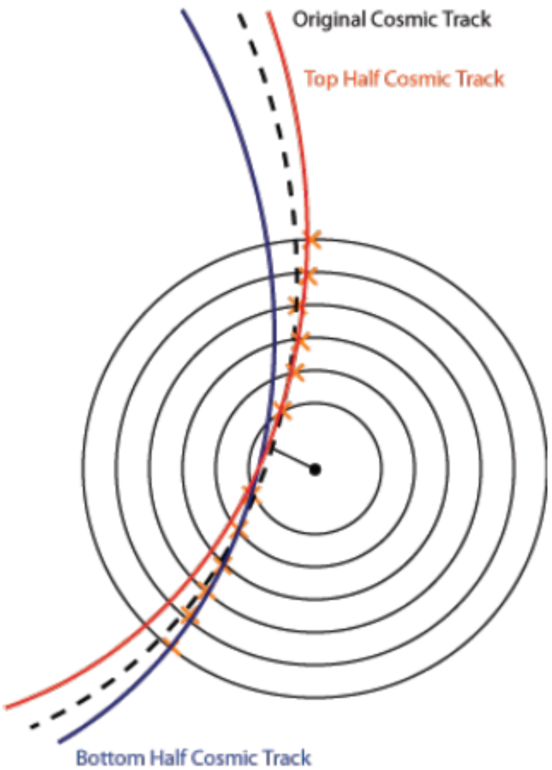
Cluster efficiency LHC data

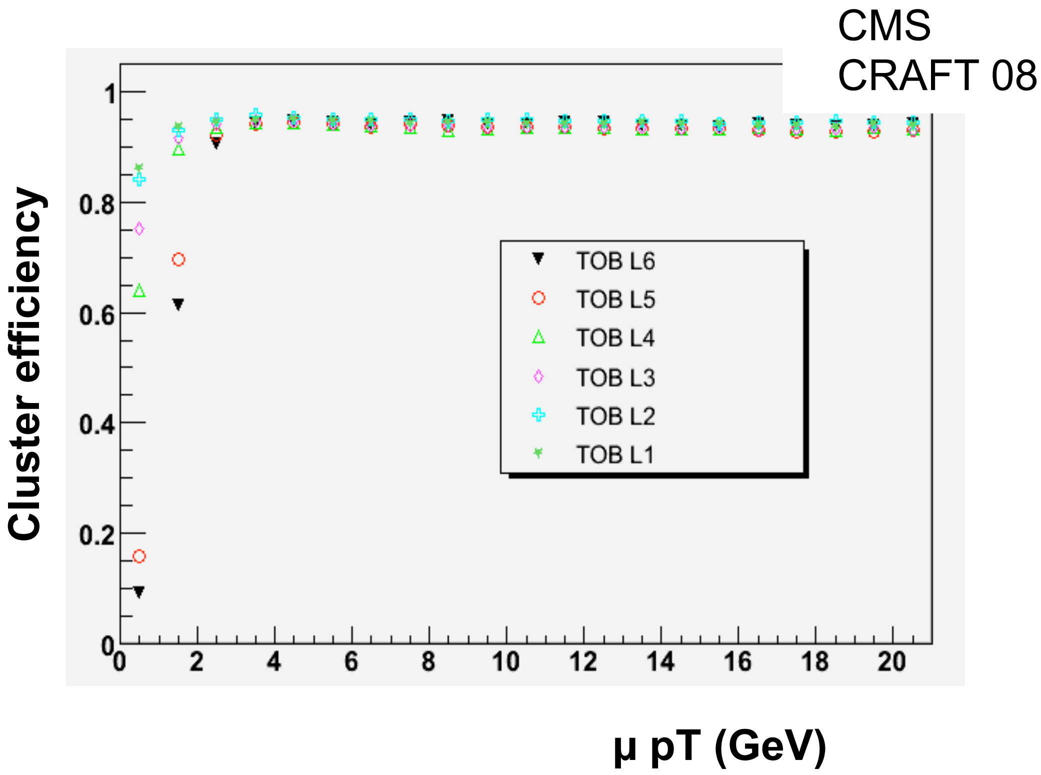
Fraction of clusters with CW <3 cut per pT bin.



Efficiency in cosmic muons

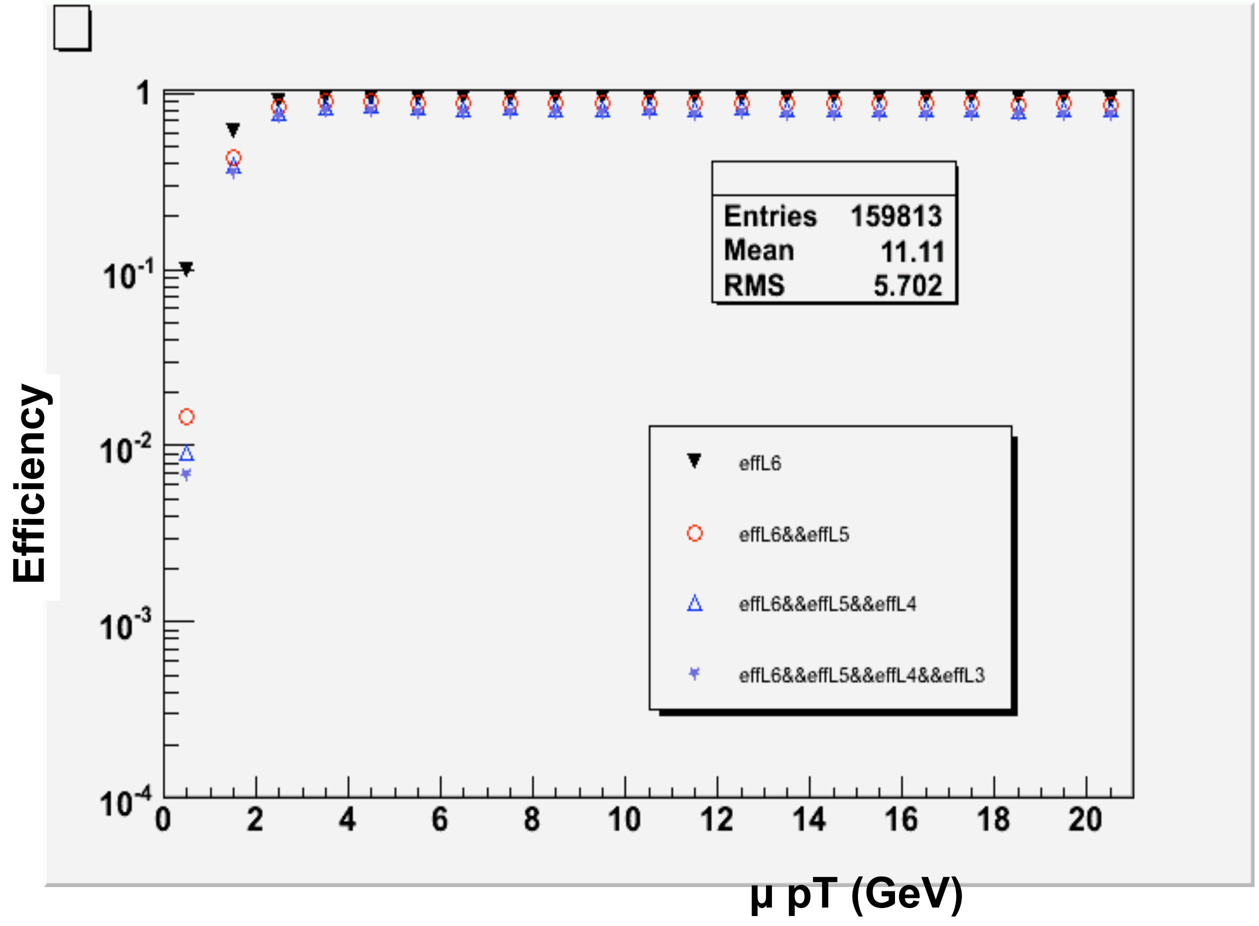
Study cluster efficiency (CW < 3)





“Tracking” efficiency with muons

Require muons in multiple layers

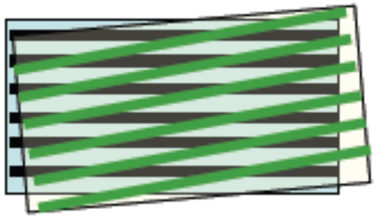


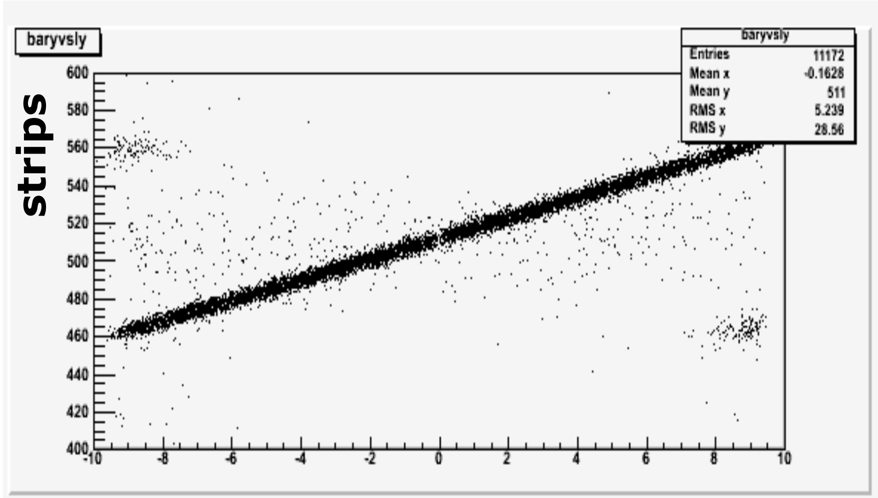
Mimicking strips doublets

Glued stereo modules

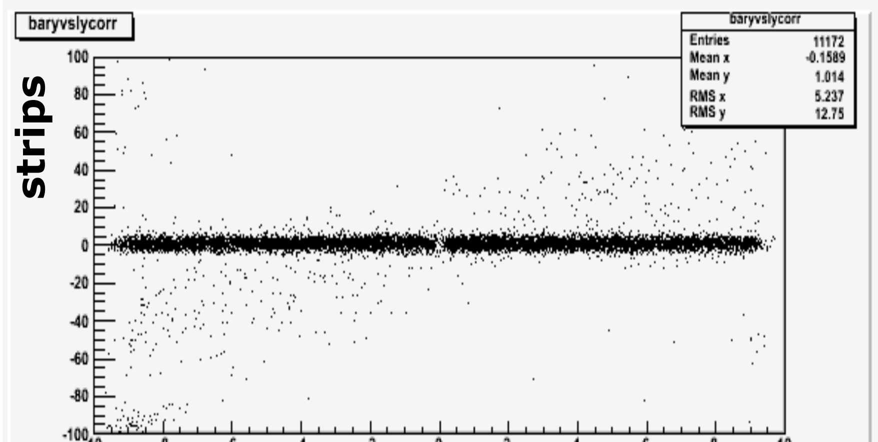
sensors separation ~ 2 mm

Stereo + Rphi modules





Stereo + Rphi modules **100 mrad rotation**

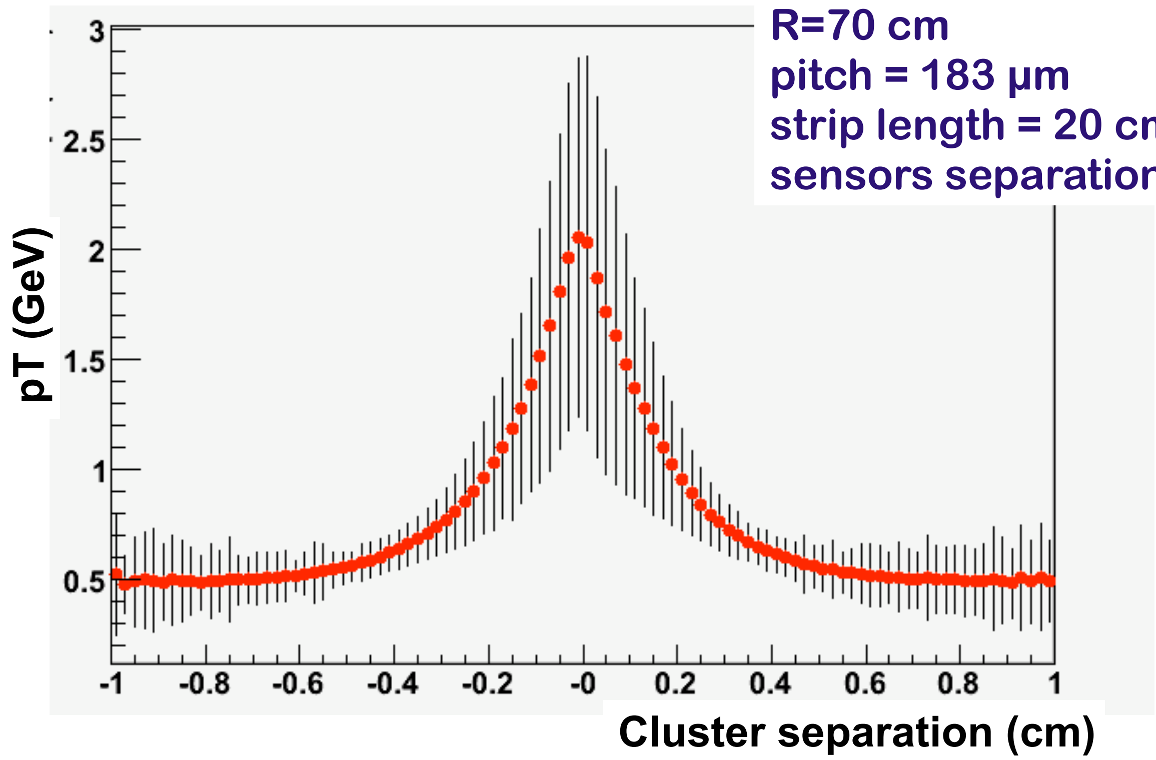


$$x_{ster} = 513 - x'_{ster} + 0.1/0.0183\ y$$

Strip Doublet with LHC data

- Separation between two clusters in back-to-back sensors as a function of track pT

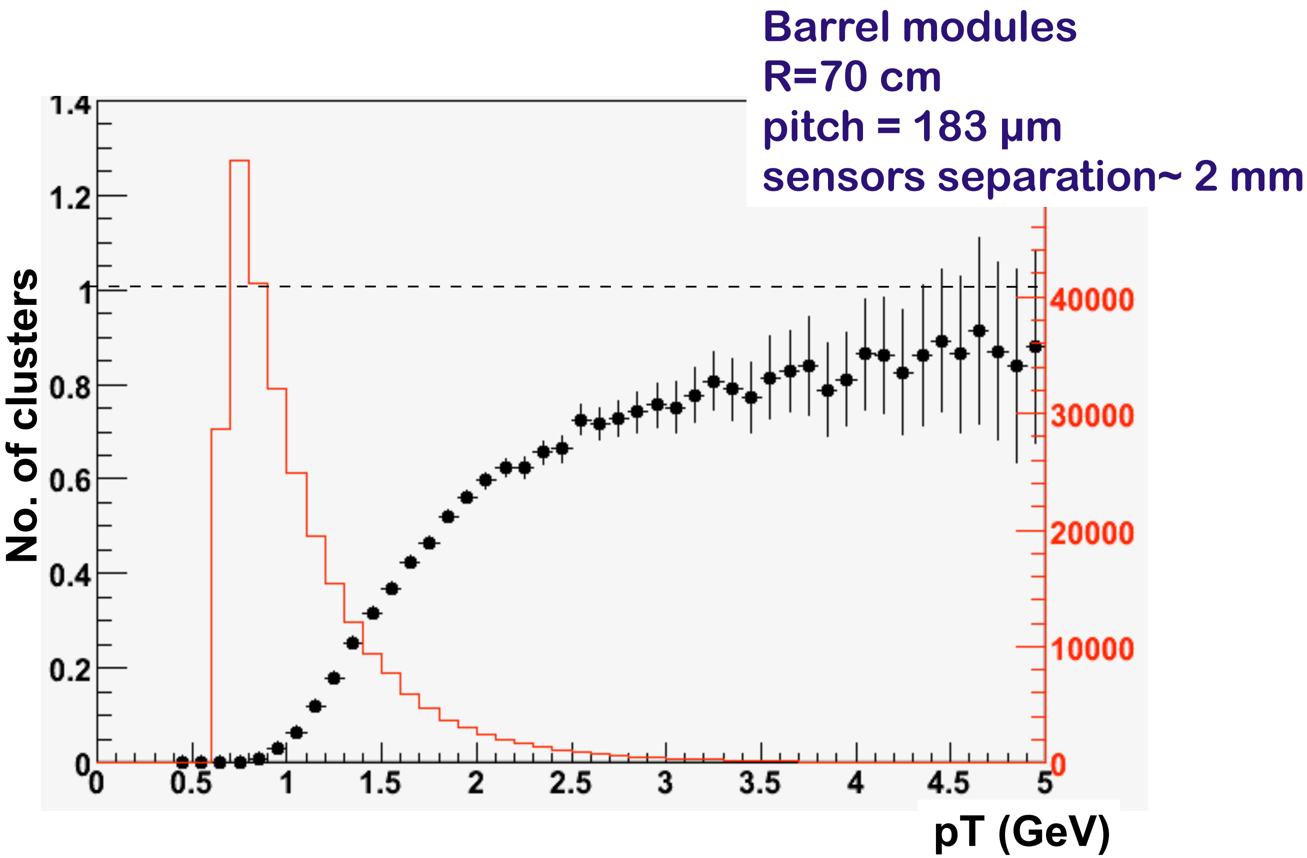
Barrel modules
R=70 cm
pitch = 183 μm
strip length = 20 cm
sensors separation~ 2 mm



Efficiency of the doublet with LHC data

Cluster efficiency as a function of pT

- Two clusters in separate sensors and cluster distance < 1 mm



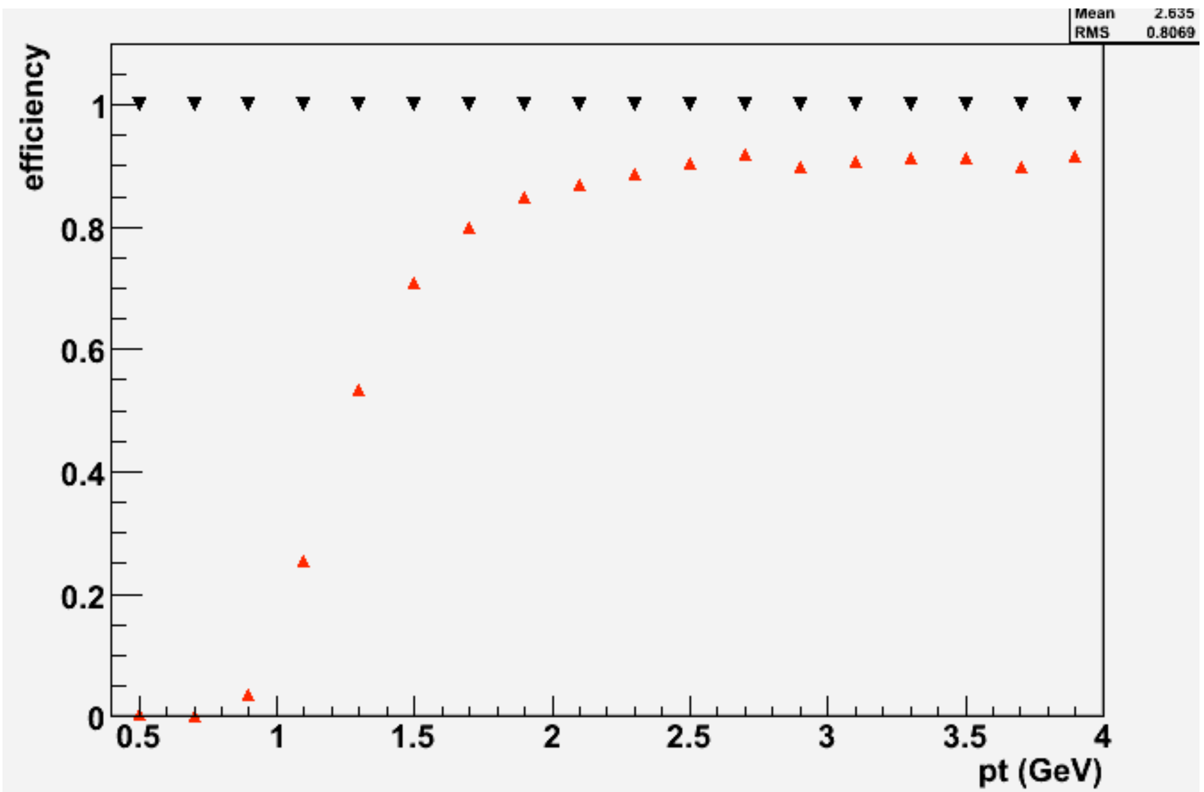
Conclusions

- A concept for tracker with trigger capabilities has been shown to be feasible:
  - Keeps the data rate manageable using a cluster width data reduction on chip
    - Up to 20:1 suppression factor [from strips to small clusters]
    - Highest bandwidth 10 Mbps cm^{-2} at 50 cm radius
    - Can use “today” technology
  - Multi-layer approach required for efficiency and redundancy
    - Use external intelligence based on addressable memories
  - Endcap region addressable using stacked strips sensors
- Validation of the concept ongoing with LHC collision data
  - Tune MC simulations and data rates
  - Allows studying high multiplicity jets
- Subsequent talks on on-going R&D
  - Messineo, Janner, Heintz, Magazzù

Backup

Pseudo-Track efficiency LHC 900 GeV Minbias

- Fraction of tracks with at least 3 out of 4 in the barrel trigger layers with a Cluster width <3 in Minimum bias events at 900 GeV

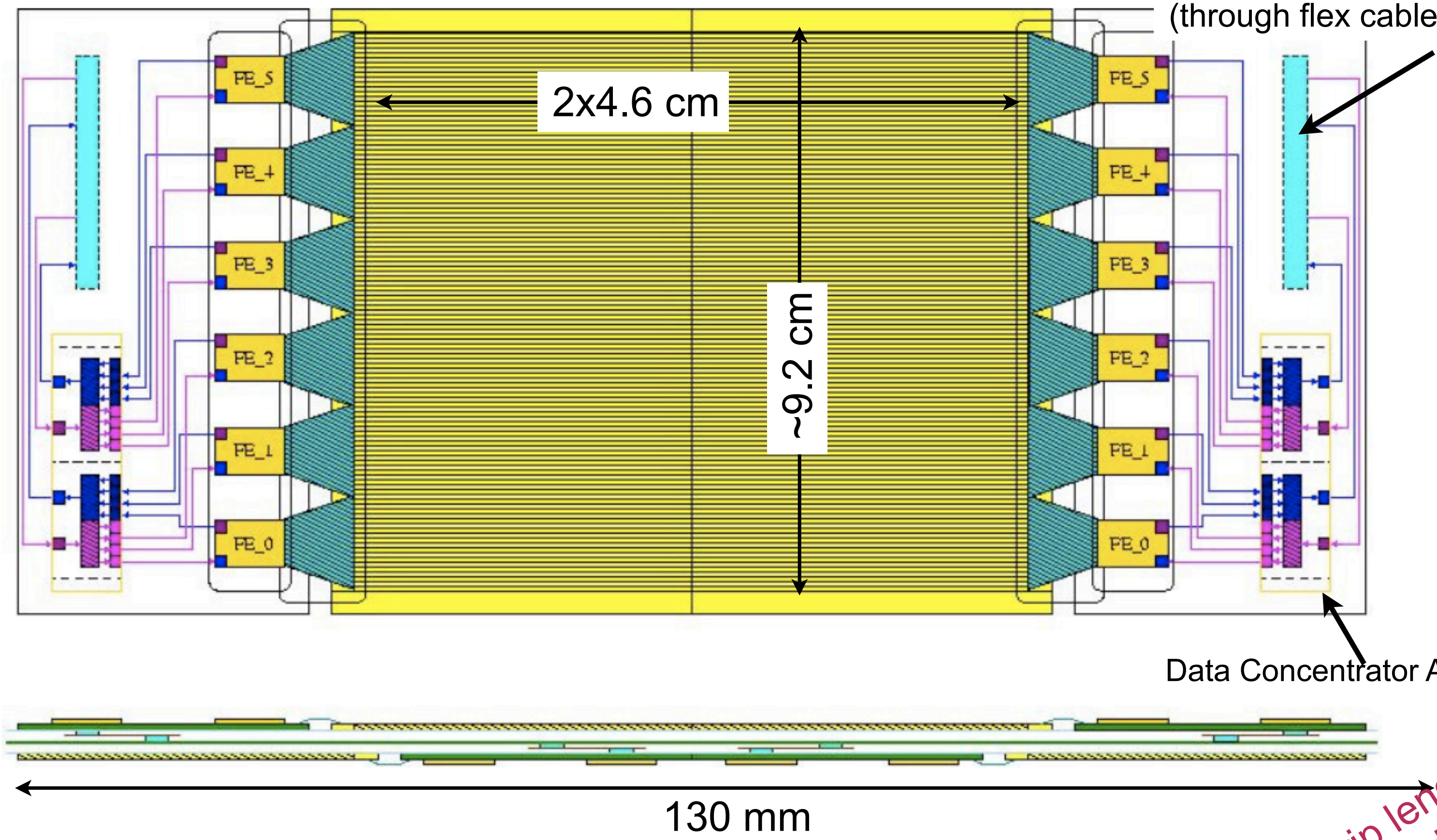


Trigger working model

- Subdivide the detector in several - O(50) - φ sectors
  - Keep data volume to be transferred limited in each sector
  - Introduce an intrinsic pT cut
- Data reduction and transfer
  - Reduce the data rate for Trigger purpose on detector
  - Use high speed data links O(20 Gbps) to limit the no. of links to manageable level
- Process the data off detector
  - majority logic: for instance at least 3 layers out of 4 in each trigger sector
  - compute pT and impact point
  - match with muons and calorimeters
- Output of the Trigger
  - Tracks reconstructed above a given pT sector by sector

A possible module layout (outer layers)

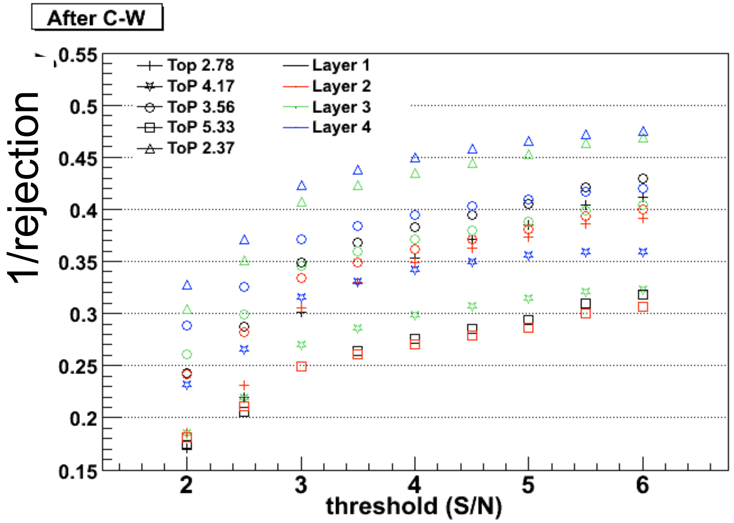
Connector to Mother Board (through flex cable)

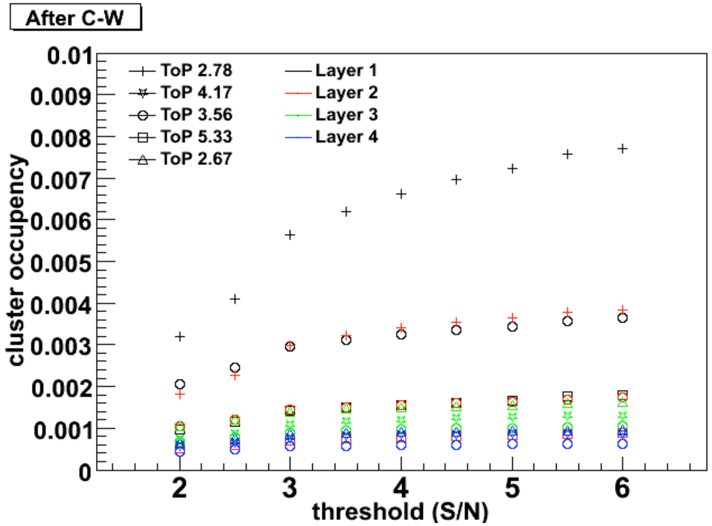


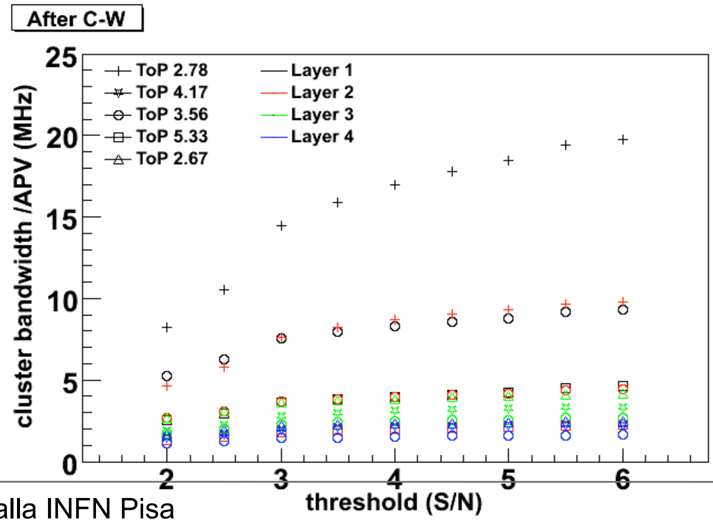
120 µm pitch
128 strips/FE
300 µm thick

Pitch and strip length not yet optimized

400 overlapped minimum bias







Strong dependence
on layer parameters

Reasonable
range

A geometry optimized on larger bandwidth but lower number of channels

4 layers in trigger (L1/L2/L3/L4)

Thresholds and choice of layers adjusted to ~ 3.5 MHz per APV and 96% hit efficiency for muons with Pt>5GeV/c ~ 99% of tracks with >=3 hits out of 4 layers

(last layer could possibly have only 4 APVs)

Alternative 3 layer in trigger (L2/L3/L4)

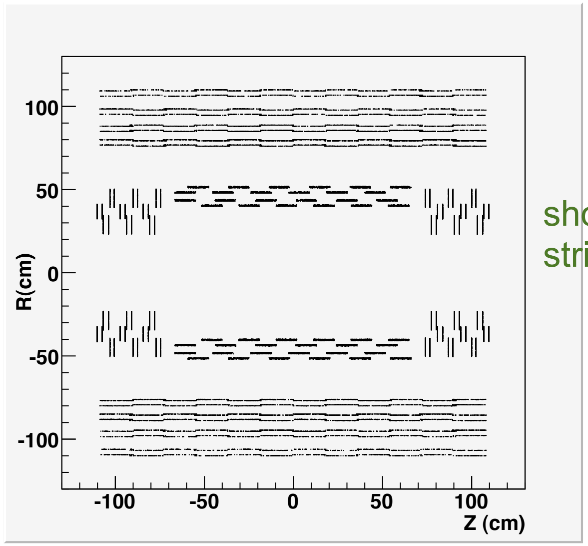
~100% of tracks with >=2 hits out of 3 layers (88.8% tracks with 3 hits, 11% with 2 hits)

Layer radius (cm)	50	70	90	110
pitch (μm)	60	90	120	120
Total No. Strips/layer (Million)	3.1	2.4	2.4	2.7
Strip S/N threshold	3	3	3	3
Cluster Rejection factor	4	3	2.4	2.4
Strip Rejection factor	11.6	7	10	8
Cluster Bandwidth (KHz/cm^2) [after cut]	1000	670	380	270
Cluster Bandwidth/module (Mbps)	983	987	597	482
Cluster Bandwidth/rod (Gbps)	13	13	11	9

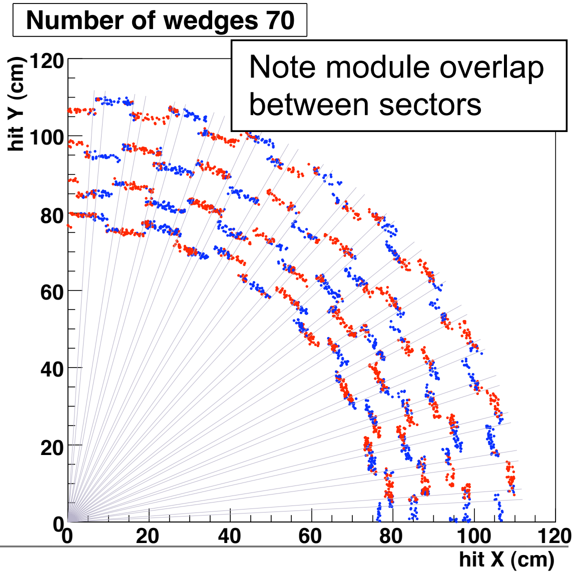
Full GEANT4 simulation

- **Modified Strawman A*:**
  - 4 pixel layers (4, 7, 11 and 18 cm)
  - 2 silicon strip layers at 40 and 50 cm
  - Trigger layers located at: 78, 87, 97, 108 cm (current last 4 TOB)
    - 290 µm active thickness, 91.5 µm pitch (97 and 108 cm layers) and 122 µm pitch (78 and 87 cm layers), n-type bulk, 4.65 cm strips length, AC coupling, 3% inter-strip couplings
      - ➨ no Lorentz angle compensation
      - ➨ 12192 mini-modules, 7.96 M channels

*Dimensions constrained by the Strawman A simulation approach



showing only strip modules

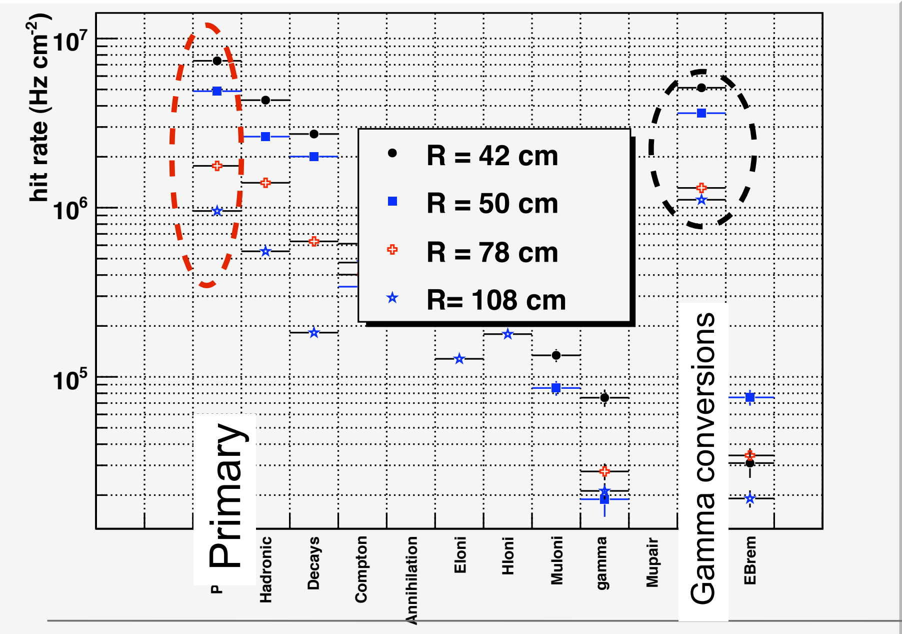


Data rate in Barrel - I

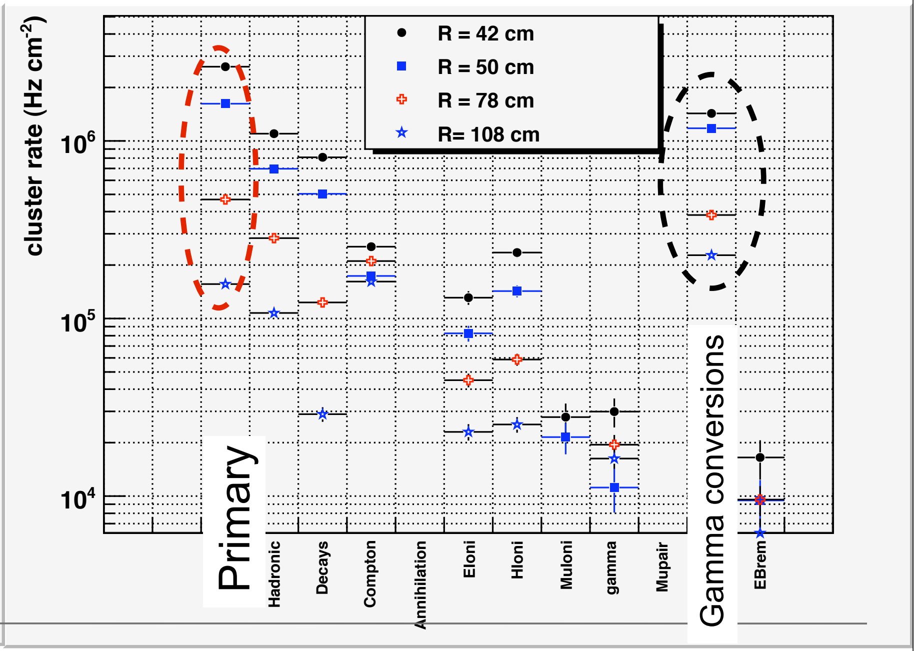
- Huge data rate (at 10^{35} cm^{-2} s^{-1})
  - Use clusters instead of hits to first decrease the rate
    - R=42 cm: clusters (hits) ~7 (22) MHz cm^{-2}
    - R=78 cm: clusters (hits) ~1.6 (6) MHz cm^{-2}
    - R=108 cm: clusters (hits) ~0.7 (3.6) MHz cm^{-2}

    (Note: if no zero-suppression applied (DIGI) rates are a factor 10 larger)

HITS



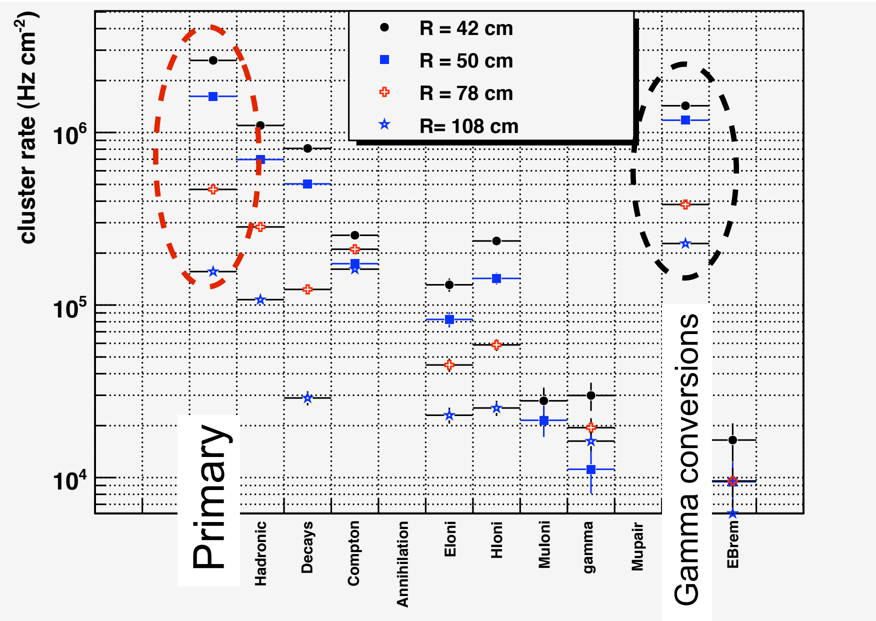
CLUSTERS



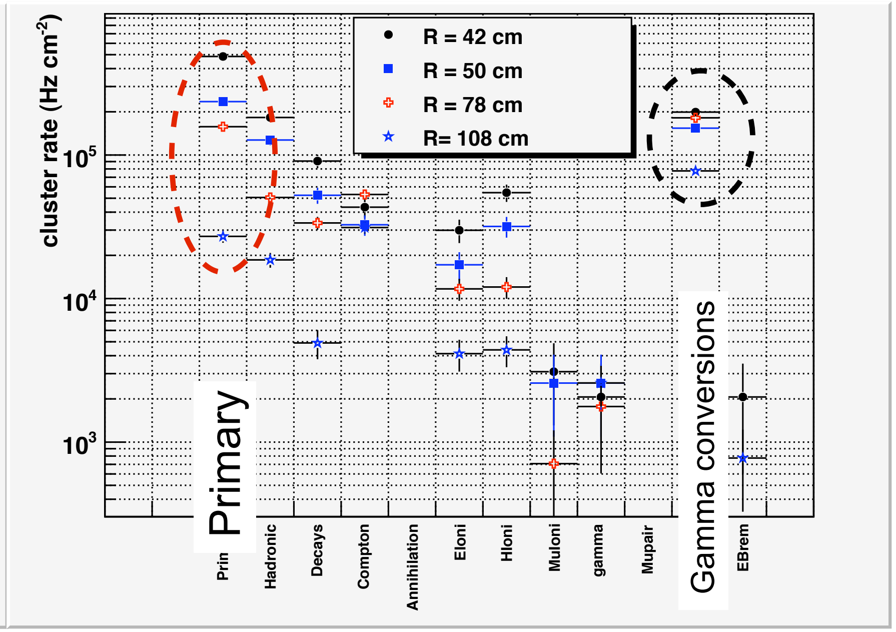
Data rate in Barrel- II

- **Large reduction in data rate expected:**
  - R=78 cm: 500 kHz cm^{-2} (it was 6 MHz cm^{-2} hit rate)
  - R=108 cm : 170 kHz cm^{-2} (it was 3.6 MHz cm^{-2} hit rate)

Cluster rate **before** CW reduction



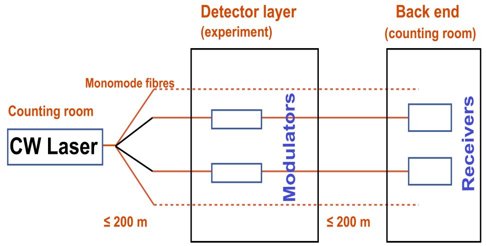
Cluster rate **after** CW reduction

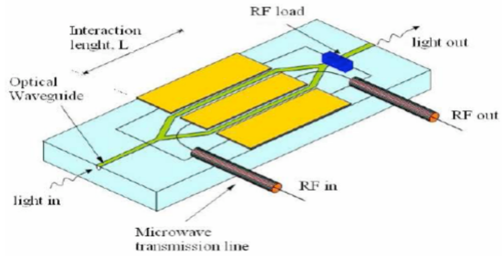


Fast Links

Telecommunication/IT standards

Put Laser power outside the detector and use modulators





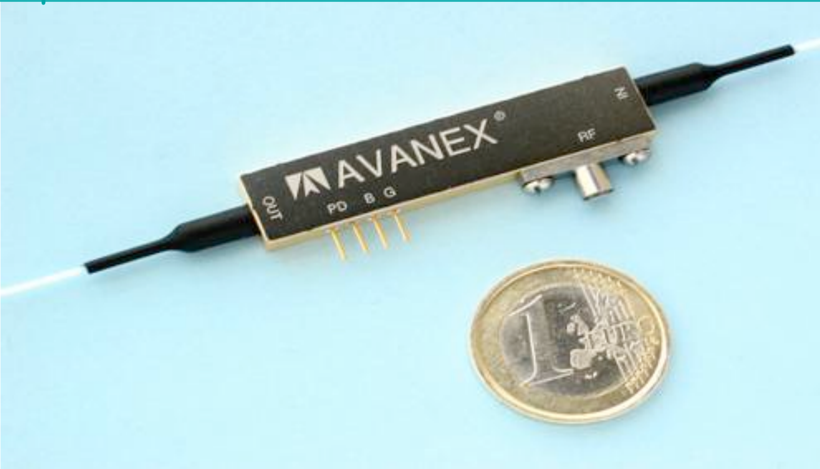
- Normally uses electro-optical modulators (reaching up to 40 Gbps)
- Need to be tested in high B field, low temperature and high fluence

Modulator	Vpi @ 10Gb/s	Dyn. Extinction Ratio (dB)	Modulation Power	Power dissipated: driver (Typ)	Packaged Dimensions (Typ)	Laser Source	Notes
LiNbO3 (Avanex Small Form Factor)[2]	5 V	13	250 mW	1-1.5 W[8,9]	81 mm x 9.3 mm x 5 mm	External	Vpi L =9V
LiNbO3 (Avanex Low Voltage)[3]	4 V	14	200 mW	~1 W[8,9]	98 mm x 9.3 mm x 5 mm	External	
LiNbO3 ridge[4]	3 V	> 10	200 mW	0.5-1 W[10]		External	Vpi L =7V (only R&D)
EAM (Bookham)[5]	2.7 V	11	200 mW	0.5-1 W[10]	60 mm x 13 mm x 5 mm	Internal (0.6 W cons.)	Rad Hard? High insertion loss (~7 dB)
EAM (OKI)[6]	2.5 V	9.5	200-300 mW	0.5-1 W[10]	25 mm x 13 mm x 6 mm	Internal (0.4 W cons.)	Rad Hard?
VCSEL (BeamExpress)[7]	2.5 V	>10	~30 mW	~200 mW	not std TBD	Direct modulation	Rad Hard?[11,12] Low temp?

standard

Some interesting products

http://www.avanex.com/Products/datasheets/Transmission/2613_PwrBitXS10-1700-2000.pdf

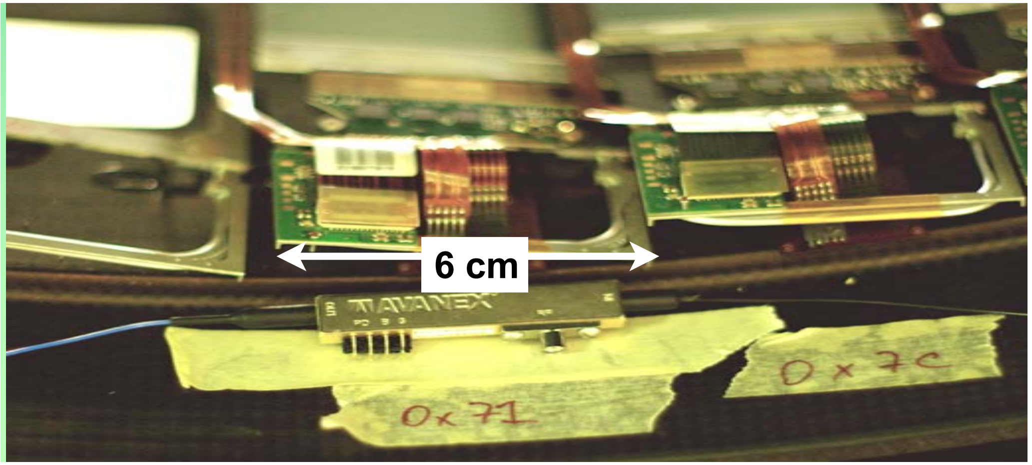


SPECIFICATIONS

Parameters		Units
Optical		
Operating Wavelengths Range	C- and L-Band	
Insertion Loss	4	dB
Extinction Ratio (DC), 0-Chirp Version	≥ 20	dB
Note: Prechirped Versions for 1700 ps/nm, 2000 ps/nm or Custom are Available on Request.		
Optical Return Loss (without connectors)	≥ 45	dB
Electrical		
S_{21} Electro Optic Bandwidth (-3 dBe)	12.5	GHz
S_{11} Electrical Return Loss	< - 10	dB
RF V_{π} Voltage (@ 1 kHz)	5.0	V
Bias V_{π} Voltage (@1 kHz)	6.9	V
Dynamic Extinction Ratio (0-chirp version)	13	dB
10.7 Gb/s PRBS Electrical Drive Voltage (V_{amp})	5.0	V

CONNECTOR AND FIBER SPECIFICATIONS

RF Input Port	GPO
Bias and VOA Connector	Solder pins
Input Fiber	Corning/Fujikura SM15P UV/UV400
Output Fiber	Corning SMF-28™ or single mode ITU-T G.652[1]

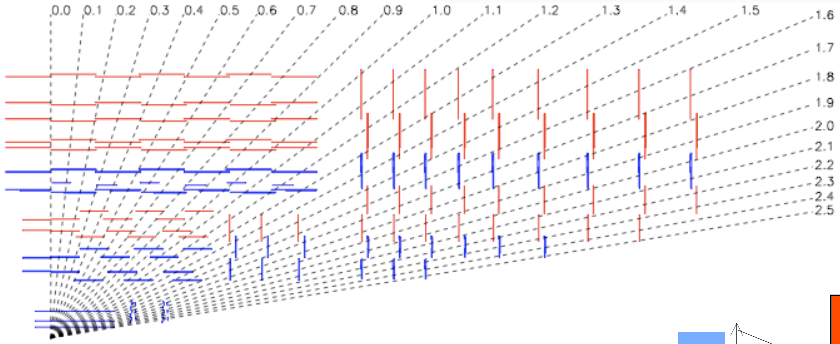


RD23 project legacy

- **RD23** project was mainly focussed on **analogue** data transmission. CMS data link upgrade is based on digital links. Analogue data transmission is much more sensitive to environmental effects, since these can lower/change the **linear response** of the system.
- **Radiation hardness** of lithium niobate is defined "**outstanding**" in the RD23 CERN-DRDC_93-35(1993) document.
- Lithium niobate modulators have not been chosen in the RD23 project not because of poor performance, but due to their **high cost** (decreased since that time) and excessive **device dimension** (CERN-DRDC-94-38). This can still be seen as an issue, but which **can be overcome taking into account the performance they can deliver**, still not reached by other devices.

http://documents.cern.ch/cgi-bin/setlink?base=generic&categ=public&id=cer-0212283
http://documents.cern.ch/cgi-bin/setlink?base=generic&categ=public&id=cer-0215602

The CMS Silicon Tracker



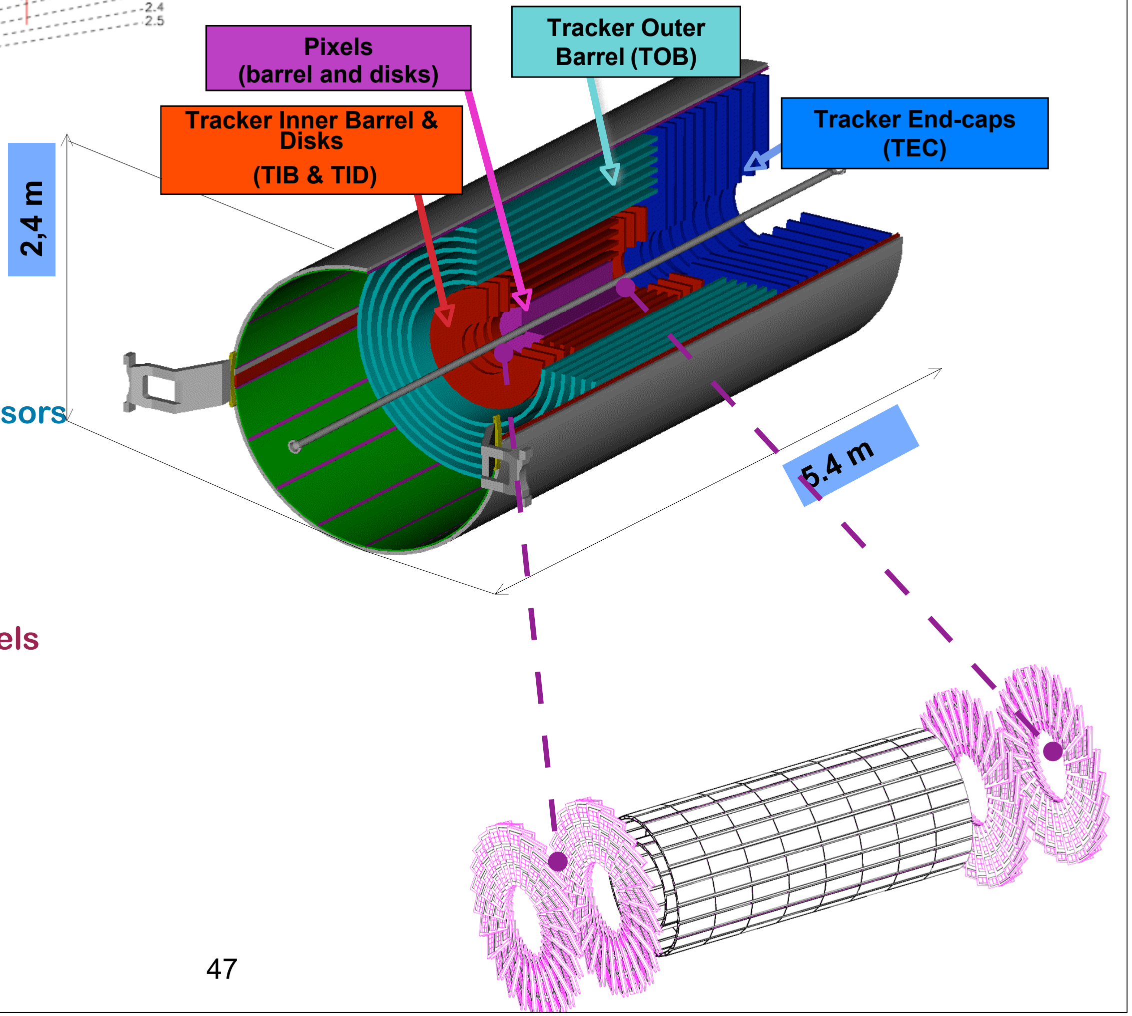
Magnetic field operating at 3.8 Tesla

STRIPS:

~200 m^2 micro-strip silicon modules
15.232 modules
6136 320 μm and 18.192 500 μm thick sensors
9.648.128 analogue channels
pitch from 80 a 183 μm
10-14 measurement points up to η ~2.5

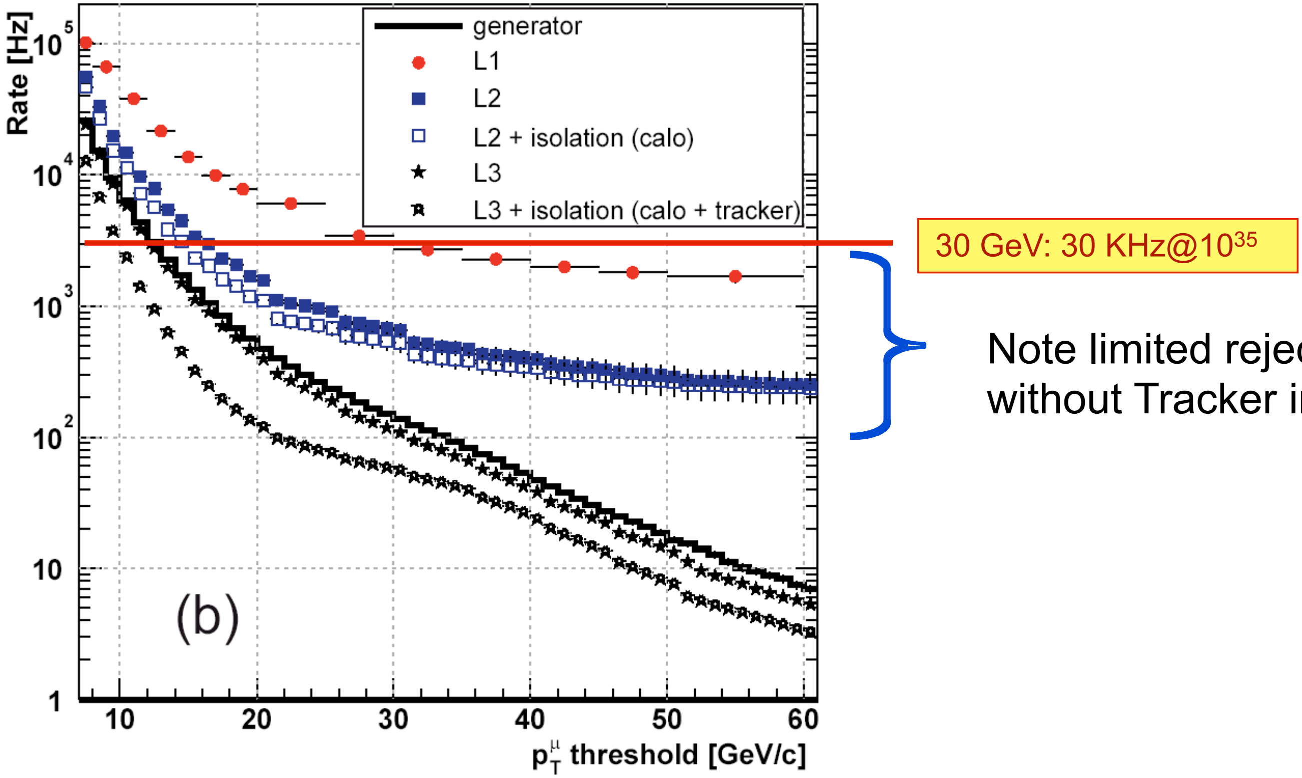
PIXEL:

~1 m^2 pixel modules pixel and 66 million pixels
1400 modules
4, 7 and 11 cm from beam (barrel)
pixel dimensions 100 x 150 μm^2



Tracker in High Level Triggers

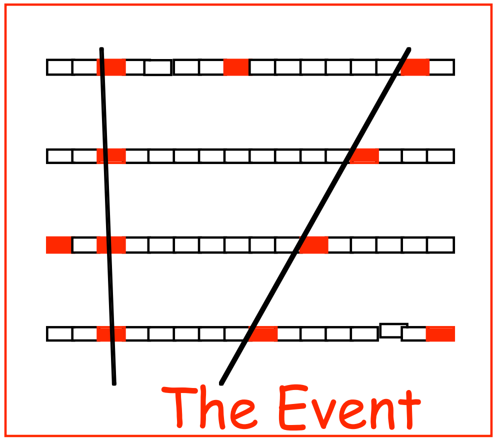
Muon Trigger rate at 10 ^{34} cm^{-2} s^{-1}

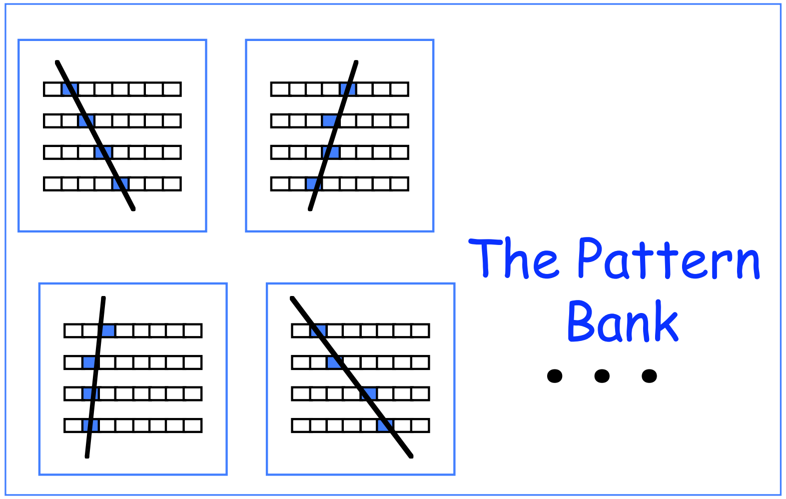


Note limited rejection power (slope) without Tracker information

Pattern matching with AM

- The pattern bank is a set of pre-calculated patterns
  - can accommodate for alignment
  - changing detector conditions
  - beam displacements
- An Associative Memory holds different patterns banks and compares them with the current event pattern

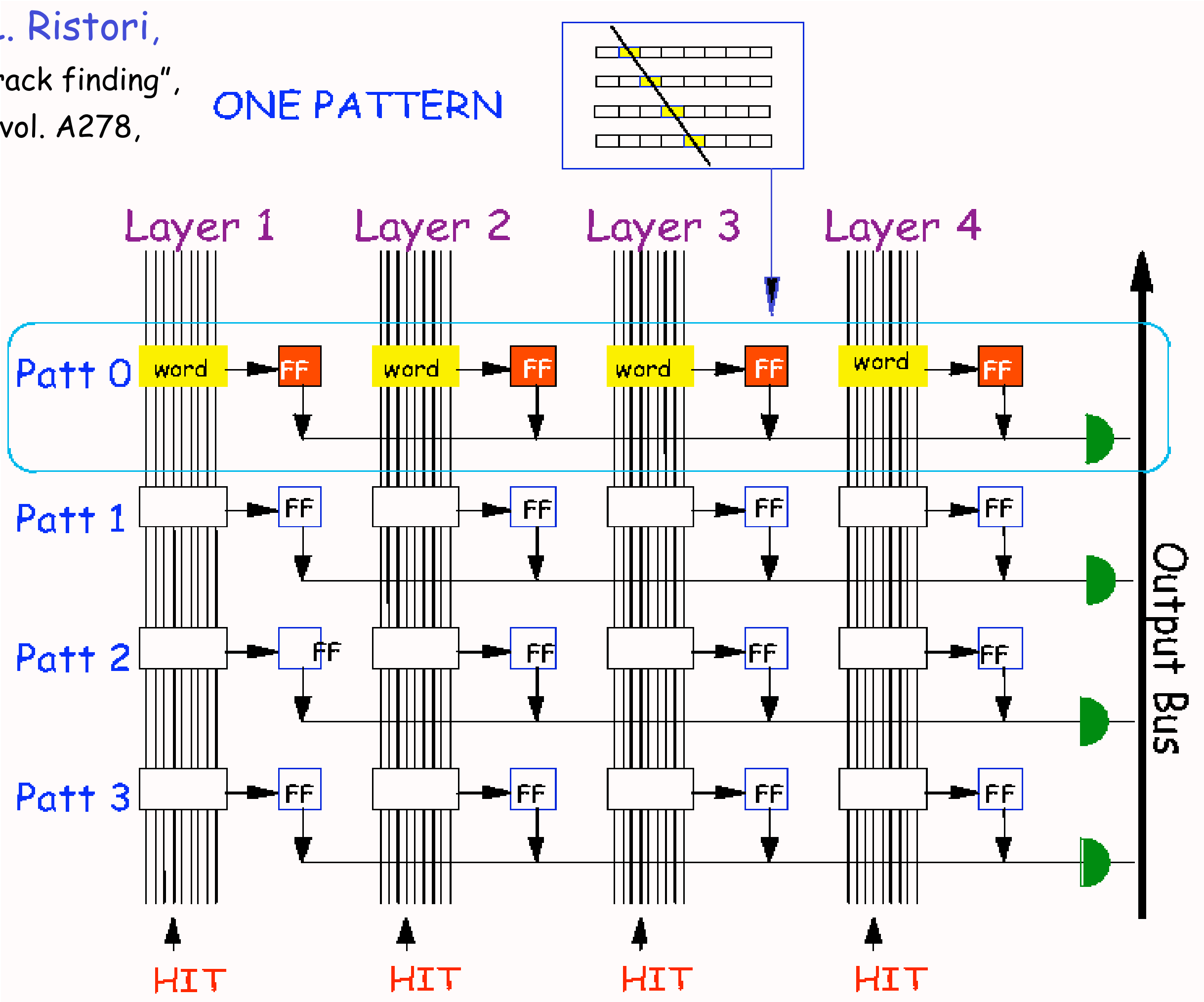




Associative Memory for pattern matching

M. Dell'Orso and L. Ristori,
"VLSI structures for track finding",
Nucl. Instr. and Meth., vol. A278,
pp. 436-440, (1989).

1 register
1 comparator
1 match FF
/ layer
/ pattern



Associative memories evolution

- Long history
  - 1990: Full custom VLSI chip - 0.7 μm (INFN-Pisa), 128 patterns/chip: high pattern density, not easy design
  - FPGA approach 1998: easier design but fewer density
  - A good compromise is the standard cell approach currently used for the SVT CDF upgrade: J. Adelman et al., Nuclear Science Symposium, 2005 IEEE, vol. 1, 2005, p. 603.
    - 0.18μm (INFN-Pisa), 5000 patterns/chip, 6 buses input lines, 50 MHz/bus, 18 bits/bus
      - produced by UMC (Taiwan) - design time ~8 months + 2 months production
- Forecast for 2013:
  - 90 or 65 nm technology would allow higher density pattern
  - Factor 4 higher clock speeds achievable
  - All in all: allow to reach ~30K patterns/chip with 200 MHz/bus speed

AM chip details

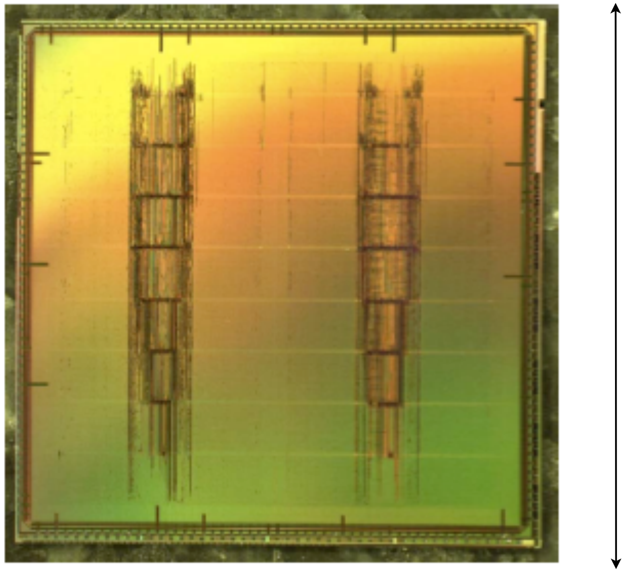
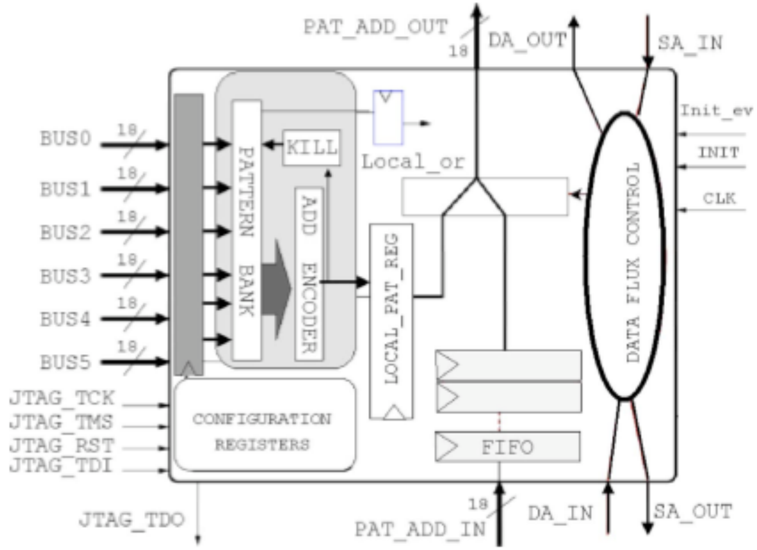


Fig. 2. Micrograph of the AMchip03 device. Four manually optimized columns of 1280 patterns each are visible. One on the left, one on the right and two in the middle. The two columns of lower density logic correspond to the interconnection and readout logic that was automatically placed. (Color version available online at http://ieeexplore.ieee.org.)

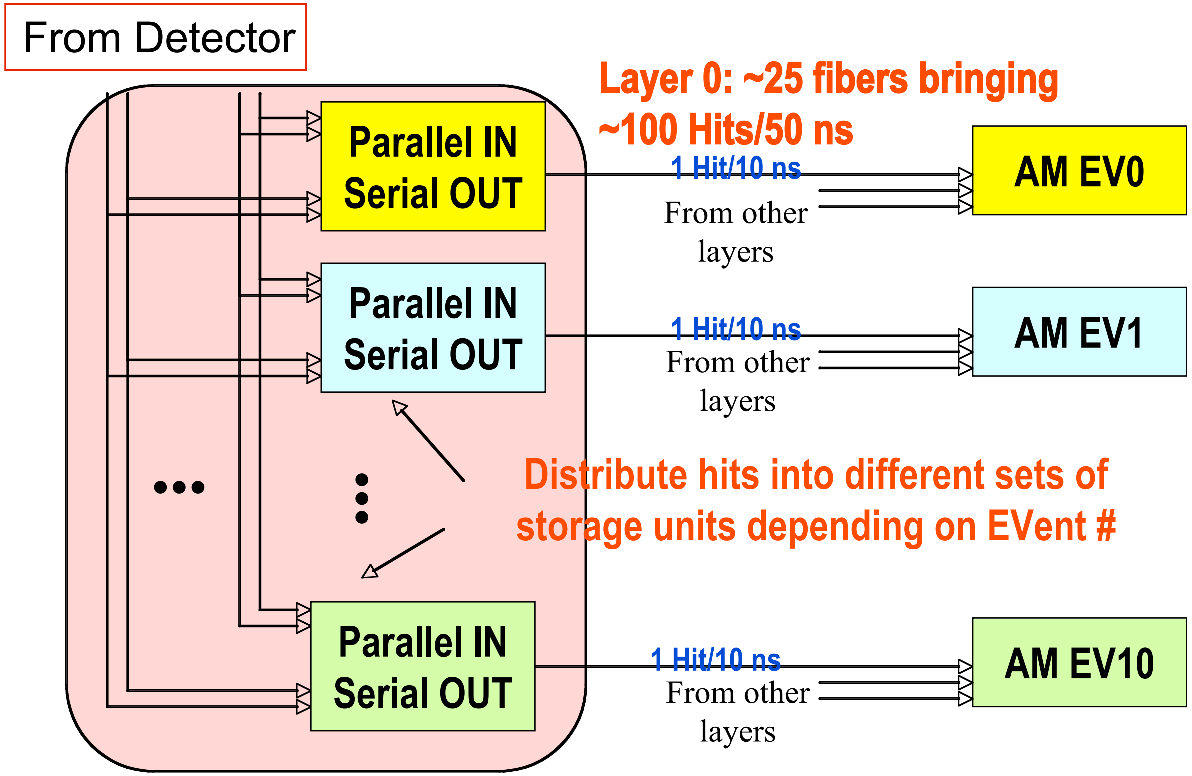


Power dissipation

Clock (MHz)	Power (W)
10	0.5
20	1.0
40	1.8

Switch conceptual design

A possible switch that allows the analysis of 10 consecutive events

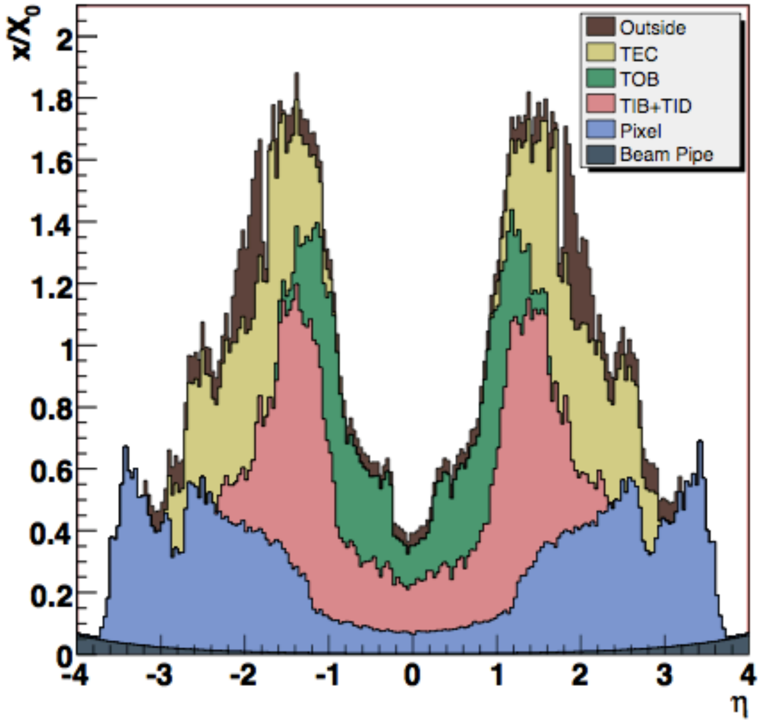


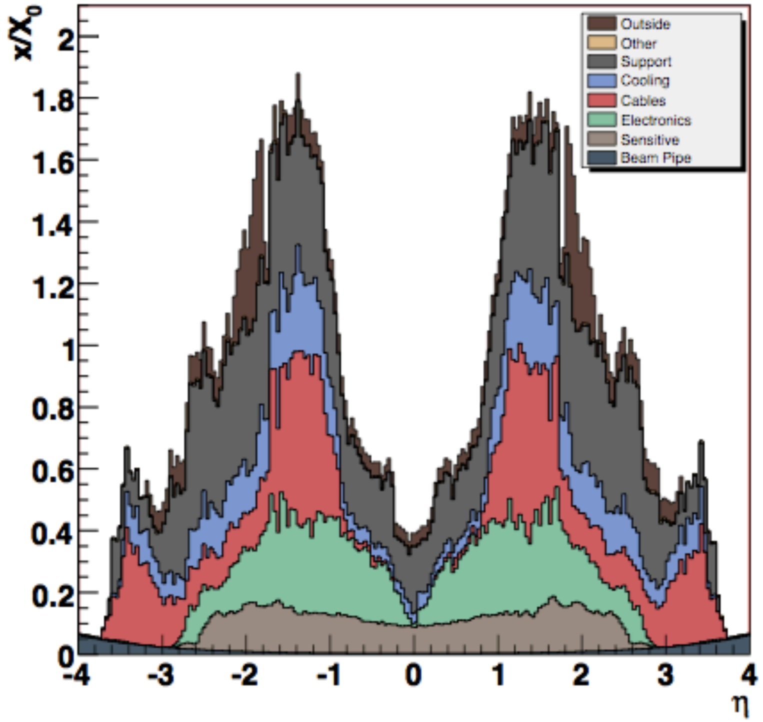
Some references

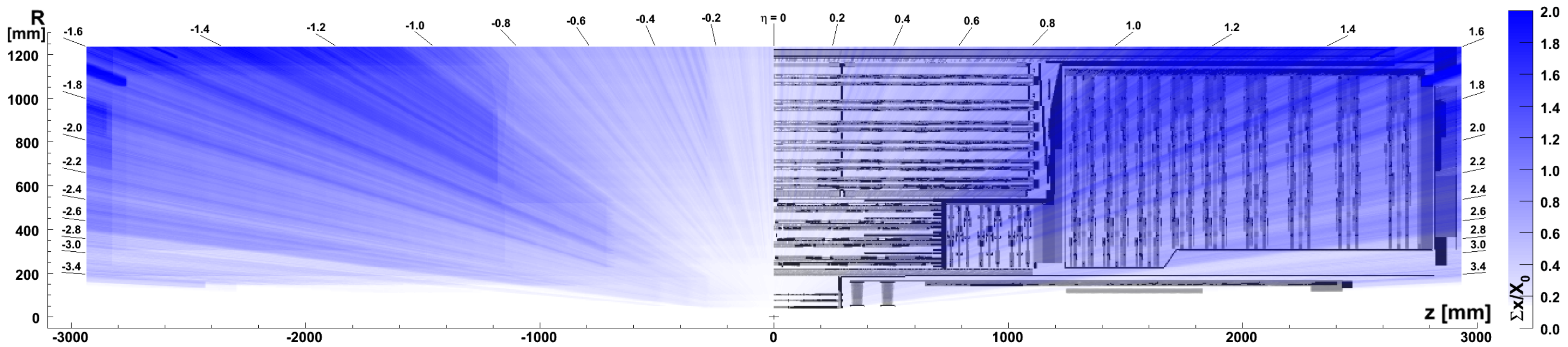
References

- F. Palla, JINST 2:P02002,2007
- F. Palla, F. Crescioli and F. Catastini, 15th IEEE Real Time Conference 2007 (RT 07)
- G. Barbagli, G. Parrini and F. Palla TWEPP-07, Prague 2007
  - http://indico.cern.ch/getFile.py/access?contribId=80&sessionId=29&resId=0&materialId=paper&confId=11994
- F. Palla, Vertex 2007 workshop
  - http://pos.sissa.it/archive/conferences/057/034/Vertex%202007_034.pdf

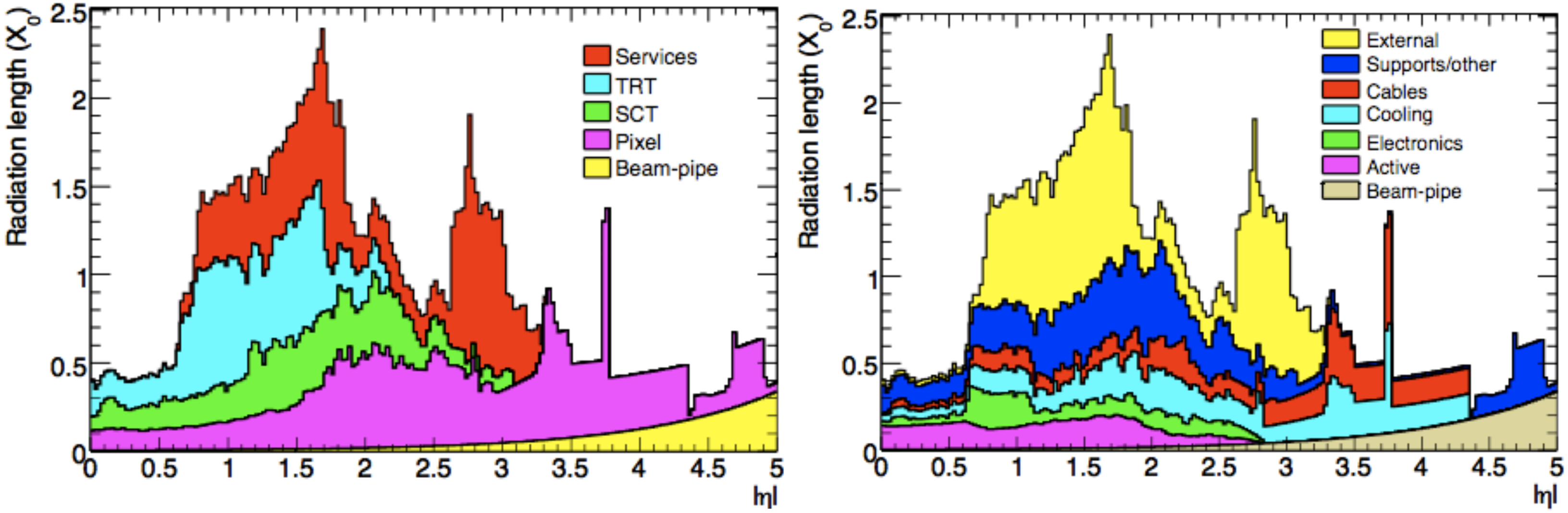
CMS Tracker Material budget







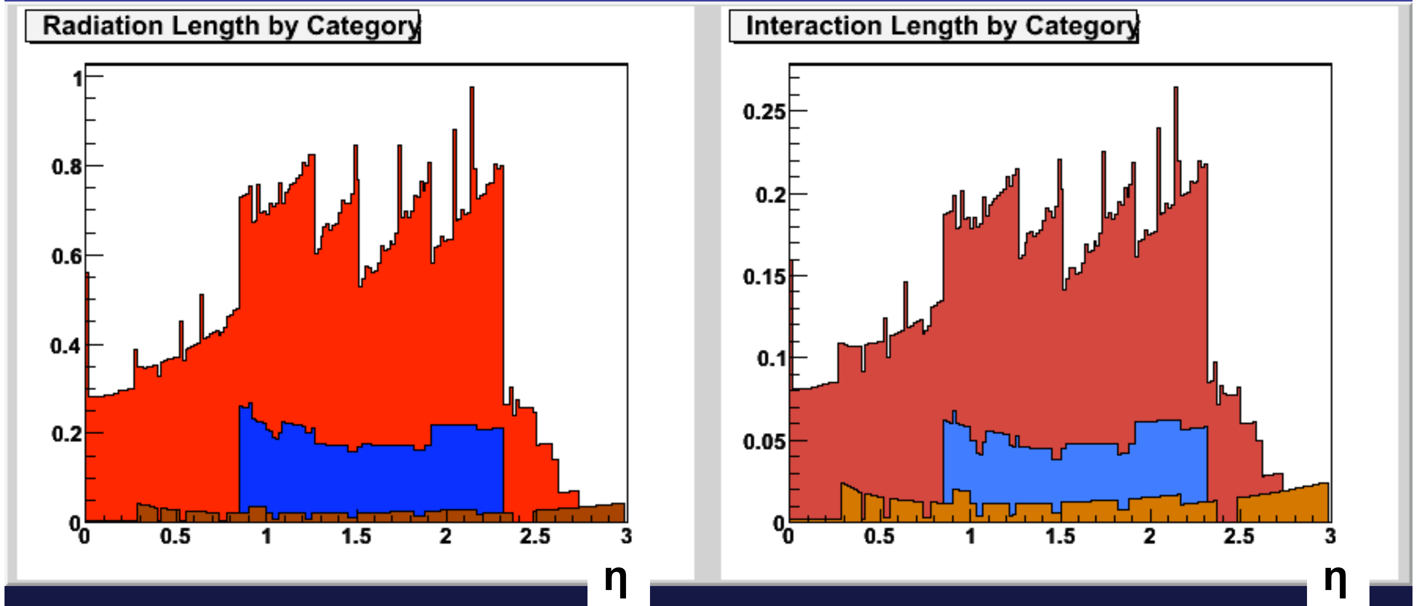
ATLAS



Radiation length (X0)
Services
TRT
SCT
Pixel
Beam-pipe
|η|
External
Supports/other
Cables
Cooling
Electronics
Active
Beam-pipe

X/X_0 and λ/λ_0

Material – “Cluster width”



- Average radiation length in tracking volume [0, 2.4]: 57%
  - Max of ~80%
- Average interaction length in tracking volume [0, 2.4]: 16%
  - Max of ~20%

D. Abbaneo