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Present and future inter pixel communication architectures in Timepix/Medipix derived read out chips

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The Medipix3 read out chip (ROC) demonstrates the successful use of inter-pixel communication to reconstruct spectroscopic information from X-ray hits in a segmented sensor mitigating the effects of charge sharing. Building on this work and the success of the current Timepix chip, conceptual designs for the matrix architecture of the Timepix2 and VELOpix ROCs are presented. These chips will use distributed analogue and digital architectures to increase the functionality available to each pixel and to perform significant on-chip data compression. Timepix2 will combine a measurement of the charge deposited in each pixel with a sub-2ns timestamp resolution and pipeline-trigger readout requiring significant on-pixel digital circuitry. The VELOpix chip being proposed for the LHCb VELO upgrade will utilise local pixel hit clustering and on-chip data compression to allow triggerless event readout at a sustained bunch crossing rate of 40MHz.

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