Interposer Development for CMS track-trigger upgrade R&D

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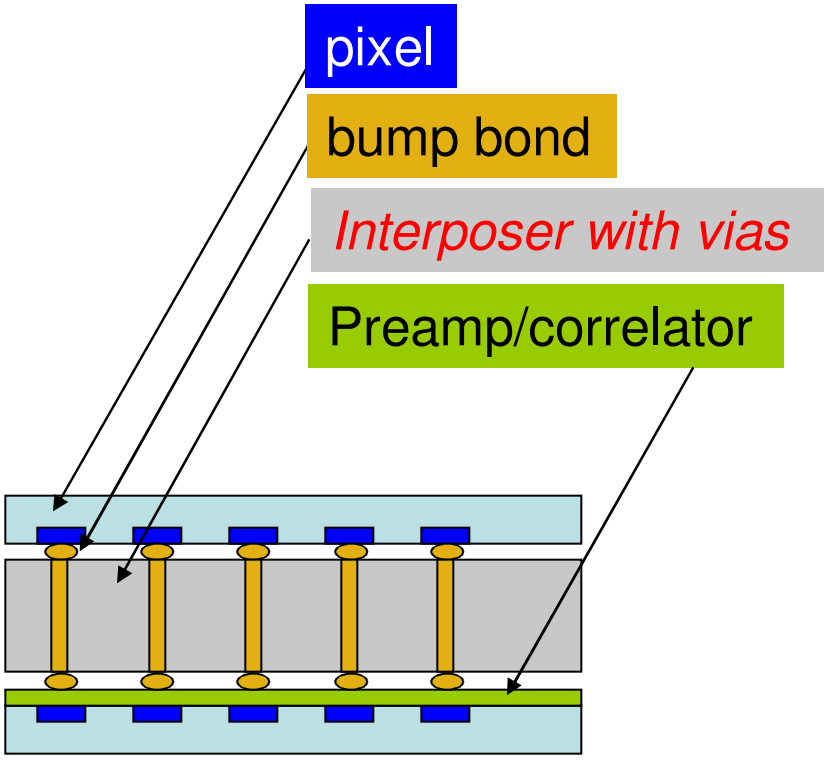
Many avenues explored in parallel

pT modules

QuickTime™ and a
decompressor
are needed to see this picture.

Conventional technology

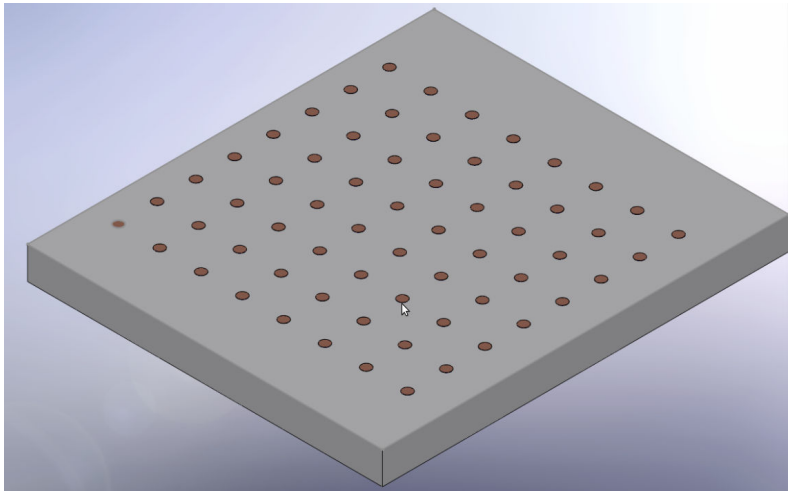
Vertically Integrated Modules



3D technology

Interposer Issues

- Vias
  - Achievable density
  - Aspect ratio, d/L
  - Yield
  - Electrical parameters (R, C)
- Mass
  - Thickness of interposer
  - Excess material removal
  - Choice of substrate
    - Silicon
    - Kapton
    - Other
  - Mechanical robustness
- Fabrication
  - Single substrate
  - Stacked & bonded layers
  - Internal traces for power, ground
  - Commercial capabilities



Silicon interposer prototype:

- 150um diameter vias
- 600x640um pitch
- 500um thick wafer

+ CTE, thermal conductivity, rigid, workable
- mass, X0

Cornell Nanofabrication Facility

- Nanotechnology user facility
  - ~16,000 sqft clean room space
  - ~100 fabrication and characterization instruments
  - ~20 staff members for support, training
  - Oriented to university researchers
    - Well adapted to working with students, etc
    - Very flexible, open-ended, willing to try new ideas
  - ~30% of operations are MEMS (MicroElectoMechanical Systems)
    - Microfluidics -- popular with biophysics, biomedical researchers
    - Moving parts -- micro machines, micro optical devices, etc
    - Quantum devices - entangled cantilevers

Fabrication overview

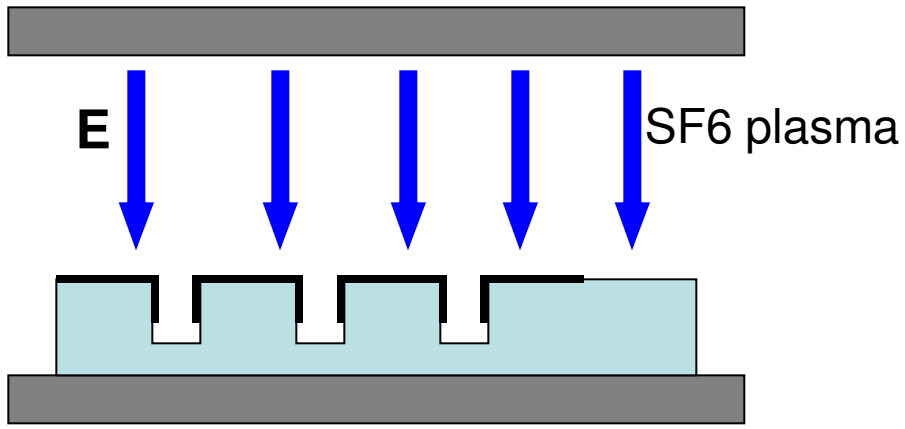
1. Oxidize 500 um silicon wafer
2. Etch SiO2 where vias are desired
3. Deep reactive ion etch silicon to make vias
4. Remove all oxide
5. Re-oxidize: insulated inner surface of via
6. Sputter metal - coat inner surface
7. Remove excess metal on surface
8. Add contact/bonding pads by evaporation
9. Dice

All work has been done by 2 students* at the Cornell Nanofabrication Facility

* Applied Physics, Electrical Engineering

Sidebar: Deep Reactive Ion Etching

- RF field to generate plasma (SF_6)
- SiO2 on surface is patterned to define etch locations -- hard resist
- Static E field to enforce directionality on ion motion --> vertical sidewalls
- Bosch process: alternate etch with passivation growth on walls. This limits sideways etching. Slight scalloping of walls. ~1000 cycles
- Etch rate 1~10 um/min
- Walls not perfectly vertical: 3-5% slope is typical spec.



Interposer fabrication - 1

1. Oxidize wafer - 3 hours, 1200C; 1.5um SiO2. Wafers are 500um thick.

This oxide will define the via location and diameters.

Interposer fabrication - 2

Prepare mask for defining holes in oxide where vias will be etched.

(Manan Suri at the mask developer.)

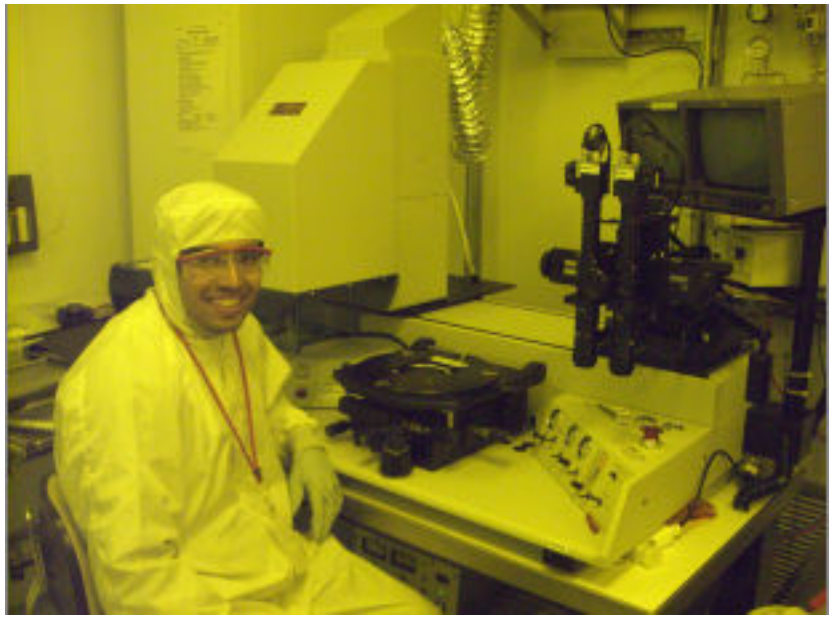
Interposer fabrication - 3

Spin resist on wafer

Tim Lutz at spinner.

Interposer fabrication - 4

Contact aligner: align mask on wafer; then expose to UV and develop by hand. Result is resist patterned with holes where vias will be.



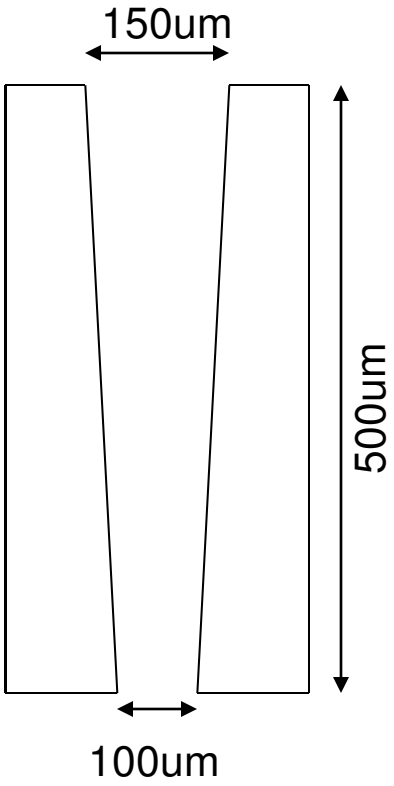
Plasma etch: 500W RF etcher, use SF6 to etch the SiO2. This opens holes in the oxide at via locations, exposing raw silicon in preparation for subsequent silicon etching.

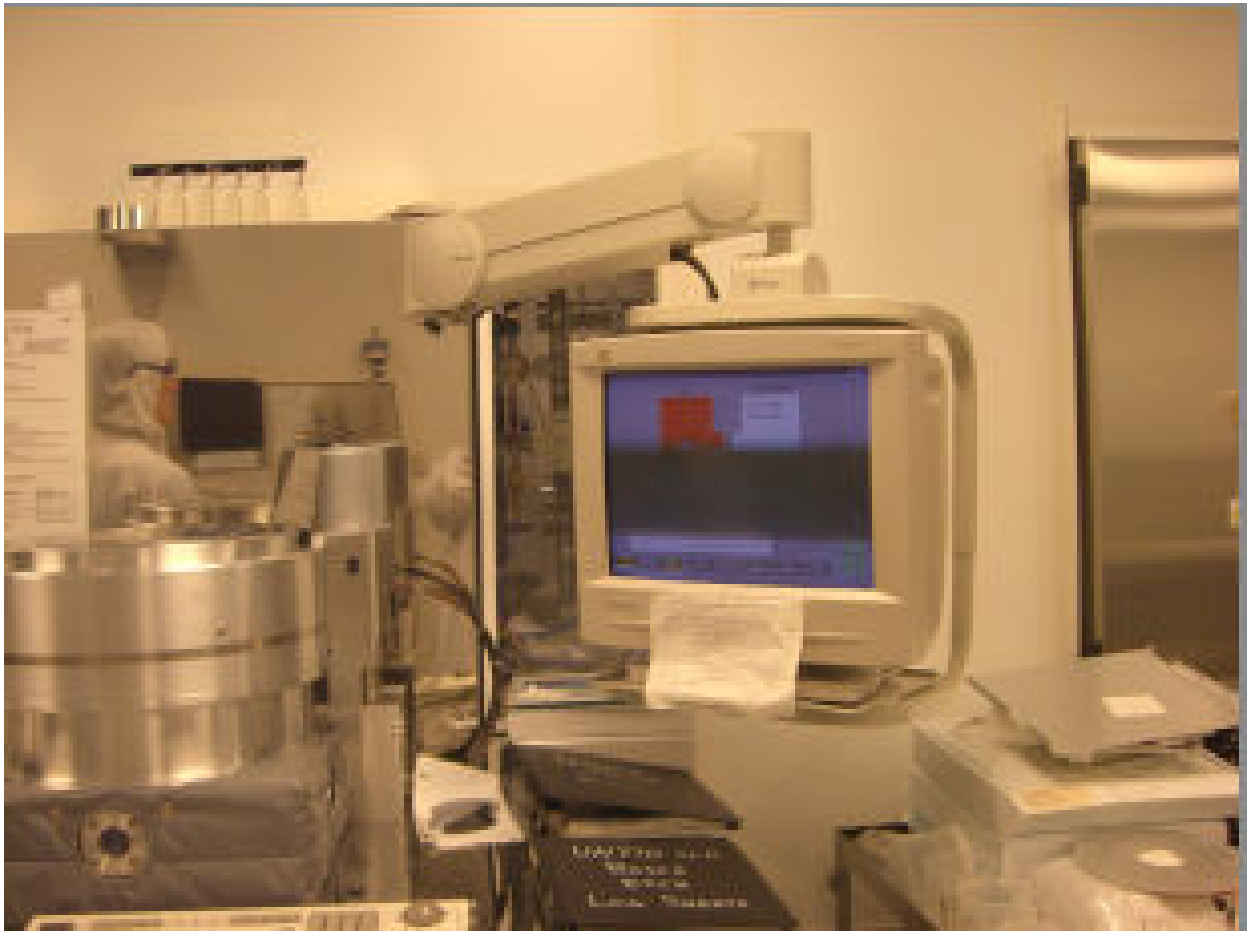
Interposer fabrication - 5

Deep silicon etching: “drilling” the vias.

Bosch flourine process, Uniaxis SLR 770 etcher: 2 um/min, aspect ratios up to 20:1.

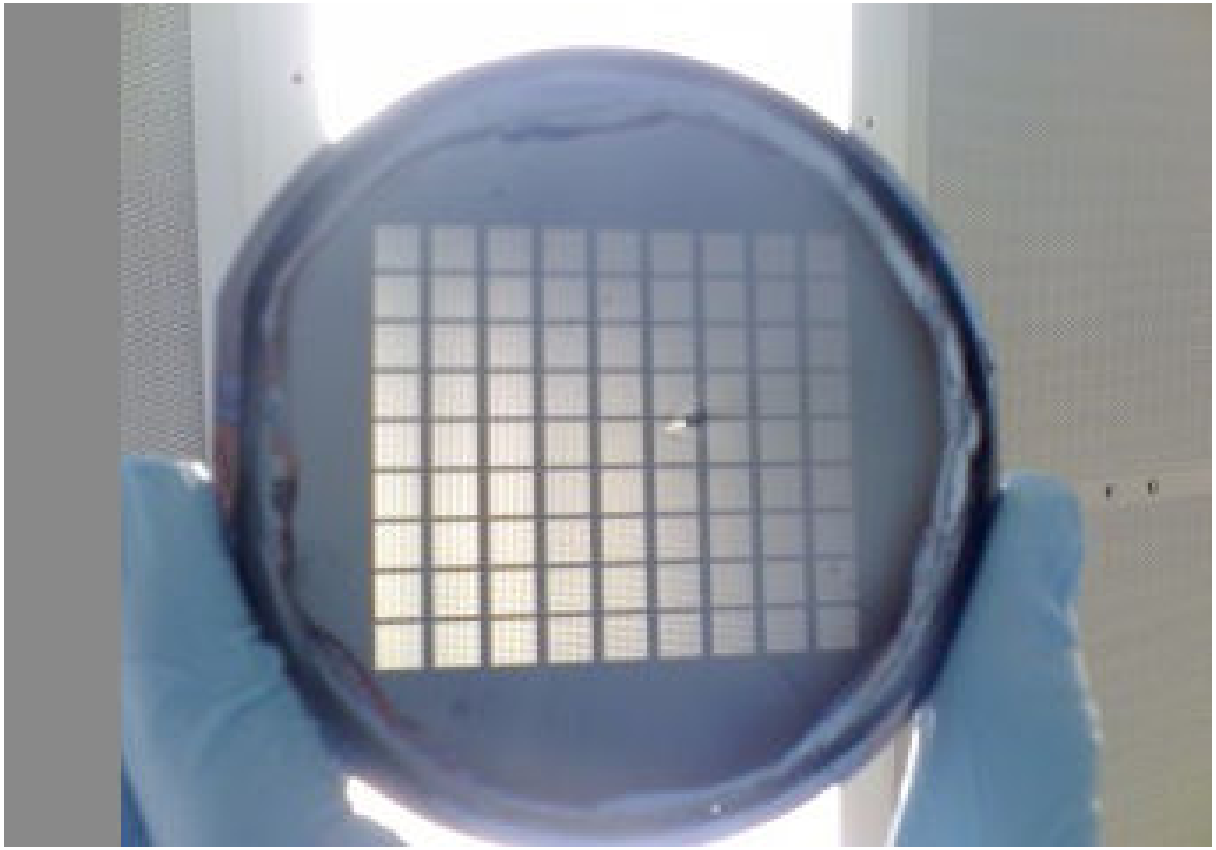
Total etch time in 500um wafer: 7 hours. (New etcher at CNF will be < 2 hours)





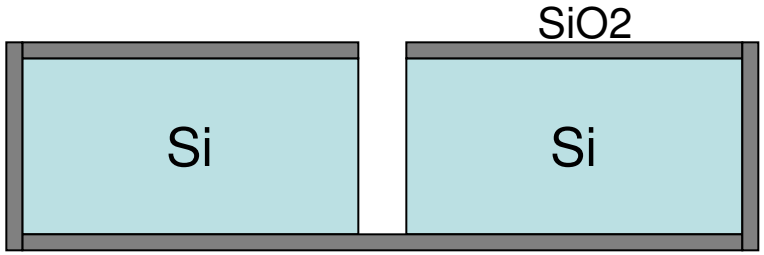
Etched wafer

81 interposers; each square contains a 64-via array



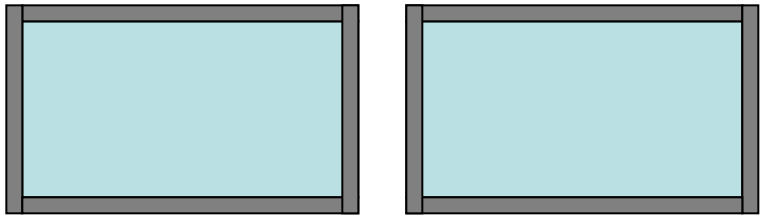
Interposer fabrication - 6

After deep etching, vias exist but are closed off on back side by SiO2 layer.



Next steps:

- remove resist
- etch SiO2
- re-oxidize to develop uniform oxide over all surfaces including inside the vias. 80 minutes --> 1um SiO2.
- dice wafers
- sputter…



Interposer fabrication - 7

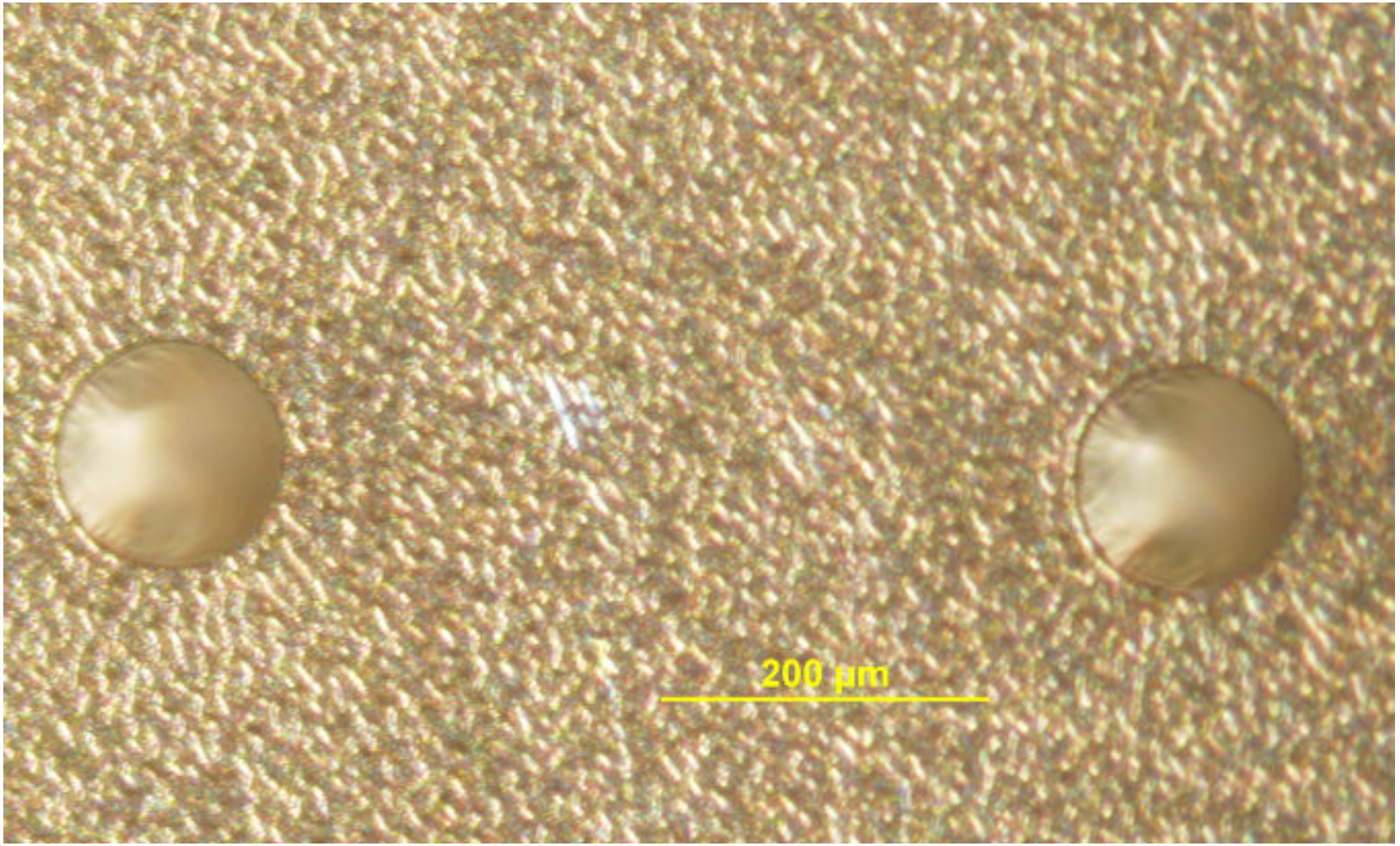
Sputtering: CVC 601 sputtering deposition system.

Many metals are possible (Al, Al+1%Si, Al+1%Si+4%Cu, Co, Cr, Cu, MoSi, Nb, Si, SiO2, Ta, Ti, TiW, W).

Deposition is done from both sides, and the sample is rotated to try to achieve best coverage inside the via, all the way thru.

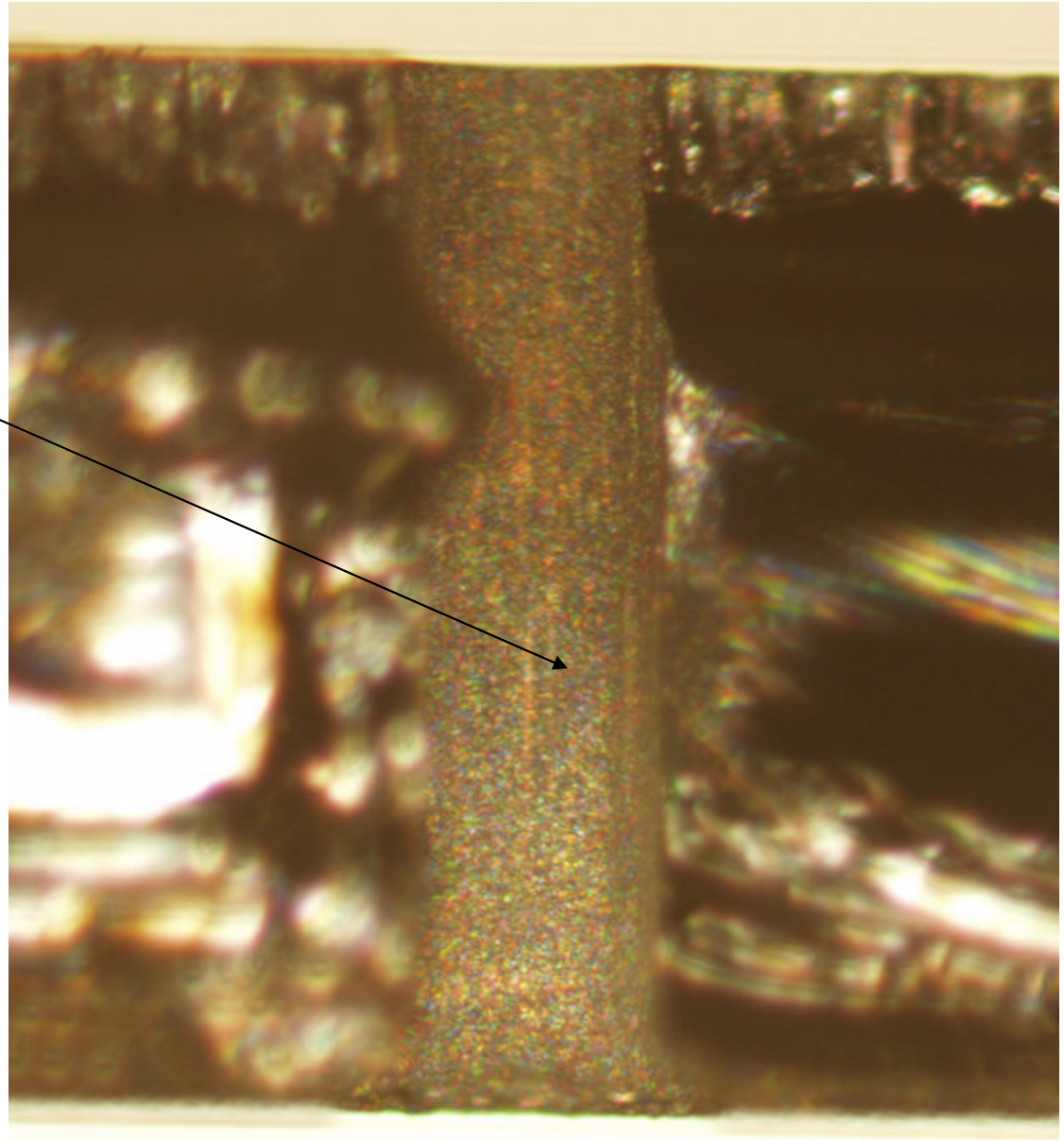
Interposer fabrication - 8

- Surface after sputtering. Two vias shown, 150um diameter, 600um separation.



Interposer fabrication - 9

- Interior of via after sputtering. (Aluminum)
- 60 minute sputtering, 30min each side
- Grainy surface indicates good metal coverage



Interposer fabrication - 10

- Via with copper metallization
- 30 minute sputtering
- M&T believe the copper sputtering quality is superior to aluminum.

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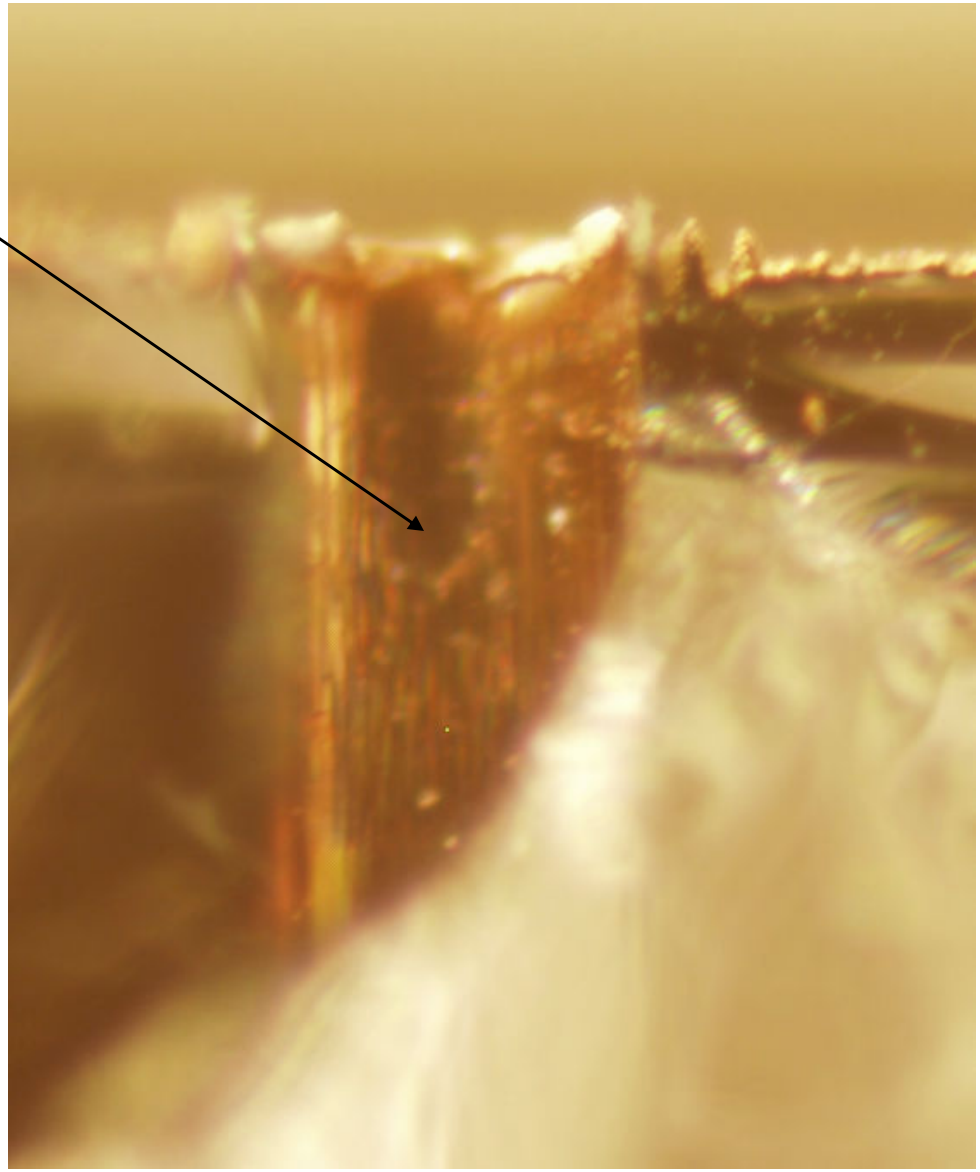

Swiss Cheese Model

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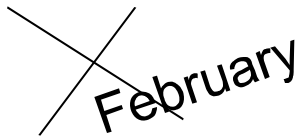
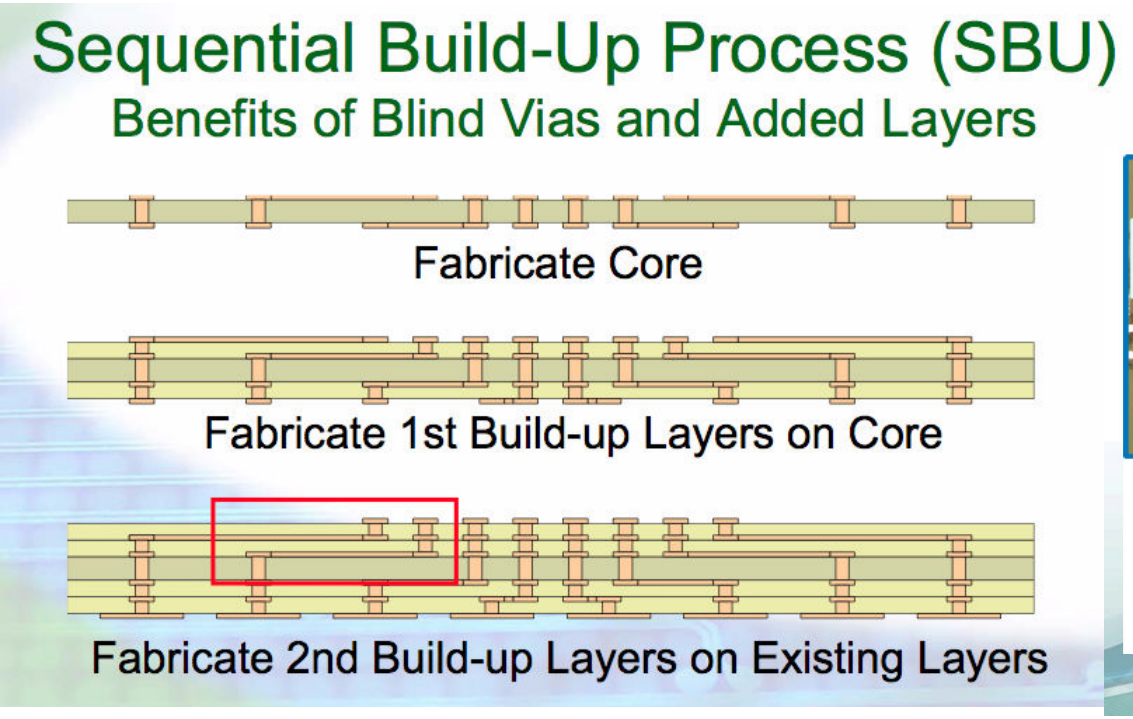
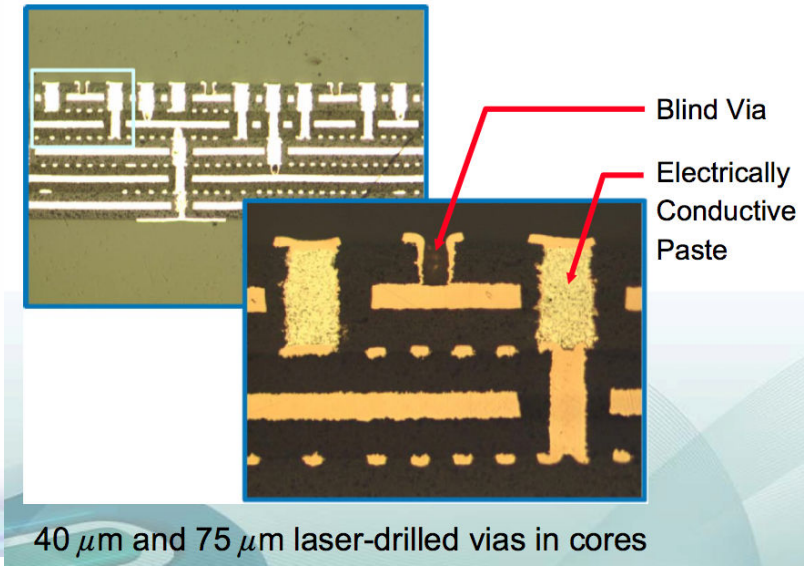


Industrialization

- So far, little activity. But…
- Micralyne (Calgary, AB): several phone meetings, negative result.
- Endicott Interconnect (Endicot, NY): Manan & Jim visited in August.
  - Good local resource
  - Willing to do R&D in silicon, but this isn't their normal medium
  - Organic polymers are their preferred medium. Previously: ceramics
  - Vias can be done by laser drilling, mechanical drilling, etching, etc .
  - complex interconnects with many internal layers and cross circuitry, blind vias, etc





Future

- Bonding tests & R, C measurements - with UC Davis
- Production of final prototype for first test module

- Explore via properties: density, taper, metalization, etc
- Swiss cheese mass reduction
- Multi-wafer sandwich
- Kapton - external