Developing ITk Front-End Silicon-Strip Readout ASIC Testing Capability at Carleton University

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On behalf of the ATLAS Canada ITk Collaboration
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W3-7 Applied Physics Instrumentation (DAPI) | Instrumentation de physique appliquée (DPAI)
Talk ToC

- Overview of ATLAS ITk Strips Detectors and HL-LHC
- Carleton's scope-setting exercise and decisions
- Capability ramp-up and initial testing
- Results of first ASIC wafer tests
- Current ASIC testing work and next steps
The current ATLAS Inner Detector designed for:
- 10 year operation, integrated luminosity of 300 fb$^{-1}$
- instantaneous luminosity of $1.0 \times 10^{34}$ cm$^{-2}$ s$^{-1}$
- 14 TeV centre-of-mass energy, 25 ns between crossings
- pile-up of 23 proton-proton interactions per crossing

The new Inner Tracker (ITk) is designed for:
- 10 year operation, integrated luminosity of 4000 fb$^{-1}$
- instantaneous luminosity of $7.5 \times 10^{34}$ cm$^{-2}$ s$^{-1}$
- 14 TeV centre-of-mass energy, 25 ns between crossings
- pile-up of 200 proton-proton interactions per crossing
Carleton Motivation

- Long history of CERN detector development and assembly
  - OPAL Detector (at LEP, before the LHC)
  - ATLAS Forward Calorimeter
  - small-wire Thin-Gap Chamber for ATLAS NSW
- Little or no involvement with newer silicon-based detectors – technologies critical to modern particle collider experiments
- Many new detectors in numerous domains are using silicon
  - evolution in semiconductor industry means large area silicon detectors are no longer prohibitively expensive
  - e.g. ITk strips area of 165 m² is 2.5 times current system
  - capabilities of silicon sensors continue to expand with on-chip data processing and other innovations
ITk Architecture

Scoping Carleton's Involvement

- Strip detectors (vs. pixel) made the most sense to consider
- End-cap strip petals were under-resourced at the time
- Trip undertaken to DESY Hamburg and Zeuthen to learn how strip modules and petals were assembled and tested
- Partnership initiated with Carleton Dept. of Electronics to access their semiconductor probing stations and cleanrooms
- Focus was to be testing of end-cap silicon strip sensors
  - Partnered with local company *MuAnalysis* to access confocal laser scanning microscope and metrology lab
- Commissioned DAQ at Carleton and used a strip module at UofT to test and document system integration and operation
  - Acquired our own strips module (ABCN250-based)
Carleton’s Initial Configuration

Karl Seuss PSM6 Manual Probe Station

Wentworth 901M Manual Probe Station with Temptronic TO0315B ThermoChuck

MuAnalysis Confocal Laser Scanning Microscopy for metrology and QA/QC

Single-Chip ABC130 DAQ Load, Xilinx FPGA-based controllers, Linux PC with DAQ S/W

Canadian-made ITk Prototype Module with Sensor and ABCN250-based Hybrid (has a “B-grade” sensor)
ABC = ATLAS Binary Chip: front-end readout ASICs

ABC130 (and ABCN250) were earlier prototypes

ABCStar will be the final version (prototypes due this year)
**ITk Strips Detector Components**

- **ABCStar testing was going to need roughly 3 years!**

<table>
<thead>
<tr>
<th>Barrel Layer</th>
<th>Radius [mm]</th>
<th># of staves</th>
<th># of modules</th>
<th># of hybrids</th>
<th># of ABCStar</th>
<th># of channels</th>
<th>Area [m²]</th>
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<tbody>
<tr>
<td>L0</td>
<td>405</td>
<td>28</td>
<td>784</td>
<td>1568</td>
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<td>5488</td>
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<tr>
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<table>
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<th>End-cap Disk:</th>
<th>z-pos. [mm]</th>
<th># of petals</th>
<th># of modules</th>
<th># of hybrids</th>
<th># of ABCStar</th>
<th># of channels</th>
<th>Area [m²]</th>
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<td>32</td>
<td>576</td>
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<td>Total one EC</td>
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<td><strong>165.25</strong></td>
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ASIC Testing At RAL (UK)

- Adapted DAQ software and firmware to test wafers
  - Repurposed existing Micromanipulator semi-automatic probe station to test wafers (much custom software)
  - Multi-year intensive R&D effort to develop system to characterize ABCN250 and ABC130 chips on wafers
  - Was only facility that could test the ITk wafers
  - Very hands-on process requiring expert operator
    - Necessary for R&D, but only one to a few wafers/day
Can Carleton Test ASICs As Well?

- Multiple sites highly desirable for front-end ASIC testing
  - Replicate probe station setup at RAL in the UK?
  - Go our own route (acquire equipment or outsource)?
- Acquired an old “Batch 1” ABC130 wafer from RAL
  - Initial design had metalization error: shorted transceiver
- Partnered with local company DA-Integrated
  - Business model is to work with small/medium players
  - Design and manufacture probe card for ABC130
  - NRE contract to collaboratively implement test vectors
  - Test ABC130 wafers on industry standard wafer prober
  - Arrange with partner company to dice the tested wafer
Short Answer: Yes!

First Data from ABC130! (photo of prober screen)
“Batch 1” Testing At Carleton

- Spent two weeks at RAL testing “Batch 4” ABC130 wafers
- Determine CMOS/SLVS interface requirements for ABC130
- Reverse engineer complex DAQ code
  - Written in C/C++/ROOT
  - On “Batch 1”, only the basic analog could be tested
  - Provided DA Integrated with test “cookbook”, they wrote code
  - Work collaboratively with their engineers to adapt/debug tests
  - Pass/fail on prober, offline data analysis at Carleton
- Much to be learned to bridge physics/engineering domains
We are using their *Electroglas 4090μ* automated wafer prober:
- Can test a wafer of ABC130 chips in about 15 minutes
- Can be programmed in C/C++ (used for analog tests)
- Can run tests provided as binary pin stimulation vectors
- Has sophisticated test debug/visualization tools

Carleton is provided with a pass/fail wafer map and all measurements in a text file format (we wrote a parser)
Example Data Analysis (Analog Tests)

Sweeping D/A converters and reading the associated voltage on the Analog Multiplexer pin

SLVS output driver current sweep measurements (DATAL, DATAR, XOFFL, and XOFFR)

Individual LDOA and LDOD measurements

Distribution of LDO tuning parameters across entire wafer
Great concern at CERN about dicing yield/different methods

Wafer is pre-thinned to \(~300\mu m\) and dicing partner was concerned about possible chipping and delamination

Challenge due to Multi-Project Wafer (sacrificed TDCPix)

Results were as good as or better than existing provider
With success of “Batch 1” testing, Carleton received two “Batch 4” wafers (fully functional chips, tested at RAL)

Need to communicate with all I/O pins to the chip now

- Translate digital test vectors from coded format used by DAQ into binary 1/0 stimulation vector for prober
- To determine output, use empirical test: send test vector, see what comes out (once), expect that every time
- Some tests require pattern searching and field masking

Successfully tested purely digital portion of chip 2 weeks ago

Now working on test vectors for testing the ASIC front end

- Back to reverse engineering DAQ – tests complex
- Will likely provide “cookbook” to DA Integrated again
160MHz point-to-point vs. 80/160MHz daisy-chain datapath

- Expect the first wafers to be available as early as August 2018
- Wafer includes ABCStar, HCCStar, AMAC, and unrelated chip
  - Multi-Project Wafer will present serious dicing challenge
Conclusion

- Carleton has been able to expand its capabilities to include the testing and characterization of both silicon sensors for HEP and their associated readout and control ASICs.

- In addition to sensor testing, the work we have done partnering with a commercial vendor of wafer test services and dicing may prove critical to timely completion of the ITk (testing all 700 wafers could be done in two to three months).

- We can now participate in this and future silicon-based detector development and testing, including custom chips for readout and communication, as we build the foundations needed to do R&D with these leading-edge technologies.

- Through the expertise developed, exciting new opportunities for faculty and students at all levels are opened up.
Questions?

This work has been made possible by significant contributions by: Thomas Koffas, Dag Gillberg, John Keller, and Ezekiel Staats, Carleton Dept. of Physics; Steve McGarry, Rob Vandusen, and Garry Tarr, Carleton Dept. of Electronics; Peter Philips and Bruce Gallop, Rutherford Appleton Laboratory; Matt Warren, University College London; and Ingo Bloch, Deutsches Elektronen-Synchrotron, Zeuthen campus.

Background and title slide image source: ATLAS and CMS upgrade proceeds to the next stage, Contardo and Wells, CERN Courier, Jan 15, 2016.
Introduced new feature: chose 8 representative front-end pads
  - Will use calibrated gated capacitor discharge as charge source (~fC)
RAL concern: probe pins will disrupt self-test measurements
Carleton goal: provide precision performance and calibration data
ABC130 Chip Architecture

Front End x256

Comparator

Input Register (Mask Register)

LO_Buffer

L1_Buffer

Top_Lo gic

L1_DCL

R3_DCL

Status, Readback

ReadOut Block

Detector pads: 256 input pads

Command Decoder

Data, Xoff

BC

COM/LO

R3/L1

RC/LO

Data, Xoff
Digital Test Vector Translation

DA Integrated cannot run RAL DAQ system, so Carleton must decipher it and specify “raw” bit-level coding for use in their IC prober system.

Input: “ITSDAQ format” digital test vector
Output: CSV format ASCII-coded binary pad stimulation vector for Electroglas

Worked with DA Integrated on “universal” pad stimulus vector structure and timing.

- Wrote software to provide human-readable “disassembly” of ABC130 bit streams.