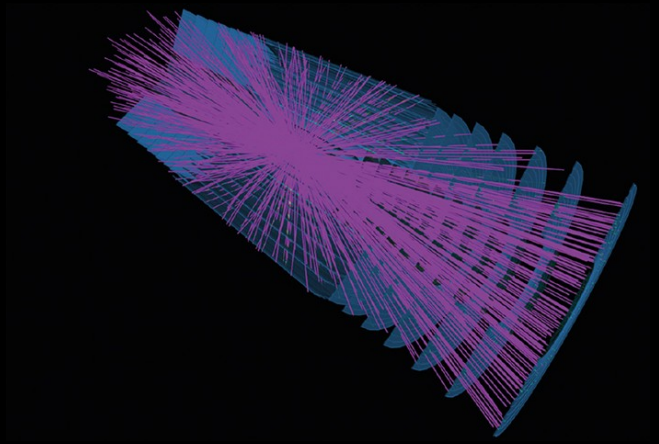
HL-LHC ATLAS ITk Strip Detector



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Developing ITk Front-End Silicon-Strip Readout ASIC Testing Capability at Carleton University

James Botte (jbotte@cern.ch)
On behalf of the ATLAS Canada ITk Collaboration

June 13, 2018 – 2018 CAP Congress / Congrès de l'ACP 2018

W3-7 Applied Physics Instrumentation (DAPI) | Instrumentation de physique appliquée (DPAI)

Talk ToC

- Overview of ATLAS ITk Strips Detectors and HL-LHC
- Carleton's scope-setting exercise and decisions
- Capability ramp-up and initial testing
- Results of first ASIC wafer tests
- Current ASIC testing work and next steps

ITk Motivation: HL-LHC

- The current ATLAS Inner Detector designed for
  - 10 year operation, integrated luminosity of 300 fb^{-1}
  - instantaneous luminosity of 1.0×10^{34} cm^{-2} s^{-1}
  - 14 TeV centre-of-mass energy, 25 ns between crossings
  - pile-up of 23 proton-proton interactions per crossing
- The new Inner Tracker (ITk) is designed for
  - 10 year operation, integrated luminosity of 4000 fb^{-1}
  - instantaneous luminosity of 7.5×10^{34} cm^{-2} s^{-1}
  - 14 TeV centre-of-mass energy, 25 ns between crossings
  - pile-up of 200 proton-proton interactions per crossing

Carleton Motivation

- Long history of CERN detector development and assembly
  - OPAL Detector (at LEP, before the LHC)
  - ATLAS Forward Calorimeter
  - small-wire Thin-Gap Chamber for ATLAS NSW
- Little or no involvement with newer silicon-based detectors – technologies critical to modern particle collider experiments
- Many new detectors in numerous domains are using silicon
  - evolution in semiconductor industry means large area silicon detectors are no longer prohibitively expensive
  - e.g. ITk strips area of 165 m^2 is 2.5 times current system
  - capabilities of silicon sensors continue to expand with on-chip data processing and other innovations

ITk Architecture

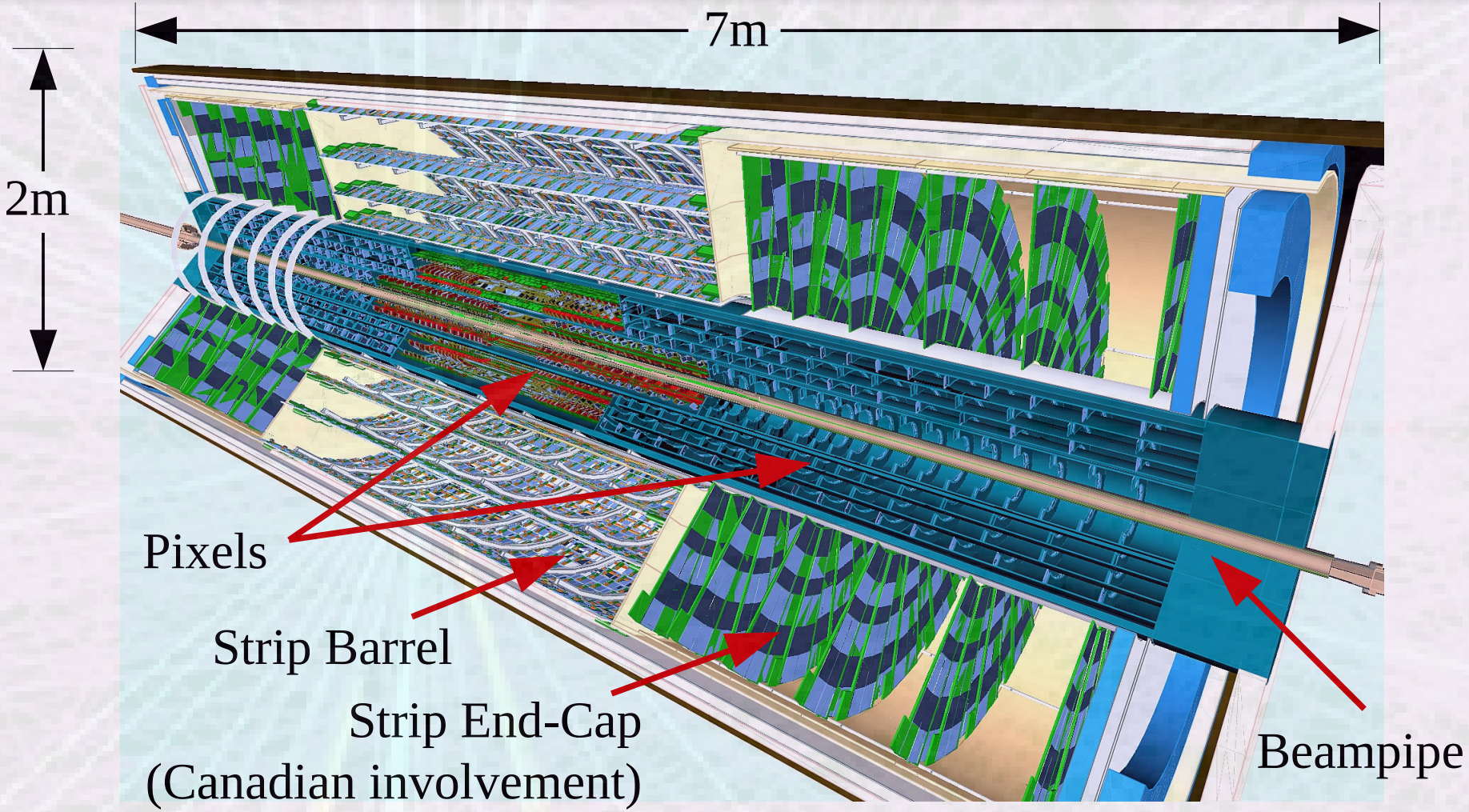

Image source: Technical Design Report for the ATLAS Inner Tracker Strip Detector, The ATLAS Collaboration, CERN-LHCC-2017-005, 2017.

Scoping Carleton's Involvement

- Strip detectors (vs. pixel) made the most sense to consider
- End-cap strip petals were under-resourced at the time
- Trip undertaken to DESY Hamburg and Zeuthen to learn how strip modules and petals were assembled and tested
- Partnership initiated with Carleton Dept. of Electronics to access their semiconductor probing stations and cleanrooms
- Focus was to be testing of end-cap silicon strip sensors
  - Partnered with local company ***MuAnalysis*** to access confocal laser scanning microscope and metrology lab
- Commissioned DAQ at Carleton and used a strip module at UofT to test and document system integration and operation
  - Acquired our own strips module (ABCN250-based)

Carleton's Initial Configuration

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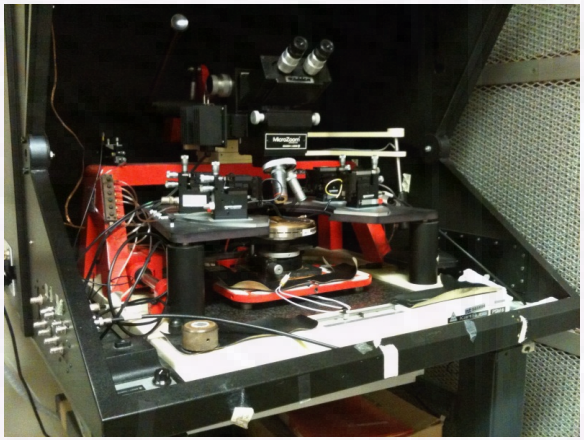
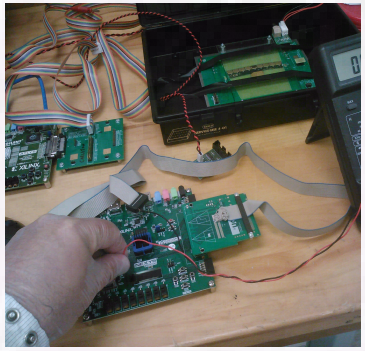
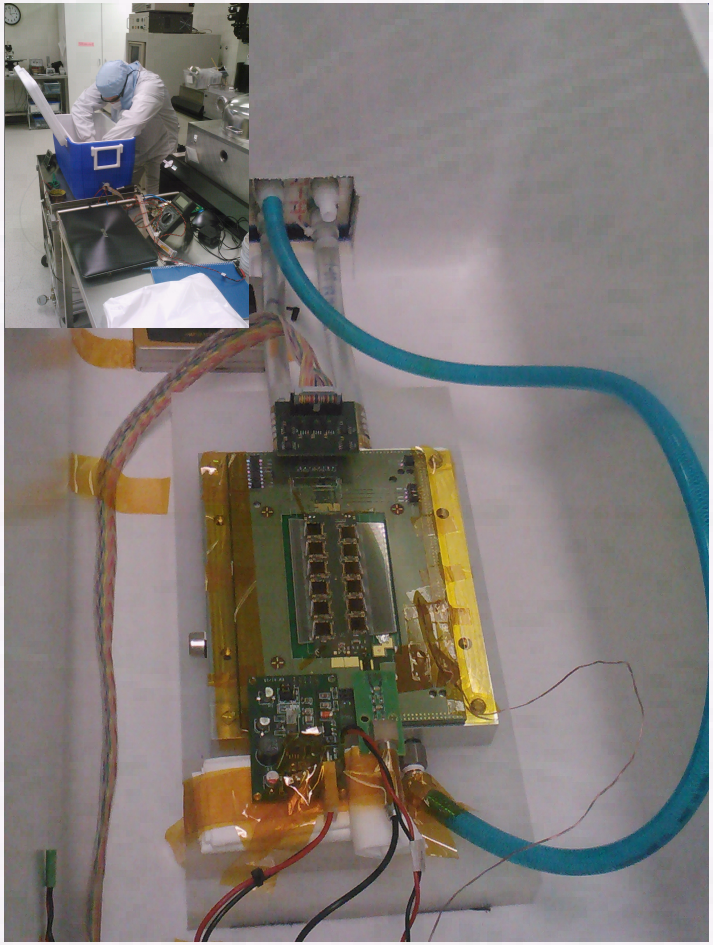


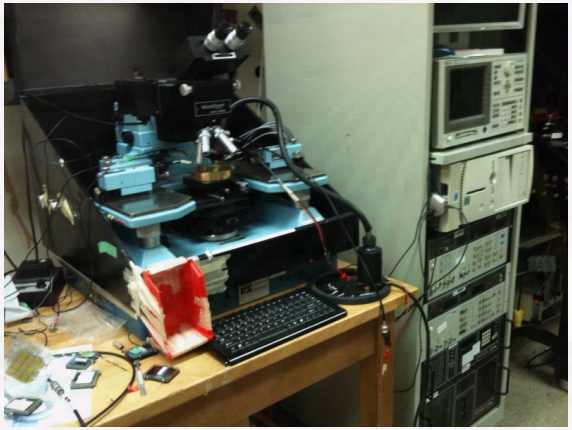
Karl Seuss PSM6 Manual Probe Station



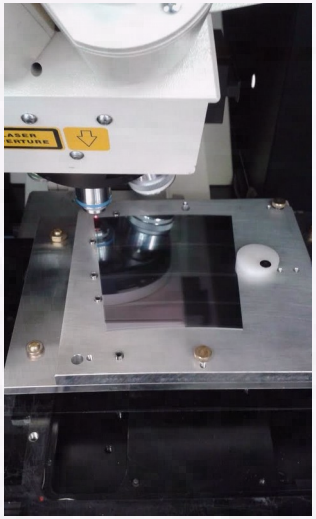
Single-Chip ABC130 DAQ Load, Xilinx FPGA-based controllers, Linux PC with DAQ S/W



Canadian-made ITk Prototype Module with Sensor and ABCN250-based Hybrid (has a "B-grade" sensor)



Wentworth 901M Manual Probe Station with Temptronic TO0315B ThermoChuck



MuAnalysis Confocal Laser Scanning Microscopy for metrology and QA/QC

ITk Strip Module Design

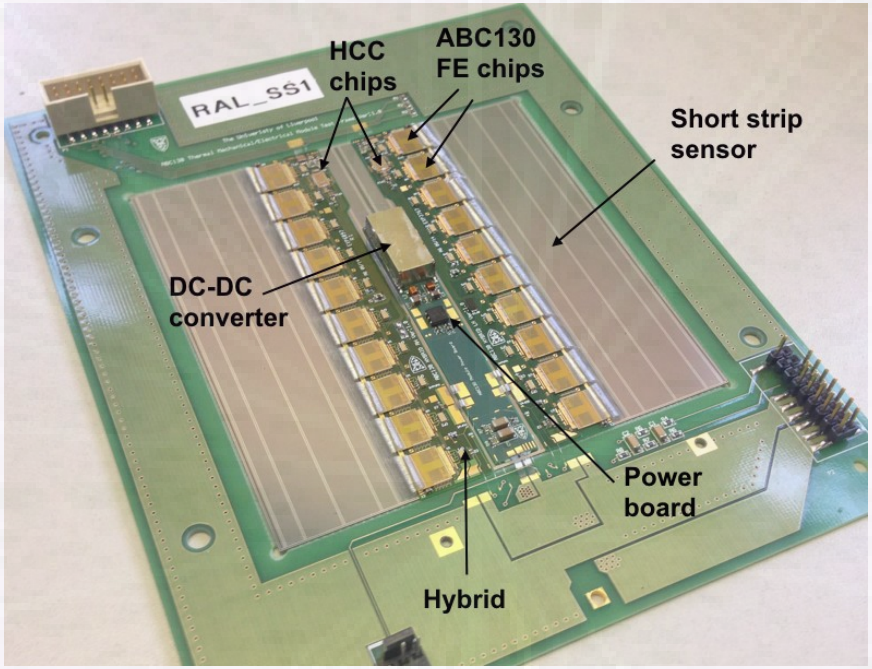
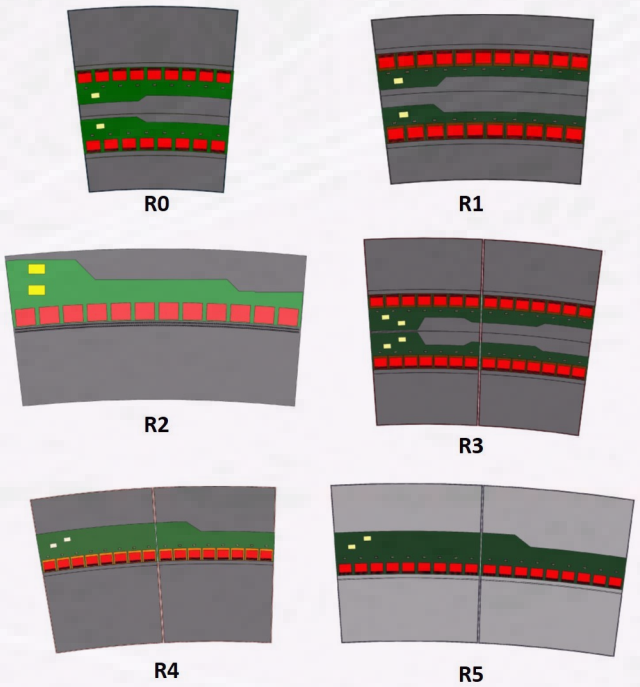


Photo of barrel strips module (mounted on test frame)

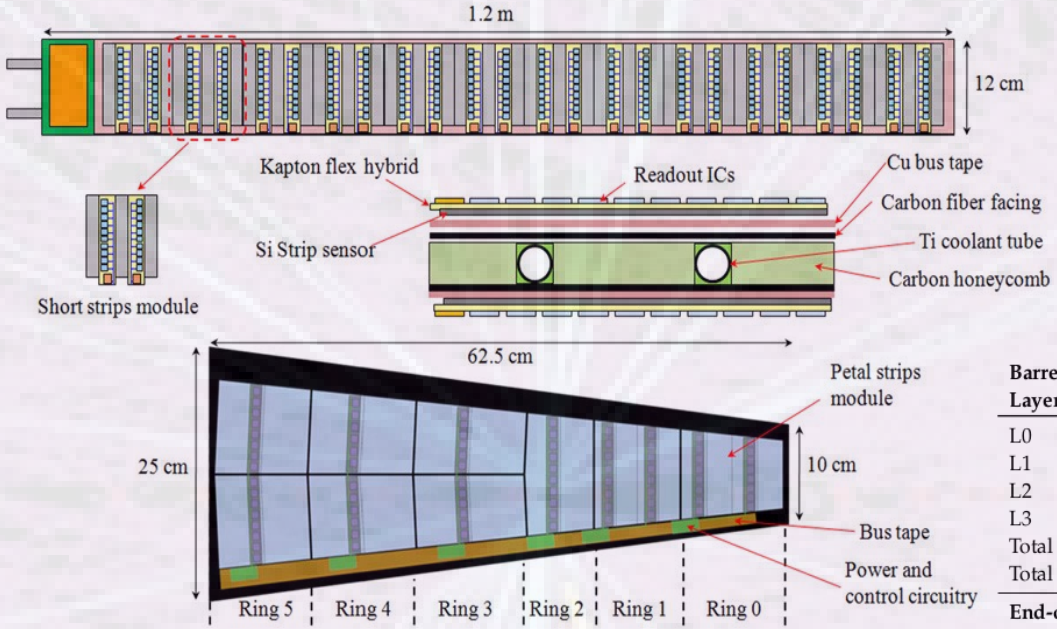


Diagrams of end-cap strip module configurations

- ABC = ATLAS Binary Chip: front-end readout ASICs
- ABC130 (and ABCN250) were earlier prototypes
- ABCStar will be the final version (prototypes due this year)

Image source: Technical Design Report for the ATLAS Inner Tracker Strip Detector, The ATLAS Collaboration, CERN-LHCC-2017-005, 2017.

ITk Strips Detector Components



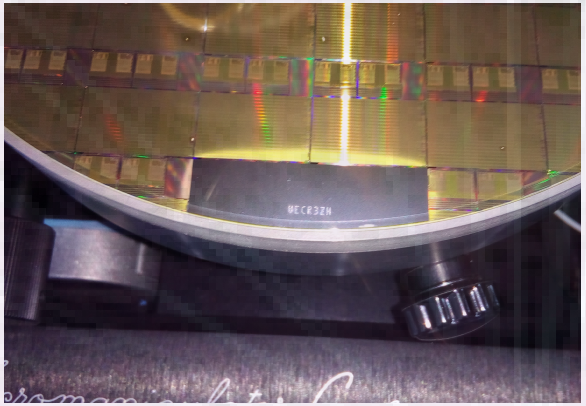
- Requires testing of ~700 dedicated ABCStar wafers

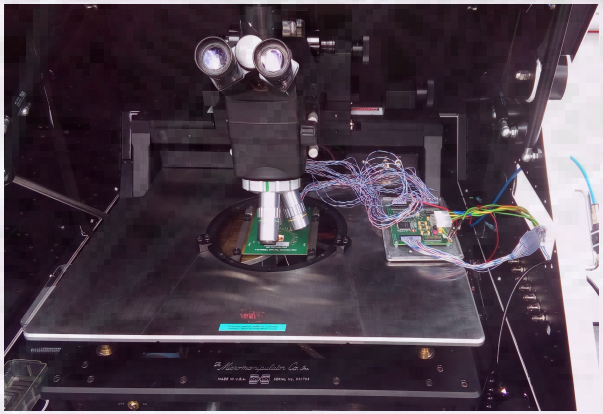
Barrel Layer:	Radius [mm]	# of staves	# of modules	# of hybrids	# of of ABCStar	# of channels	Area [m^2]
L0	405	28	784	1568	15680	4.01M	7.49
L1	562	40	1120	2240	22400	5.73M	10.7
L2	762	56	1568	1568	15680	4.01M	14.98
L3	1000	72	2016	2016	20160	5.16M	19.26
Total half barrel		196	5488	7392	73920	18.92M	52.43
Total barrel		392	10976	14784	147840	37.85M	104.86
End-cap Disk:	**z-pos. [mm]**	**# of petals**	**# of modules**	**# of hybrids**	**# of of ABCStar**	**# of channels**	**Area [m^2]**
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total one EC		192	3456	4992	43008	11.01M	30.2
Total ECs		384	6912	9984	86016	22.02M	60.4
Total		**776**	**17888**	**24768**	**233856**	**59.87M**	**165.25**

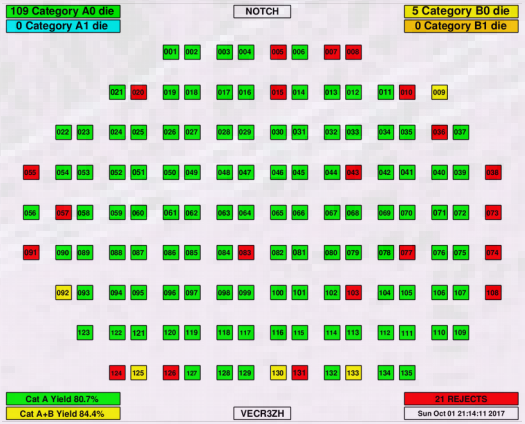
- ABCStar testing was going to need roughly 3 years!

Image source: Silicon strip staves and petals for the ATLAS Upgrade tracker of the HL-LHC, Sergio Dı´ez, NIM A 699 (2013) 93–96.
Table source: Technical Design Report for the ATLAS Inner Tracker Strip Detector, The ATLAS Collaboration, CERN-LHCC-2017-005, 2017.

ASIC Testing At RAL (UK)





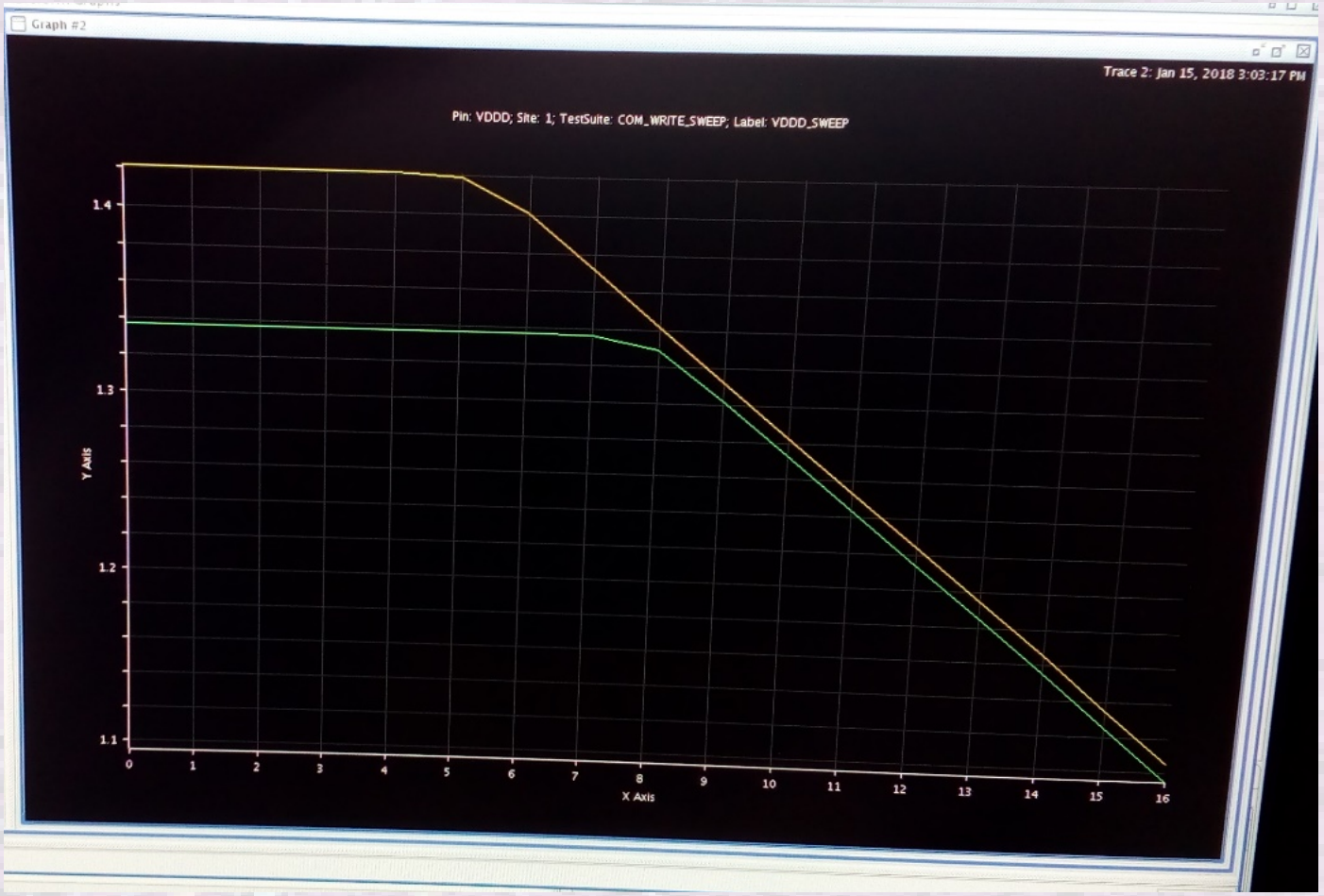


- Adapted DAQ software and firmware to test wafers
  - Repurposed existing Micromanipulator semi-automatic probe station to test wafers (much custom software)
  - Multi-year intensive R&D effort to develop system to characterize ABCN250 and ABC130 chips on wafers
  - Was only facility that could test the ITk wafers
  - Very hands-on process requiring expert operator
    - Necessary for R&D, but only one to a few wafers/day

Can Carleton Test ASICs As Well?

- Multiple sites highly desirable for front-end ASIC testing
  - Replicate probe station setup at RAL in the UK?
  - Go our own route (acquire equipment or outsource)?
- Acquired an old "Batch 1" ABC130 wafer from RAL
  - Initial design had metalization error: shorted transceiver
- Partnered with local company ***DA-Integrated***
  - Business model is to work with small/medium players
  - Design and manufacture probe card for ABC130
  - NRE contract to collaboratively implement test vectors
  - Test ABC130 wafers on industry standard wafer prober
  - Arrange with partner company to dice the tested wafer

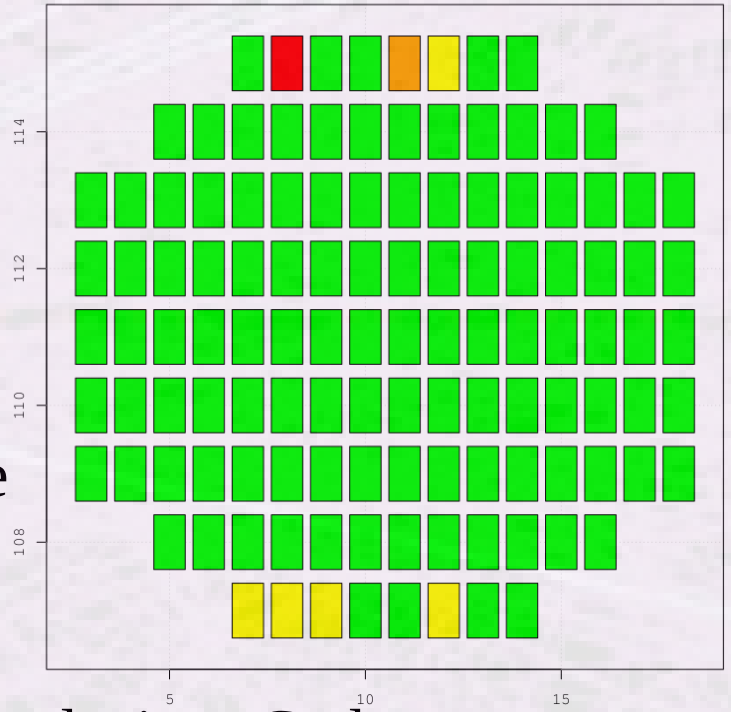
Short Answer: Yes!



First Data from ABC130! (photo of prober screen)

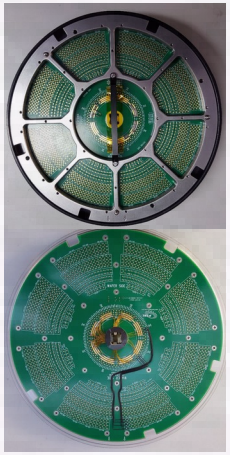
“Batch 1” Testing At Carleton

- Spent two weeks at RAL testing “Batch 4” ABC130 wafers
- Determine CMOS/SLVS interface requirements for ABC130
- Reverse engineer complex DAQ code
  - Written in C/C++/ROOT
  - On “Batch 1”, only the basic analog could be tested
  - Provided DA Integrated with test “cookbook”, they wrote code
  - Work collaboratively with their engineers to adapt/debug tests
  - Pass/fail on prober, offline data analysis at Carleton

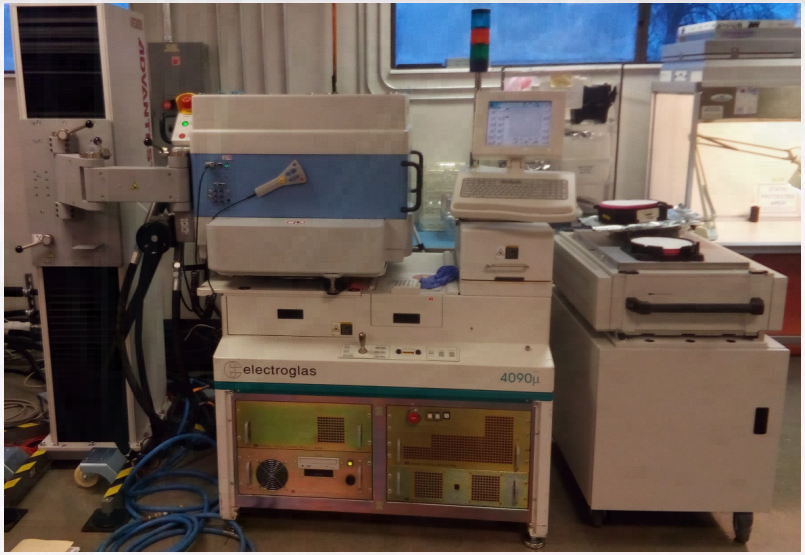


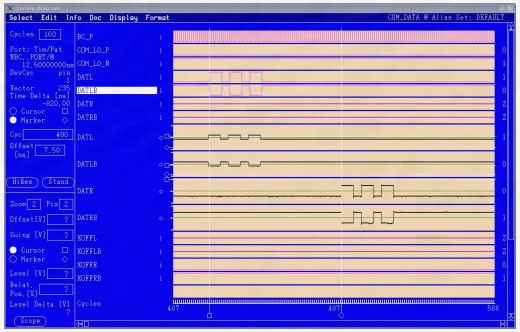
- Much to be learned to bridge physics/engineering domains

DA Integrated IC Wafer Prober



Semi-custom probe card for ABC130

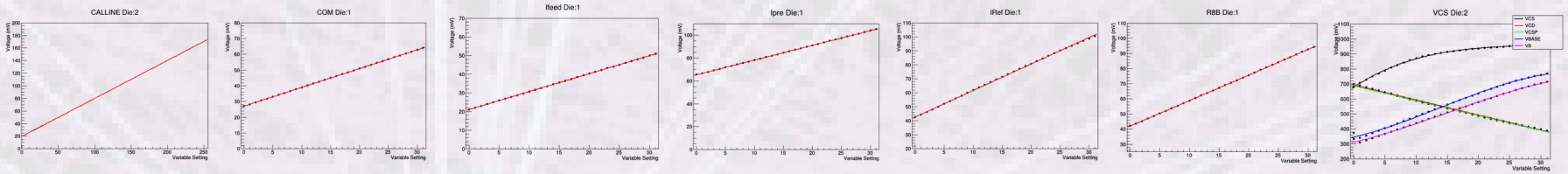




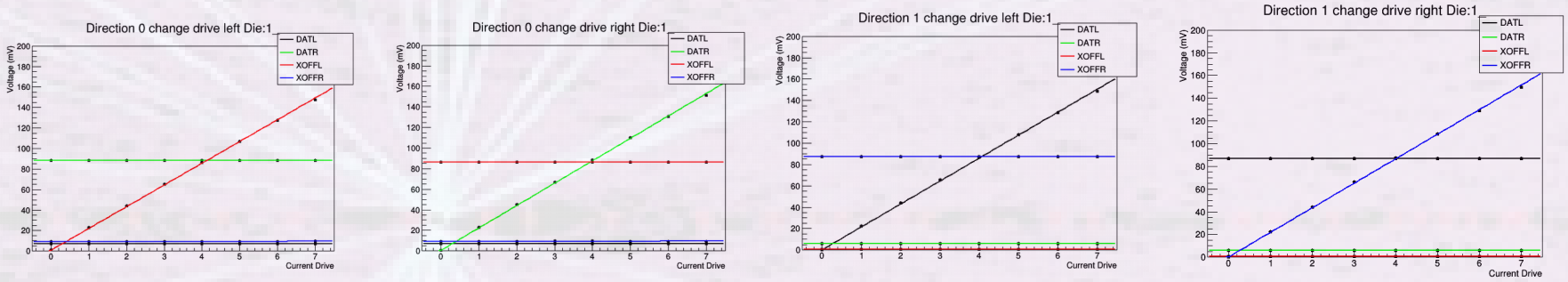
Test signal visualization tools built in to the tester software

- We are using their *Electroglas 4090μ* automated wafer prober
  - Can test a wafer of ABC130 chips in about 15 minutes
  - Can be programmed in C/C++ (used for analog tests)
  - Can run tests provided as binary pin stimulation vectors
  - Has sophisticated test debug/visualization tools
- Carleton is provided with a pass/fail wafer map and all measurements in a text file format (we wrote a parser)

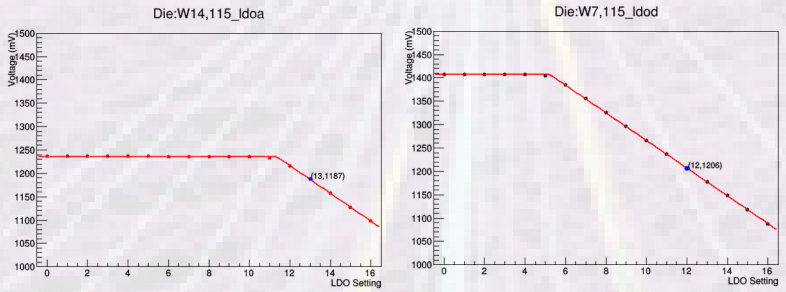
Example Data Analysis (Analog Tests)



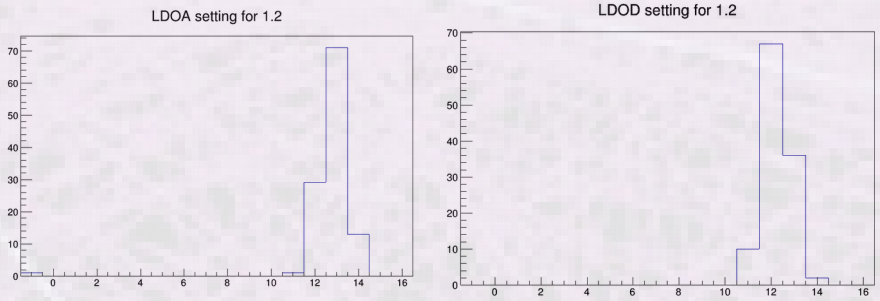
Sweeping D/A converters and reading the associated voltage on the Analog Multiplexer pin



SLVS output driver current sweep measurements (DATAL, DATAR, XOFFL, and XOFFR)



Individual LDOA and LDOD measurements



Distribution of LDO tuning parameters across entire wafer

“Batch 1” Dicing At Carleton

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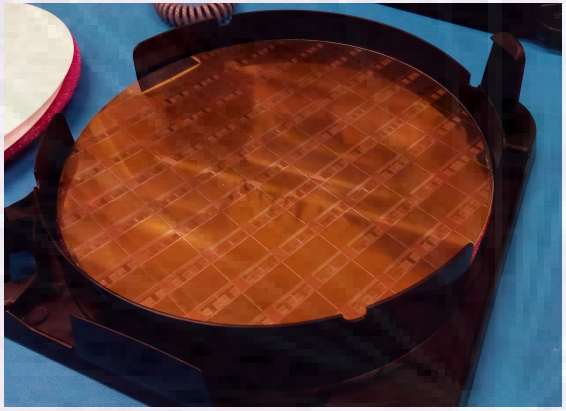
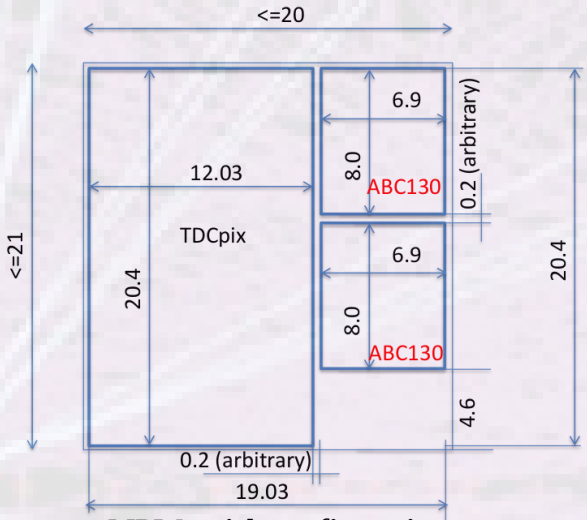


Intact “Batch 1” wafer at Carleton (wafer is 8 inches in diameter)



MPW reticle configuration

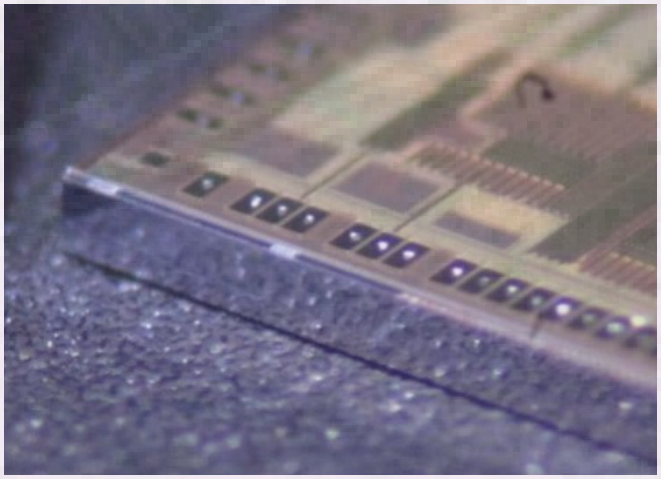


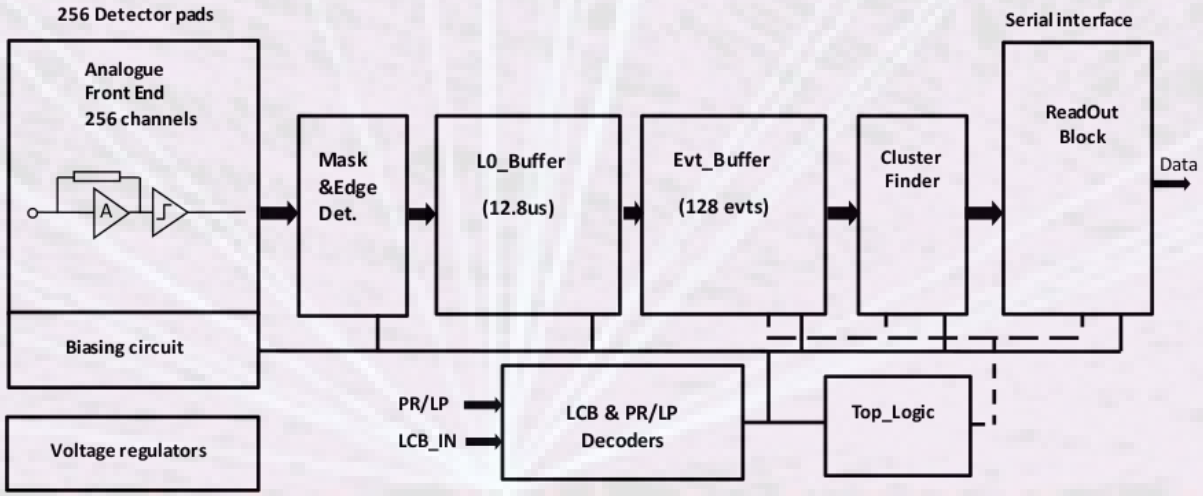
Photo of edge of diced ABC130 – no side cracks, bottom chipouts, or dicing facets!

- Great concern at CERN about dicing yield/different methods
- Wafer is pre-thinned to ~300µm and dicing partner was concerned about possible chipping and delamination
- Challenge due to Multi-Project Wafer (sacrificed TDCPix)
- Results were as good as or better than existing provider

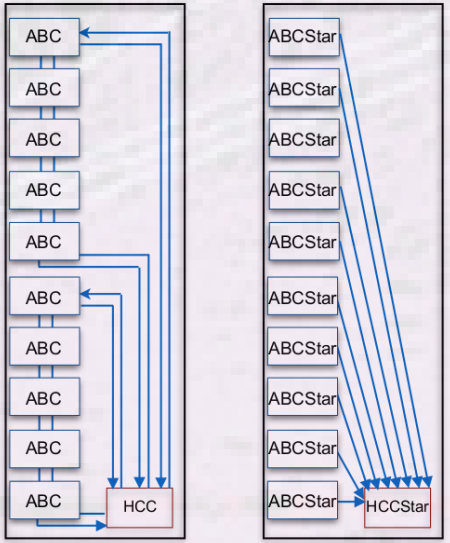
"Batch 4" Wafer Testing

- With success of "Batch 1" testing, Carleton received two "Batch 4" wafers (fully functional chips, tested at RAL)
- Need to communicate with all I/O pins to the chip now
  - Translate digital test vectors from coded format used by DAQ into binary 1/0 stimulation vector for prober
  - To determine output, use empirical test: send test vector, see what comes out (once), expect that every time
  - Some tests require pattern searching and field masking
- Successfully tested purely digital portion of chip 2 weeks ago
- Now working on test vectors for testing the ASIC front end
  - Back to reverse engineering DAQ – tests complex
  - Will likely provide "cookbook" to DA Integrated again

ABC130 vs. ABCStar



ABCStar chip architecture



Old daisy-chain vs. new star communications

- 160MHz point-to-point vs. 80/160MHz daisy-chain datapath
- Expect the first wafers to be available as early as August 2018
- Wafer includes ABCStar, HCCStar, AMAC, and unrelated chip
  - Multi-Project Wafer will present serious dicing challenge

Block diagram source: ATLAS ITk Electronics Specification: ABCStar, v7.66, 2018.
Interconnect diagram source: TDR for the ATLAS Inner Tracker Strip Detector, The ATLAS Collaboration, CERN-LHCC-2017-005, 2017.

Conclusion

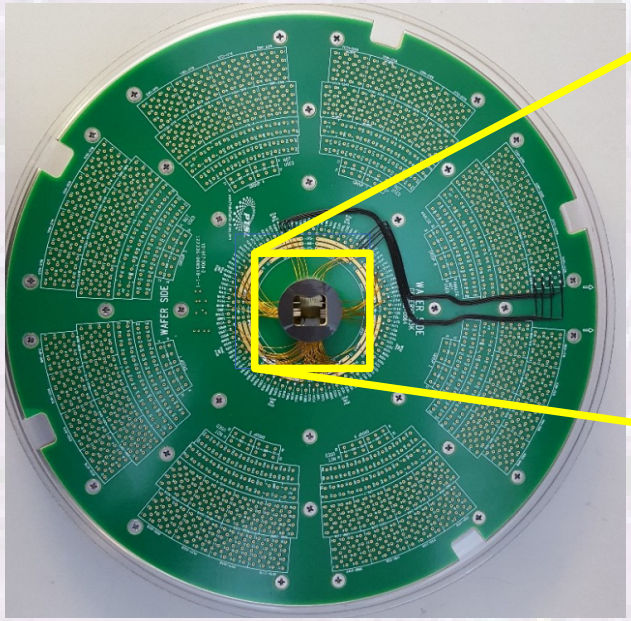
- Carleton has been able to expand its capabilities to include the testing and characterization of both silicon sensors for HEP and their associated readout and control ASICs
- In addition to sensor testing, the work we have done partnering with a commercial vendor of wafer test services and dicing may prove critical to timely completion of the ITk (testing all 700 wafers could be done in two to three months)
- We can now participate in this and future silicon-based detector development and testing, including custom chips for readout and communication, as we build the foundations needed to do R&D with these leading-edge technologies
- Through the expertise developed, exciting new opportunities for faculty and students at all levels are opened up

Questions?

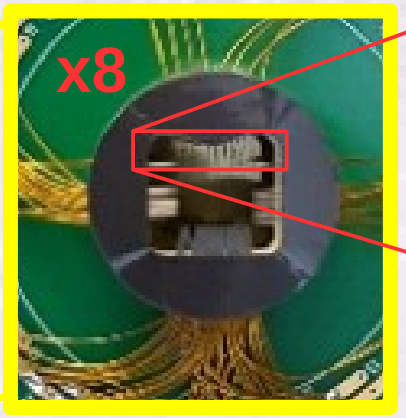
This work has been made possible by significant contributions by: Thomas Koffas, Dag Gillberg, John Keller, and Ezekiel Staats, *Carleton Dept. of Physics*; Steve McGarry, Rob Vandusen, and Garry Tarr, *Carleton Dept. of Electronics*; Peter Philips and Bruce Gallop, *Rutherford Appleton Laboratory*; Matt Warren, University College London; and Ingo Bloch, *Deutsches Elektronen-Synchrotron*, Zeuthen campus.

Background and title slide image source: ATLAS and CMS upgrade proceeds to the next stage, Contardo and Wells, CERN Courier, Jan 15, 2016.

External ASIC Front-End Testing

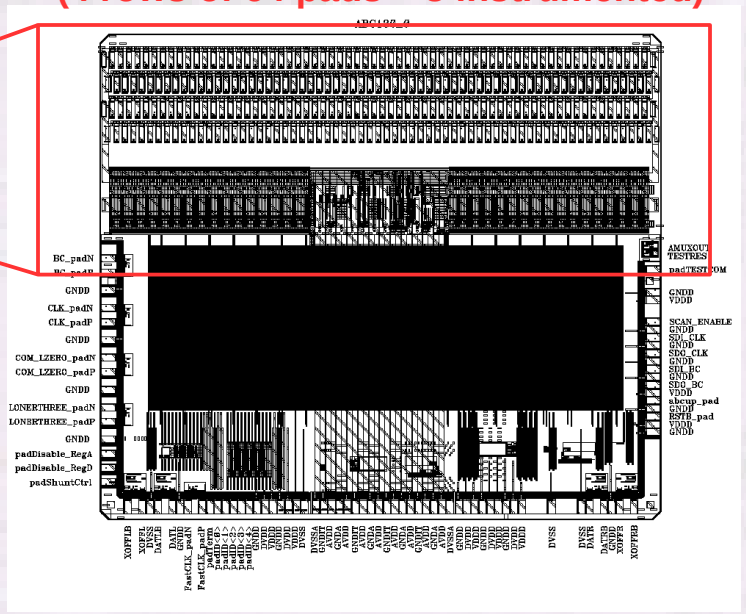


ABC130 Custom Probe Card



Cantilevered Probe Pins

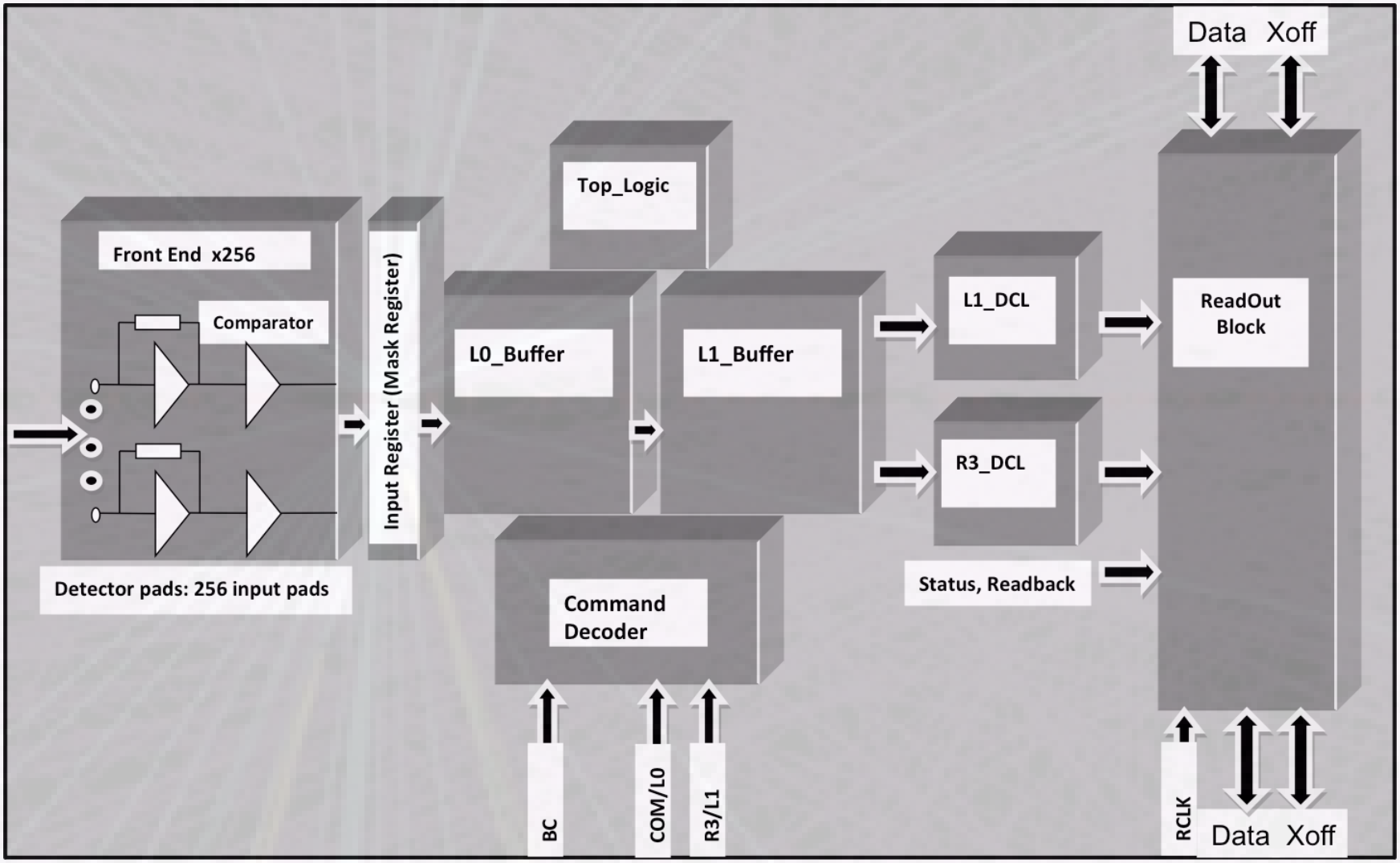
256 Analog Front-End Inputs
(4 rows of 64 pads – 8 instrumented)



ABC130 Pad Layout

- Introduced new feature: chose 8 representative front-end pads
  - Will use calibrated gated capacitor discharge as charge source (~fC)
- RAL concern: probe pins will disrupt self-test measurements
- Carleton goal: provide precision performance and calibration data

ABC130 Chip Architecture



Digital Test Vector Translation

```
# Read one thru packet from ABC130
#  7     DX3     Data Out 3      Scan SDI CLK
#  6     DX2     Data Out 2      Scan SDI BC
#  5     DX1     Data Out 1      Data/Xoff Right
#  4     DX0     Data Out 0      Data/Xoff Left
#  3     SP1     Spare 1        n/a
#  2     SP0     Spare 0         SCAN_EN
#  1     L1R3    L1 R3  L1R3
#  0     COML0   COM L0  COML0
#
# In raw mode, with DDR at 80MHz
42   0000
# Pattern on DATL 1010
6   1010
4   0000
6   1010
4   0000
6   1010
4   0000
160  0000
2  0000
```

Input: "ITSDAQ format" digital test vector

```
CLK_P,CLK_N,BC_P,BC_N,COM_L0_P,COM_L0_N,L1_R3_P,L1_R3_N,DATAL_P,DATAL_N,DATAR_P,DATAR_N,XOFFL_P,XOFFL_N,XOFFR_P,XOFFR_N
0,1,0,1,0,1,0,1,0,1,L,L,L,L,0,1
1,0,1,0,0,1,0,1,0,1,L,L,L,L,0,1
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0,1,1,0,0,1,0,1,0,1,L,L,L,L,0,1
1,0,0,1,0,1,0,1,0,1,L,L,L,L,0,1
0,1,0,1,0,1,0,1,0,1,L,L,L,L,0,1
1,0,1,0,0,1,0,1,0,1,L,L,L,L,0,1
0,1,1,0,0,1,0,1,0,1,L,L,L,L,0,1
1,0,0,1,0,1,0,1,0,1,L,L,L,L,0,1
0,1,0,1,0,1,0,1,0,1,L,L,L,L,0,1
1,0,1,0,0,1,0,1,0,1,L,L,L,L,0,1
0,1,1,0,0,1,0,1,0,1,L,L,L,L,0,1
1,0,0,1,0,1,0,1,0,1,L,L,L,L,0,1
0,1,0,1,0,1,0,1,0,1,L,L,L,L,0,1
1,0,1,0,0,1,0,1,0,1,L,L,L,L,0,1
0,1,1,0,0,1,0,1,0,1,L,L,L,L,0,1
1,0,0,1,0,1,0,1,0,1,L,L,L,L,0,1
0,1,0,1,0,1,0,1,0,1,L,L,L,L,0,1
1,0,1,0,0,1,0,1,0,1,L,L,L,L,0,1
0,1,1,0,0,1,0,1,0,1,L,L,L,L,0,1
1,0,0,1,0,1,0,1,0,1,L,L,L,L,0,1
0,1,0,1,0,1,0,1,0,1,L,L,L,L,0,1
1,0,1,0,0,1,0,1,0,1,L,L,L,L,0,1
0,1,1,0,0,1,0,1,0,1,L,L,L,L,0,1
1,0,0,1,0,1,0,1,0,1,L,L,L,L,0,1
```

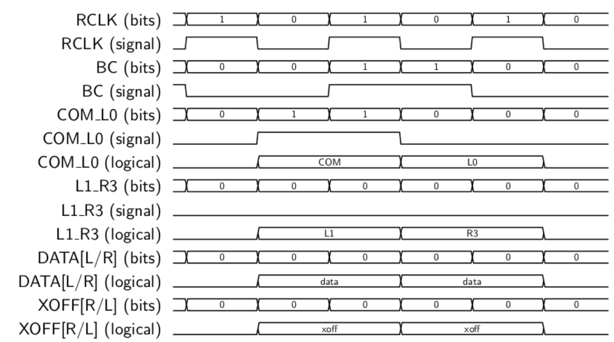

Worked with DA Integrated on "universal" pad stimulus vector structure and timing

Output: CSV format ASCII-coded binary pad stimulation vector for Electroglas

- *DA Integrated* cannot run RAL DAQ system, so Carleton must decipher it and specify "raw" bit-level coding for use in their IC prober system

```
00001: COM command start detected.
00008: issued Soft Reset command
00011: COM command start detected.
00068: issued ABC command: HCC ID = 31, ABC ID = 31,
          Reg Addr = 0x20, R/W = write, Data = 0x00000410.
00070: COM command start detected.
00127: issued ABC command: HCC ID = 31, ABC ID = 31
          Reg Addr = 0x22, R/W = write, Data = 0x000000FF.
00264: issued L0 trigger
00271: L1 trigger start detected.
00281: issued L1 trigger: L0ID = 0x0000.
00282: issued L0 trigger
00289: L1 trigger start detected.
00299: issued L1 trigger: L0ID = 0x0001.
00300: issued L0 trigger
00307: L1 trigger start detected.
00317: issued L1 trigger: L0ID = 0x0002.
00318: issued L0 trigger
```

Wrote software to provide human-readable "disassembly" of ABC130 bit streams