Upgrade of the ATLAS Thin Gap Chamber Electronics for HL-LHC

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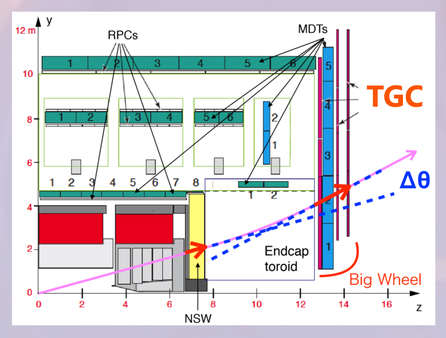
Introduction

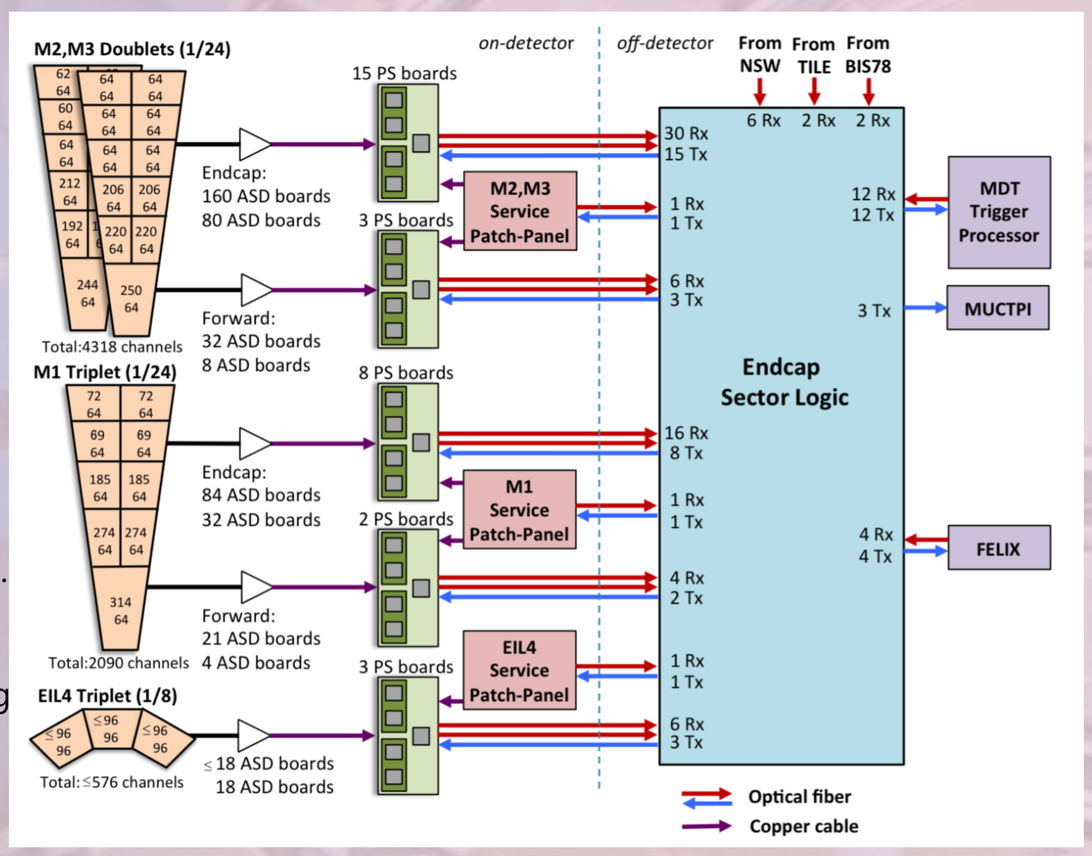
High-Luminosity LHC (HL-LHC) [1] is planned to start the operation in 2026 with instantaneous luminosity of $7.5 \times 10^{34}\ \mathrm{cm^{-2}s^{-1}}$. To cope with proton-proton collision rate higher than LHC, the trigger and readout electronics of ATLAS Thin Gap Chamber (TGC) [2] will be replaced. In the new trigger system, all TGC hit data are transferred from frontend to backend boards and exploited by advanced first-level muon trigger based on a fast tracking [3,4].

TGC electronics for HL-LHC

TGC: multi-wire proportional chamber at endcap (pseudorapidity η range $1.05 - 2.4$) of the ATLAS muon detector.
- Measures two-dimensional position using signals from wires and strips orthogonal to the wires.
- Consists of three stations. Station M1 has three layers. M2 and M3 have two layers, respectively.



The original trigger is based on simple coincidence logic in the frontend boards and transverse momentum (p_{T}) evaluation with look-up tables in the backend boards. The new trigger evaluates p_{T} in the backend boards from the angle difference **$\Delta\theta$** using TGC segments reconstructed from all TGC hits transferred by the frontend board.

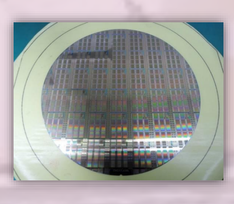


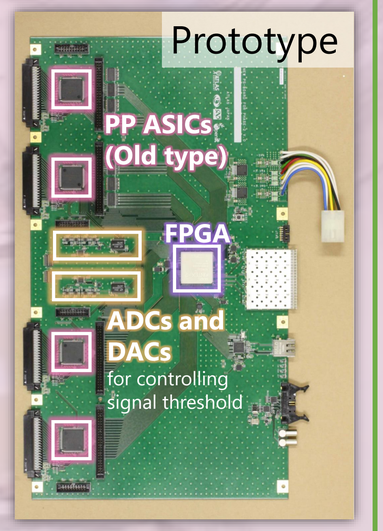
Frontend: PS board

- Hit timing alignment by Patch-Panel (PP) ASICs
- Hit data transfer at 16 Gbps and ADC/DAC control by FPGA

PS board prototype has full functions for HL-LHC.

Mass production of new PP ASICs in 2019.





Backend: Endcap Sector Logic (SL)

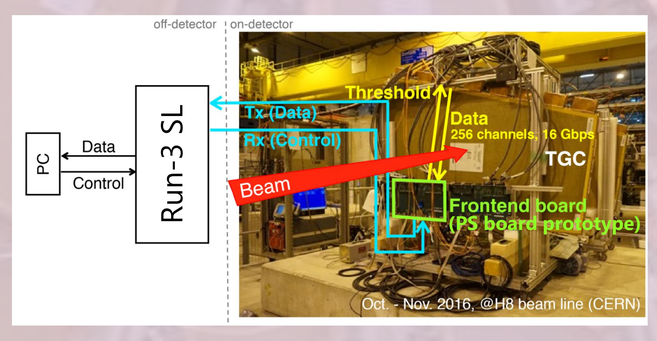
- Trigger process, e.g. TGC segment reconstruction
- Data readout

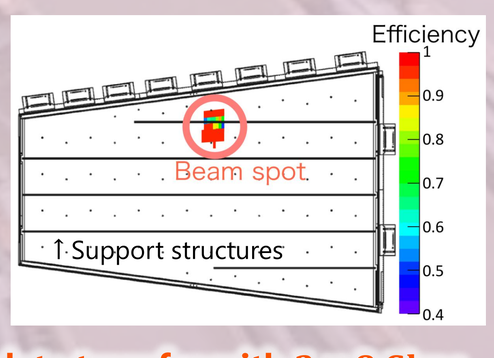
SL communicates with electronics of various detectors. Main functions of SL is implemented on one FPGA. The Virtex UltraScale(+) FPGAs provided Xilinx [5] are assumed for the FPGA on SL.

Demonstration with PS board prototype

Functions of FPGA on PS board have been tested with beams.

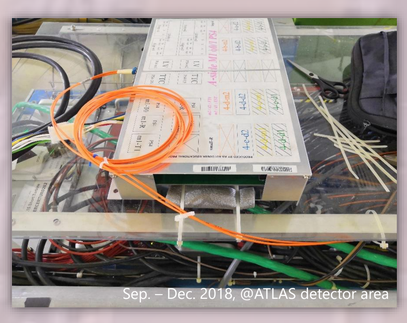
➢ Full TGC readout chain

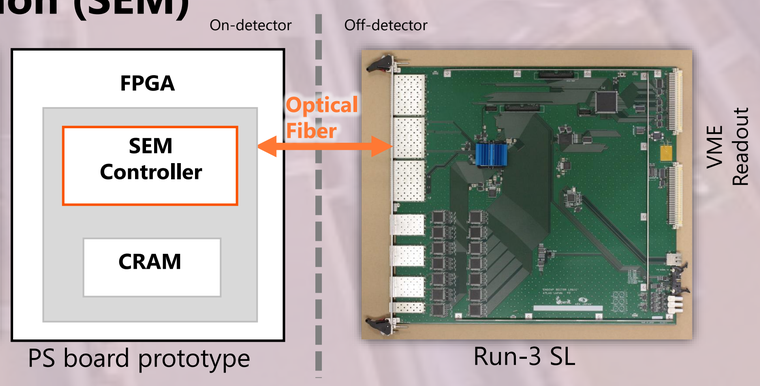




- **PS board prototype provided stable data transfer with 2×8 Gbps.**
- The validity of the transferred data has been confirmed by evaluating the efficiency for each channel.
- Signal threshold control based on FPGA has been demonstrated.

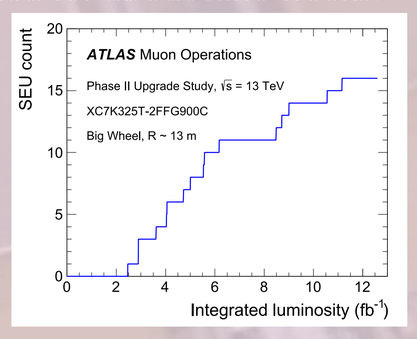
➢ Soft Error Mitigation (SEM)





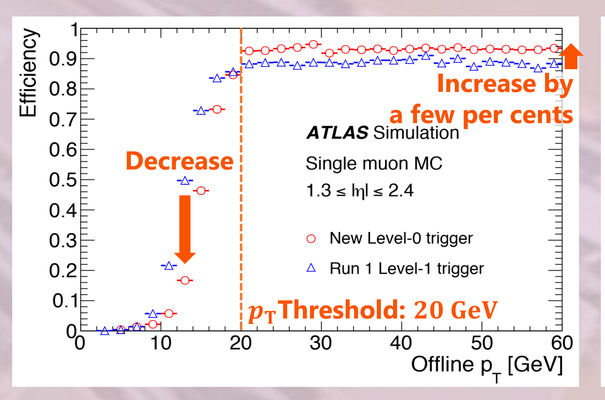
A PS board prototype was installed on the top of TGC about 13 m away from the beam axis. SEM demonstration was performed for about nine weeks.

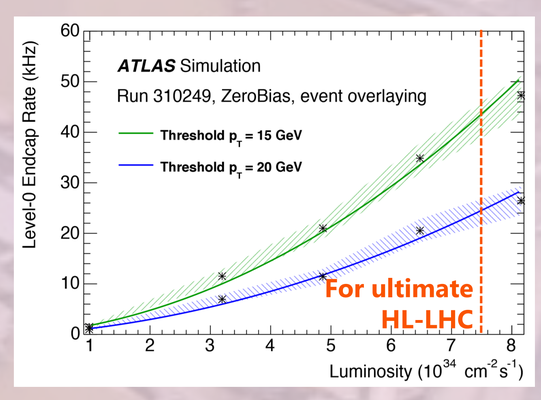
16 Single Event Upsets (SEUs) have been found on one Kintex-7 FPGA of PS board prototype in operation of $12.6\ \mathrm{fb^{-1}}$.
- All SEUs were one bit errors.
- **All errors were automatically corrected** by the SEM controller [6].
- No GTX communication error was observed.



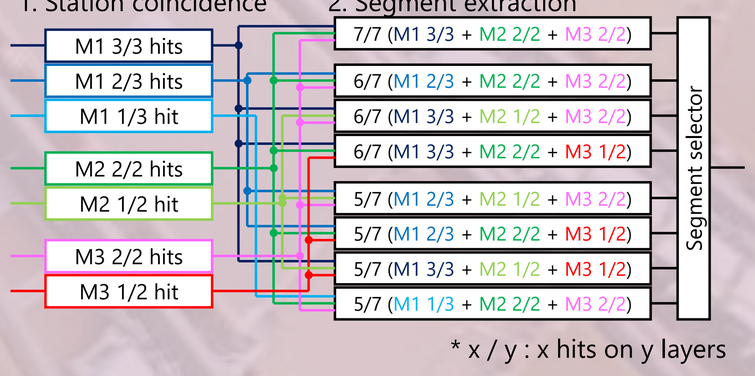
TGC segment reconstruction

Segment reconstruction with a pattern matching is under study [4].
- The new algorithm has been studied with MC and data samples.





However, the channel list used in the performance studies cannot be implemented on an FPGA because of its huge size. Therefore TGC segment reconstruction based on **two-step pattern matching** is proposed.



* x / y : x hits on y layers

The Diagram is shown for wires. Similar logic is assumed for strips.
- The list implemented on RAMs is used in the second step.
- Majority of memory resources will be spend by the list.

The resource estimation is an R&D item. Preliminary estimation of the list size per SL is **about one-third of 345.9 Mb of a RAM resource** on the baseline Virtex UltraScale+ FPGA.
The demonstration with an FPGA on an evaluation board is proceeding.

Conclusion

Hardware development of the ATLAS TGC electronics for HL-LHC is ongoing. The PS board prototype has been successfully demonstrated. The tracking trigger with pattern matching algorithm is expected to improve the endcap trigger performance.

Reference

[1] G. Apollinari, I. Bejar Alonso, O. Bruning, P. Fessia, M. Lamont, L. Rossi and L.Tavian, *High-Luminosity Large Hadron Collider (HL-LHC) : Technical Design Report V. 0.1*, CERN-2017-007-M.
[2] The ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST 3 (2008) S08003.
[3] The ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*, CERN-LHCC-2017-017.
[4] The ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ system*, CERN-LHCC-2017-020.
[5] Xilinx Inc., https://www.Xilinx.com/ (accessed on April 25th, 2019).
[6] Xilinx Inc., *Soft Error Mitigation Controller v4.1 LogiCORE IP Production Guide*, PG036 April 4, 2018.