Electronics for HL

The validity of the transferred data has been confirmed by evaluating expected hit data transfer at the ATLAS for tracking matching trigger. Consists of three stations. Station M1 has three layers. M2 and M3 have two layers, respectively.

PS board prototype provided stable data transfer with is Off with is proposed (is under study [4]. using matching PS cm All errors were automatically corrected Data readout. The Trigger process, e.g. TGC segment reconstruction Full TGC readout chain The list implemented electronics been been on an FPGA because of its huge size. Therefore TGC segment reconstruction based on two-step pattern matching is proposed. However, the channel list used in the performance studies cannot be implemented on an FPGA because of its huge size. Therefore TGC segment reconstruction based on two-step pattern matching is proposed. The Diagram is shown for wires. Similar logic is assumed for strips. - The list implemented on RAMs is used in the second step. - Majority of memory resources will be spend by the list. The resource estimation is an R&D item. Preliminary estimation of the list size per SL is about one-third of 345.9 Mb of a RAM resource on the baseline Virtex UltraScale+ FPGA. The demonstration with an FPGA on an evaluation board is proceeding.

Conclusion

Hardware development of the ATLAS TGC electronics for HL-LHC is ongoing. The PS board prototype has been successfully demonstrated. The tracking trigger with pattern matching algorithm is expected to improve the endcap trigger performance.

Reference