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Upgrade of the ATLAS Thin Gap Chamber Electronics for HL-LHC

The High-Luminosity LHC (HL-LHC) is planned to start the operation in 2026 with an instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. In order to cope with the event rate higher than that of LHC, the trigger and readout electronics of ATLAS Thin Gap Chamber (TGC) will need to be replaced. All hit data will be transferred from the frontend to the backend boards and exploited by an advanced first-level muon trigger based on a fast tracking. First prototype of the frontend board has been developed with full functions required for HL-LHC including the data transfer of 256 channels with a 16 Gbps bandwidth and the control of the discriminator threshold. They have been demonstrated at the CERN SPS beam facility. The rate of single event upset in Kintex-7 FPGA integrated on the prototype board was measured in the ATLAS detector area, and automatic error correction was demonstrated. Fast tracking algorithm has been emulated in the data taken by ATLAS. The result indicates that the advanced trigger based on fast tracking reduces the event rate by 30% while increasing the efficiency by a few percent. Test firmware was developed and the performance of fast tracking was evaluated with Virtex UltraScale+ FPGA evaluation kit. These studies provide essential ingredients in the development of ATLAS TGC electronics for HL-LHC

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