ALICE CENTRAL TRIGGGER SYSTEM FOR LHC RUN 3

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INTRODUCTION

- ALICE (A Large Ion Collider Experiment) is dedicated to the study of strongly interacting matter. In LHC Run 3 ALICE will able to collect > 10 nb^{-1} of Pb-Pb at luminosities up to 6 x 10^{27} cm^{-2} s^{-1} corresponding to collision rates of 50 kHz. ALICE will be able to operate in pp and p-Pb collisions with interaction rates up to 200 kHz.

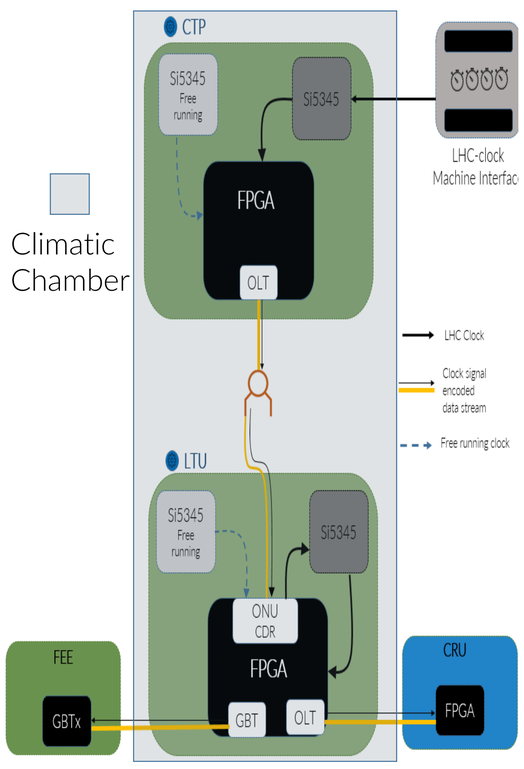
STRATEGY

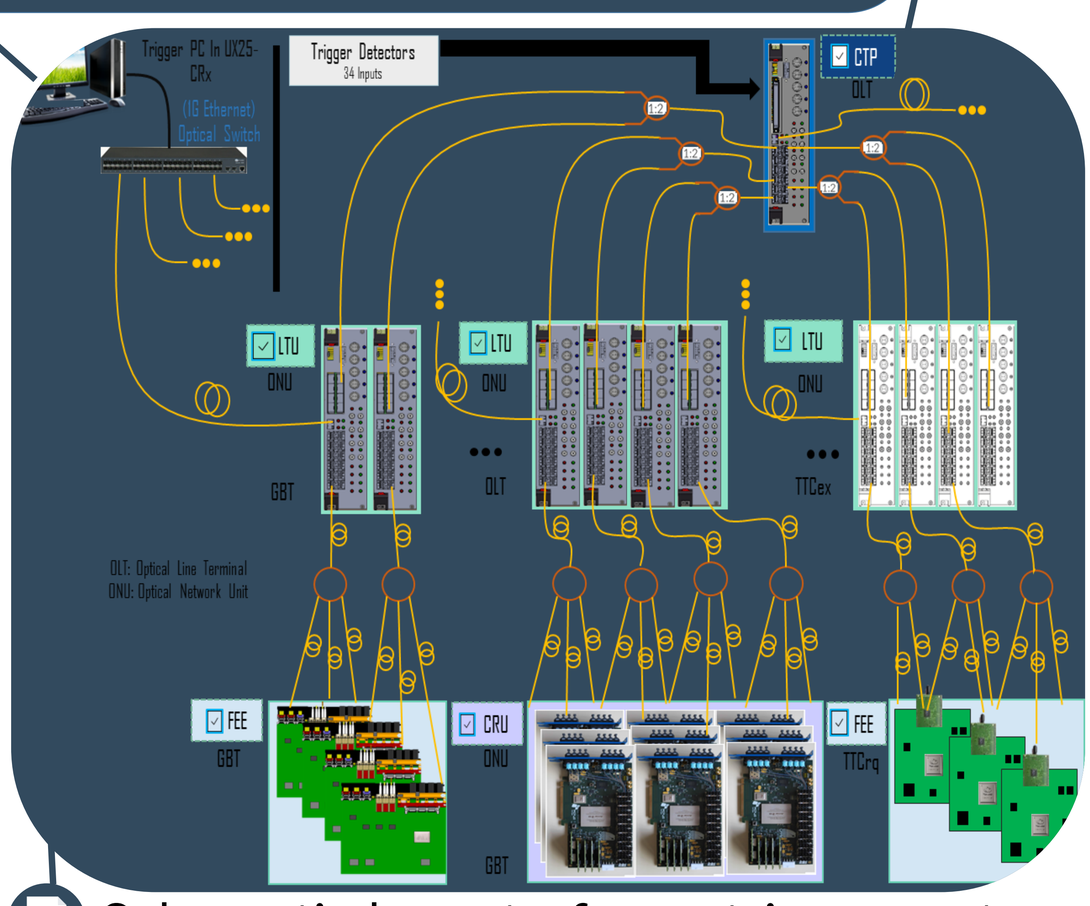
- The ALICE Upgrade will require a very different triggering strategy in comparison to the current and hence a new Central Trigger System (CTS) is needed. The central trigger processor (CTP) will be upgraded to accommodate the higher interaction rate, providing trigger and timing distribution (TTS) to the upgraded detectors and backwards compatibility to detectors not upgrading their TTS interface.

UPGRADE ALICE CENTRAL TRIGGER SYSTEM

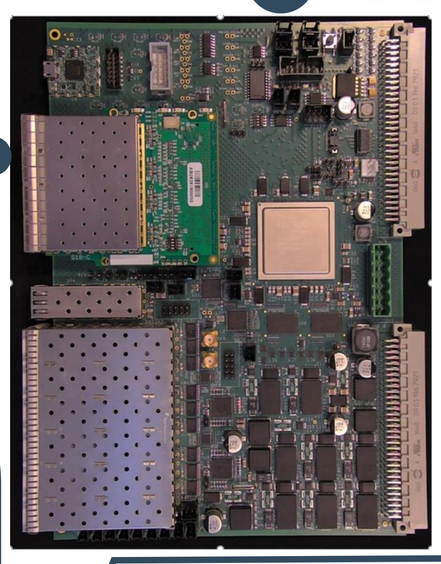
- The CTS will keep the previous architecture, a **Central Trigger Processor (CTP)** and **Local Trigger Units (LTUs)** as detector interface, the heart of the CTS will be an universal trigger board called **ALICE Trigger Board (ATB)** based on **Kintex UltraScale FPGA**, and the implementation of a novel **Timing Trigger Control** system based on Passive Optical Networks (TTC-PON).

Evaluation of the TTC-PON system





Schematic layout of new trigger system



ALICE Trigger Challenges

Select different physics

>> Different trigger detectors
--- (ACO, FIT, EMC, PHOS, TOF, ZDC).
>> Triggerless mode – offline physics selection.

Optimize for different running scenarios

>> pp, pA , AA collisions, with different interaction rates

Optimize use of detectors with

>> Widely different busy times.
>> Different latency times.
>> Different Technologies (TTC, GBT, TTC-PON)

Special triggers

>> Calibration, Control, debugging..

BUSY handling

>>BUSY for old detectors propagated over LVDS of TTC-PON upstream (TRD).
>> BUSY for upgraded detectors replaced by throttling mechanism

Available interfaces.

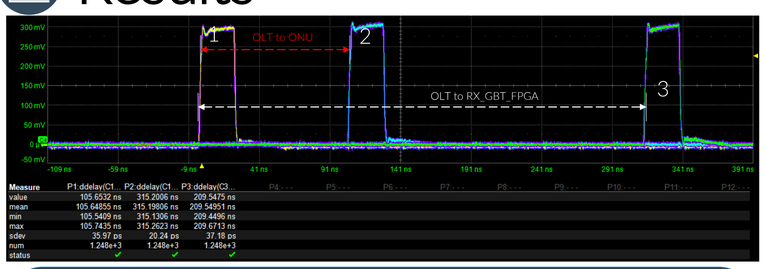
-- USB-JTAG
-- IPbus
-- DDR4
-- TTC-PON
-- TTC
-- GBT (LAT-OPT)
-- I2C
-- SPI

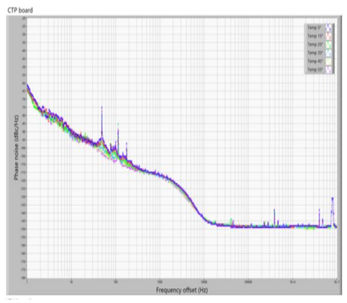
ALICE Trigger Board (ATB)

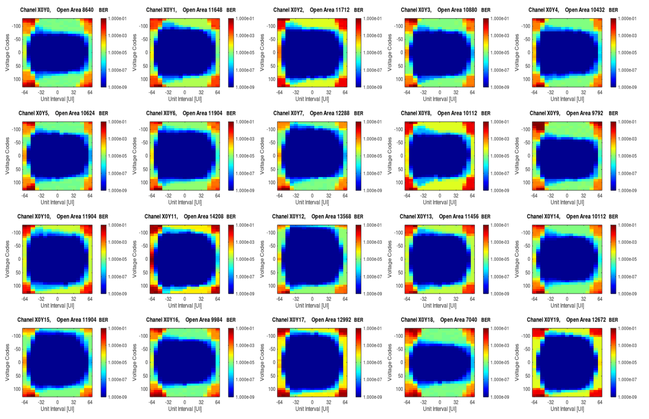
- The design is based around a single universal trigger board (CTP/LTU board).
- Is still based on a VME –Type 6u board (VME for power only)
- 20 Layers (I-TERA MT40 material)
  All clock paths have the same length.
- It Provides also high quality clock through SMA Outputs.

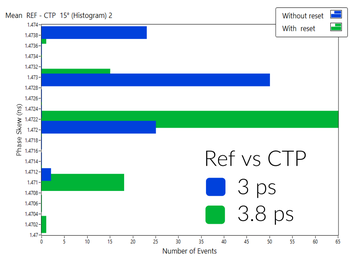
Schematic layout of new trigger system

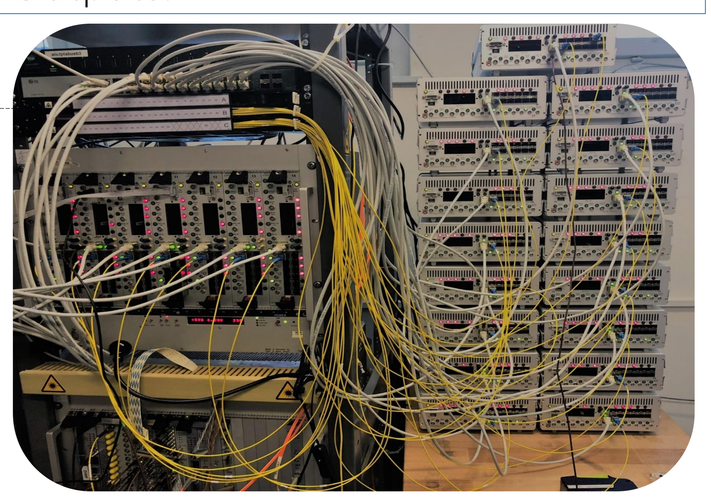
Results











Extensive Tests on 25 ATBs

TTC-PON on ATBs showed an excellent performance over temperature variations. Excellent phase stability over reset and power cycle processes.

Excellent eye aperture in all 20 High speed channels running up to 10 GHz.

Summary

A major upgrade of the ALICE experiment is in progress. A different trigger strategy will be employed by the new trigger system (CTS) . The main features of the new CTS are based on a new electronic trigger board (ATB) and the novel trigger timing system TTC-PON. Twenty five ATBs, together with TTC-PON and GBT have been extensively tested and showed an excellent performance.

References.

[1] E.Mendes. "The 10G TTC-PON: Challenges, solutions and performance". TWEPP, vol 1, 2017
[2] M. Krivda The ALICE central trigger processor upgrade , Jinst vol 1, 2017