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Readiness of the ATLAS Tile Calorimeter link daughterboard for the High Luminosity LHC era

The Phase-II upgrade plan for the ATLAS Tile Calorimeter facing the High Luminosity LHC (HL-LHC) era includes approximately 1024 radiation-tolerant readout link and control boards (Daughterboards) that will provide full granularity digital data to a fully-digital trigger system off-detector through multi-Gbps optic fibers. The Daughterboard design minimises radiation-induced errors and enhances data reliability by: embracing a fully double redundant design, using CERN radiation hard GBTx ASICs and Kintex Ultrascale+ FPGAs, implementing Triple Mode Redundancy in the FPGA firmware, and using CRC error verification in the redundant uplinks while FEC is handled by the each GBTx in each downlink. We have performed TID, NIEL and SEE radiation tests in order assess the the radiation tolerance strategies followed in the design and to qualify the Daughterboard for the HL-LHC requirements according to the ATLAS policy on radiation tolerant electronics. Over the HL-LHC lifetime, the Daughterboard positioned on the most radiation exposed area will have to withstand 23.57 kRad of Total Ionising Dose, a total Non-Ionising Energy Loss corresponding to 1.12655xE12 - 1 MeV equivalent neutron fluence, and seamlessly run and recover from any single event upset and single event latch-up for a fluence of 1.35987 E11 protons per cm2.

We present the current results of these tests, aiming to demonstrate the readiness of the Daughterboard to withstand the radiation requirements imposed by the HL-LHC.

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