ALICE LS3 Upgrade

A Fully Cylindrical Inner Tracking System

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For the ALICE Collaboration

7th Annual Conference on LHC Physics

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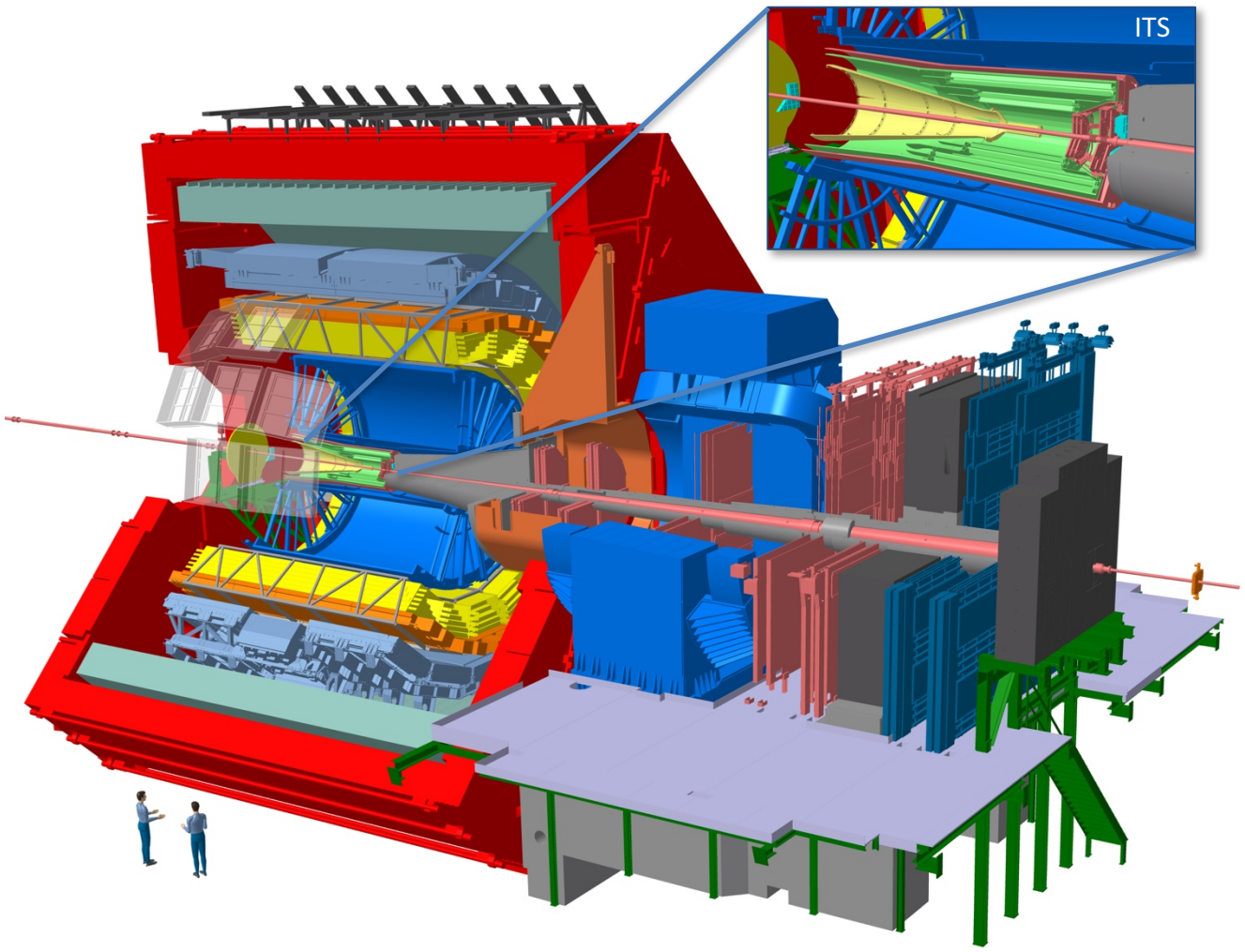
ITS Upgrade in LS2 (ITS2)



Motivations and goals:

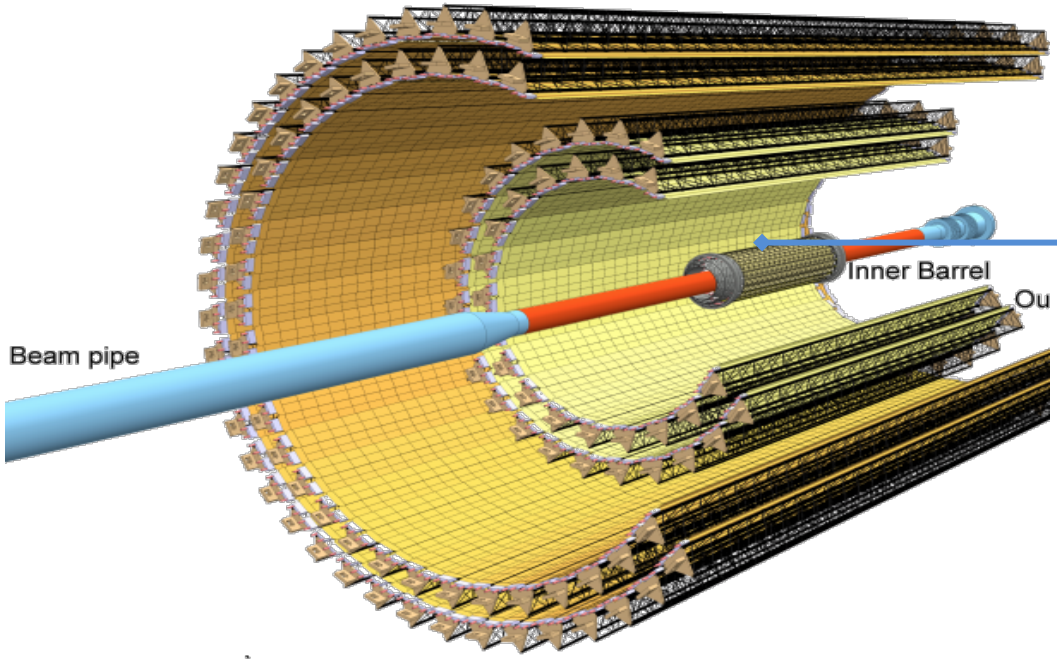
- Improved tracking precision
  smaller pixels, closer to IP, less material
- Faster readout

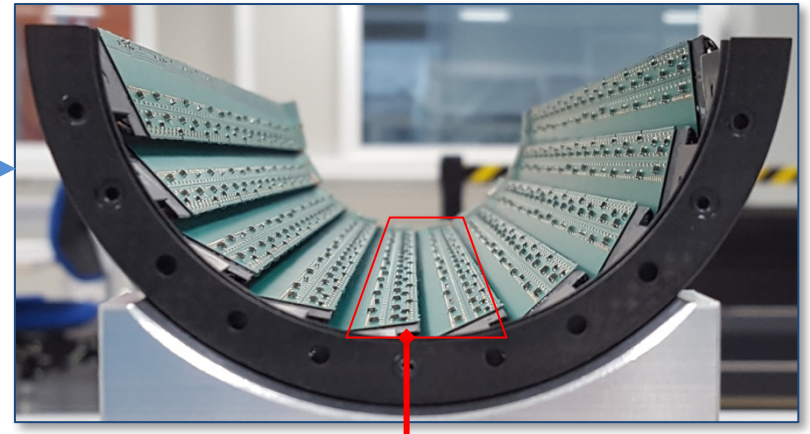
Based on novel CMOS Pixel Sensor (ALPIDE)

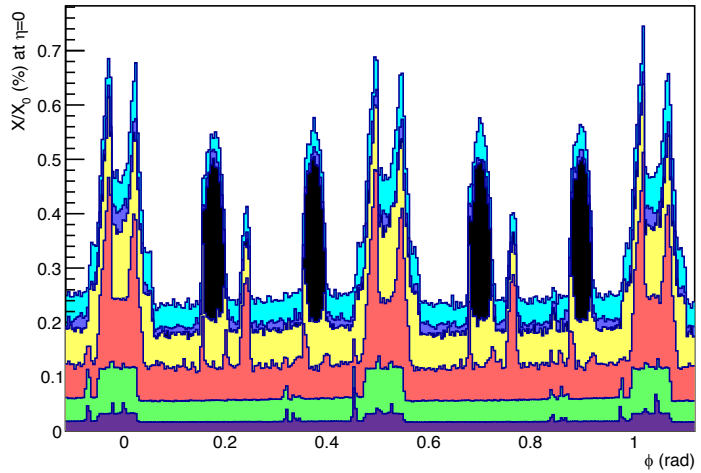
- 10 m^2 active area (12.5 G-Pixels)
- Spatial resolution ~5µm
- Power density < 40mW/cm^2
- Max. particle rate ~ 100 MHz/cm^2
- Max readout rate ~ 10 MHz/cm^2

cf. contribution by Jaime Norman:
*"ALICE LS2 Upgrade –
commissioning and Physics Projection"*

ALICE ITS2 Layout







7 cylindrical barrel layers with very low material budget

- 4 Outer barrel layers 0.8% X_0 / layer
- 3 Inner barrel layers with 0.35% X_0 / layer

But: Silicon only 15% of total material,
active silicon thickness ~20μm = 0.02% X_0

-> Can we do better?

ALICE ITS2 – Material Budget

"Non-sensing" contributions to material budget:

- Mechanical support for individual staves
- Active cooling
- Flex printed circuit to route signal and power to individual sensor chips

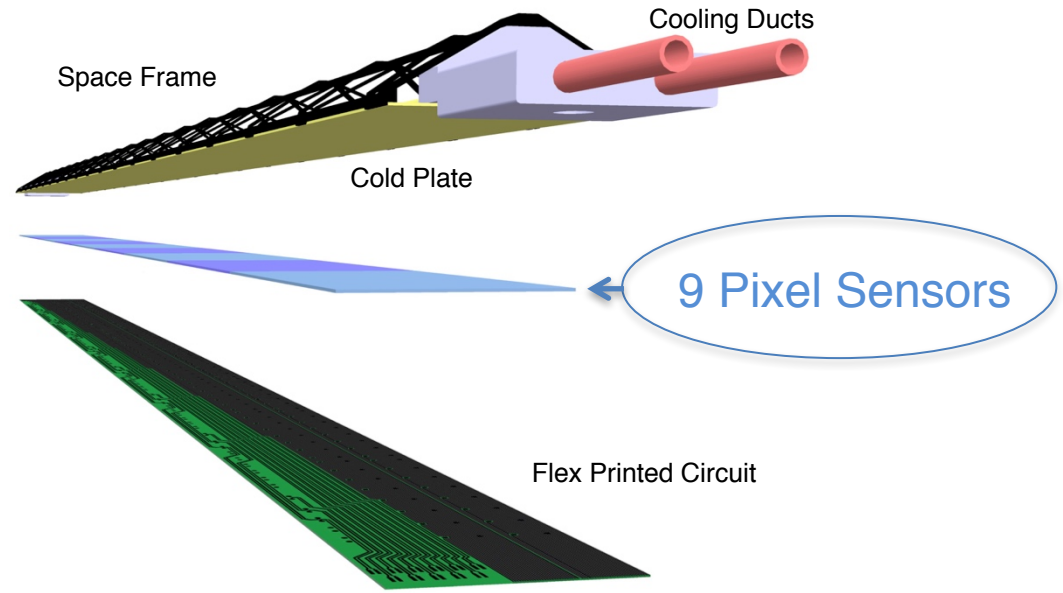
Active cooling could be replaced by air flow for power dissipations below ~20 mW/cm^2

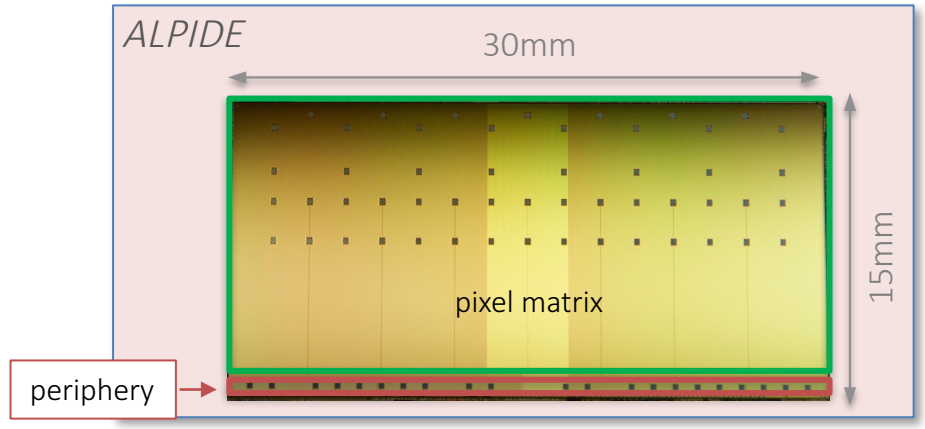
- ALPIDE: the matrix power dissipation is ~7mW/cm^2
- The rest (~33mW/cm^2) is dissipated by the peripheral circuitry

Can we move this peripheral circuitry to the periphery of the detector?

This would require a sensor of the full stave length

- Eliminates also the need for an external routing layer (Flex printed circuit)



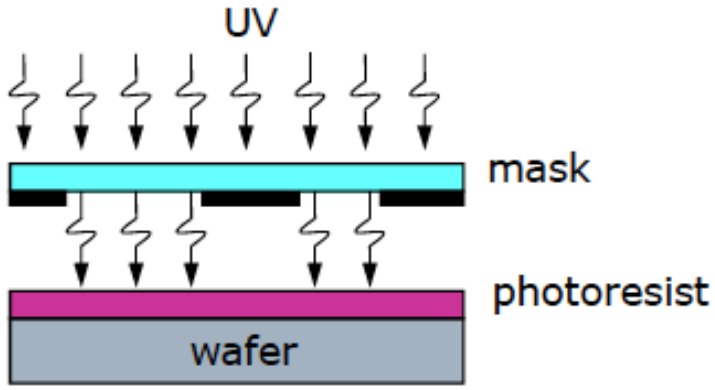


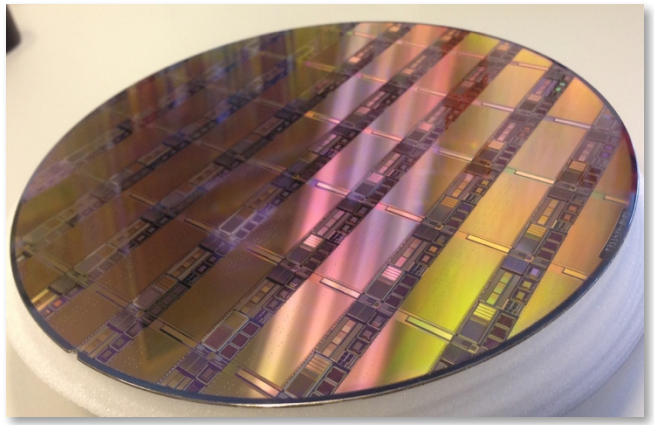
Stitching

CMOS photolithographic process defines wafer reticles size

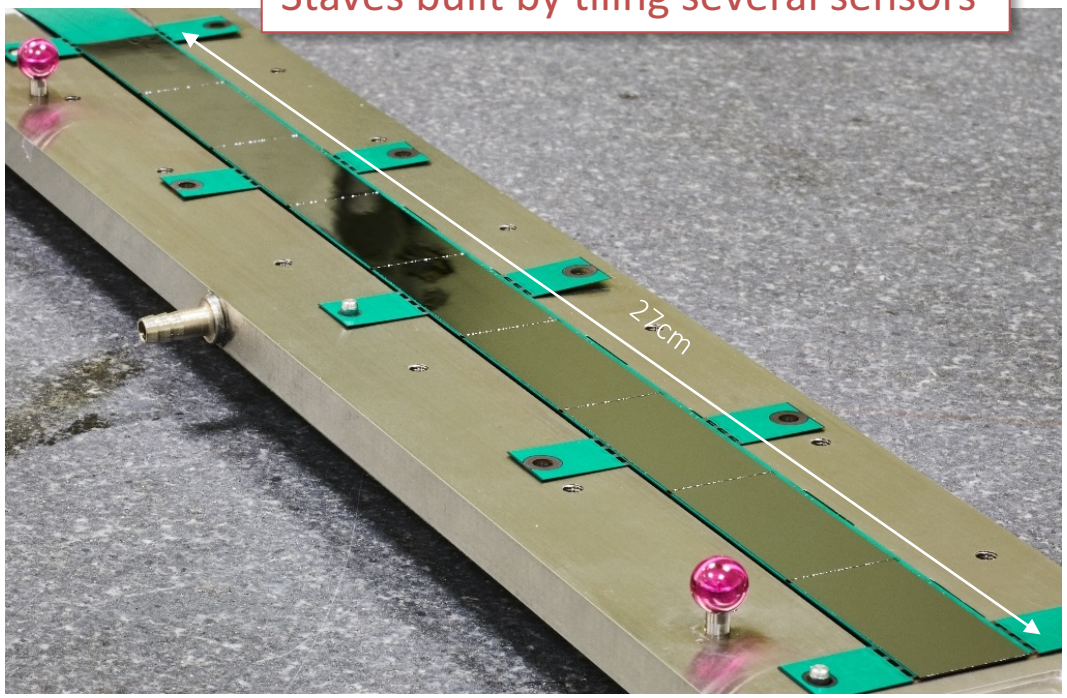
⇨ Typical field of view O(2 x 2 cm^2)

Reticle is stepped across the wafers to create multiple identical images of the circuit(s)

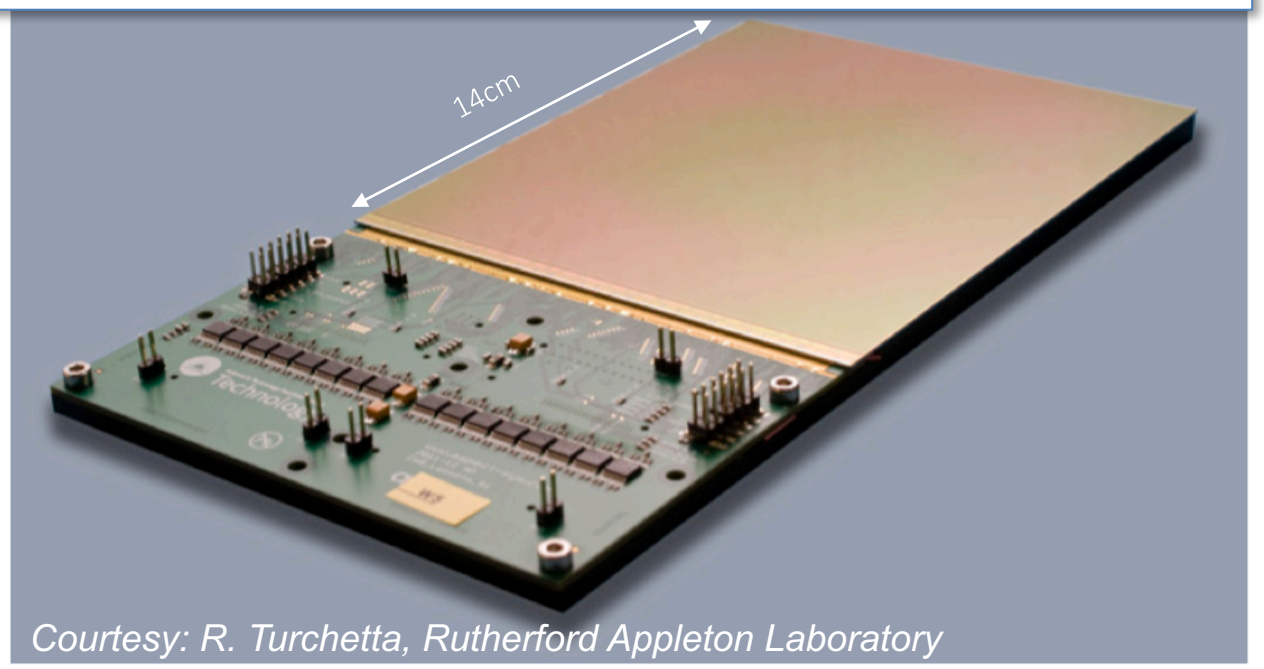




Staves built by tiling several sensors

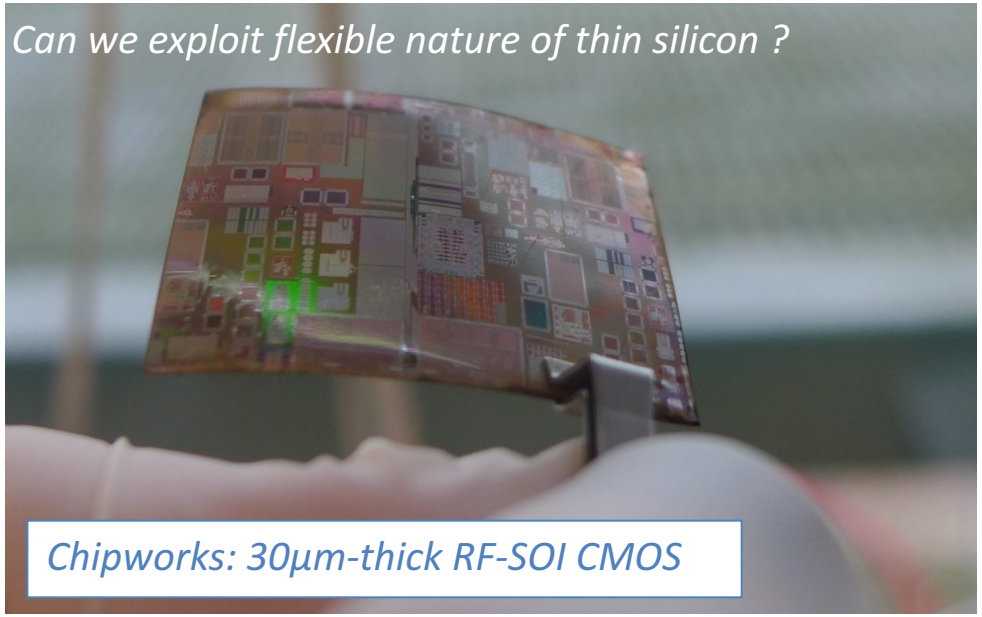


Stitching allows fabrication of sensors larger than the reticle size



Courtesy: R. Turchetta, Rutherford Appleton Laboratory

Curved Silicon Chips



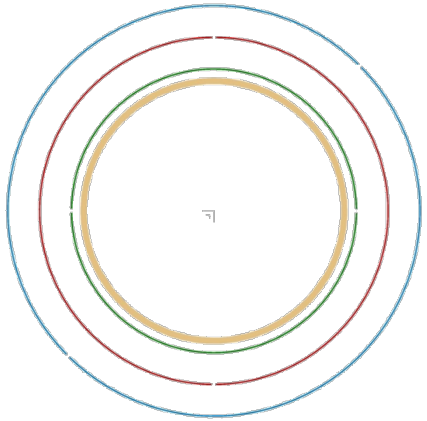
Ultra-thin chip (<50 um): flexible with good stability

Die type	Front/back side	Ground/polished/plasma	Bumps	Die thickness (µm)	CDS (MPa)	Weibull modulus	MDS (MPa)	r_{min} (mm)
Blank	Front	Ground	No	15–20	1263	7.42	691	2.46
Blank	Back	Ground	No	15–20	575	5.48	221	7.72
IZM28	Front	Ground	Yes	15–20	1032	9.44	636	2.70
IZM28	Back	Ground	Yes	15–20	494	2.04	52	32.7
Blank	Back	Polished	No	25–35	1044	4.17	334	7.72
IZM28	Back	Polished	Yes	25–35	482	2.98	107	24.3
Blank	Back	Plasma	Yes	18–22	2340	12.6	679	2.50
IZM28	Front	Plasma	Yes	18–22	1207	2.64	833	2.05
IZM28	Back	Plasma	Yes	18–22	2139	3.74	362	4.72

van den Ende DA et al. *Mechanical and electrical properties of ultra-thin chips and flexible electronics assemblies during bending*. Mircoelectron reliab (2014), http://dx.doi.org/10.1016/j.microrel.2014.07.125

R&D with IZM ALPIDE started

ITS3 – A Fully Cylindrical Tracking Detector



Pipe: r ≈ 16mm , ΔR = 0.5mm

L0: r ≈ 18mm , L1: r ≈ 24mm. L2: r ≈ 30 mm

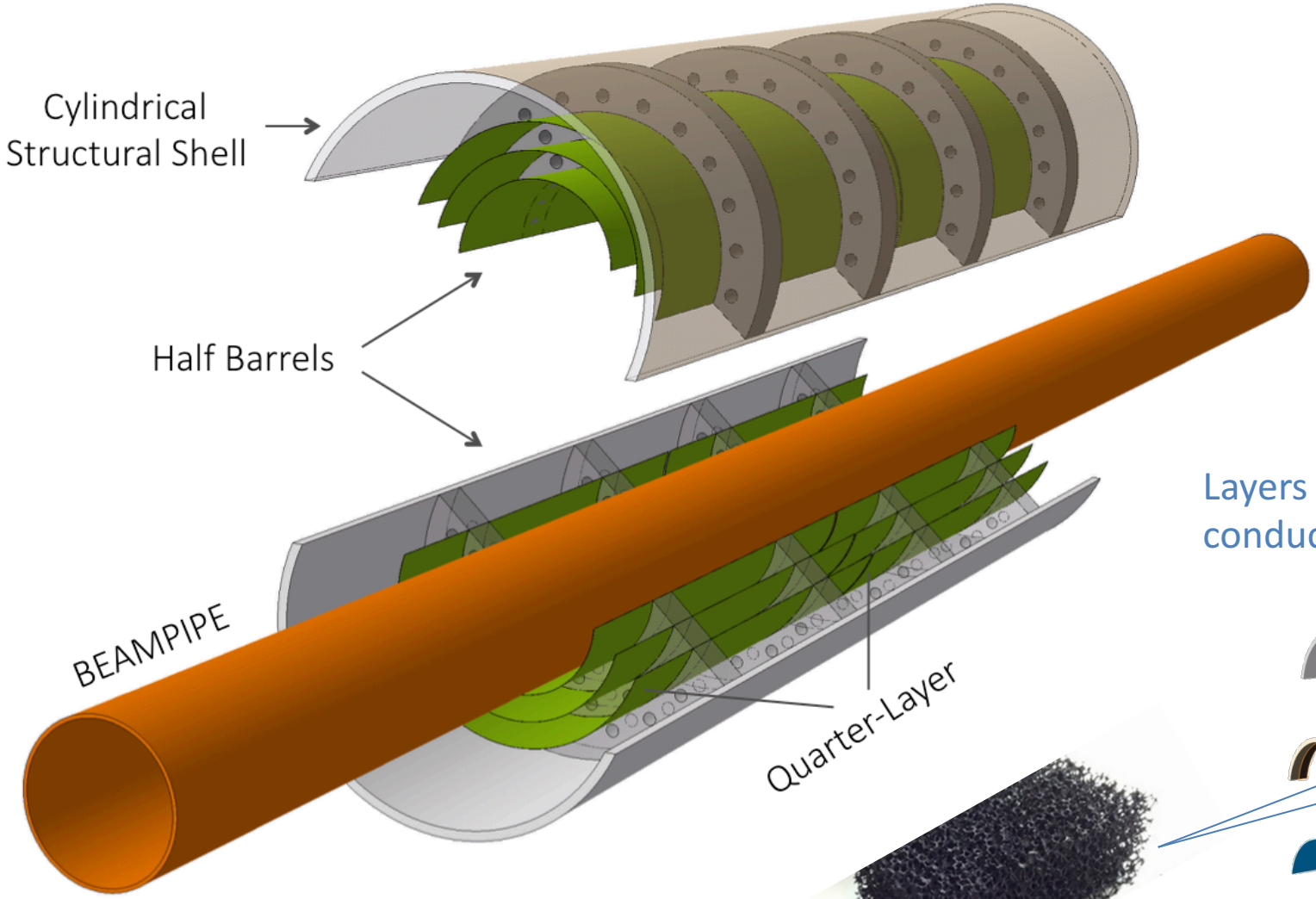
Beam pipe thickness: 500μm (0.14% X_0)

Sensor thickness: 20 – 40μm (0.03 - 0.05% X_0)

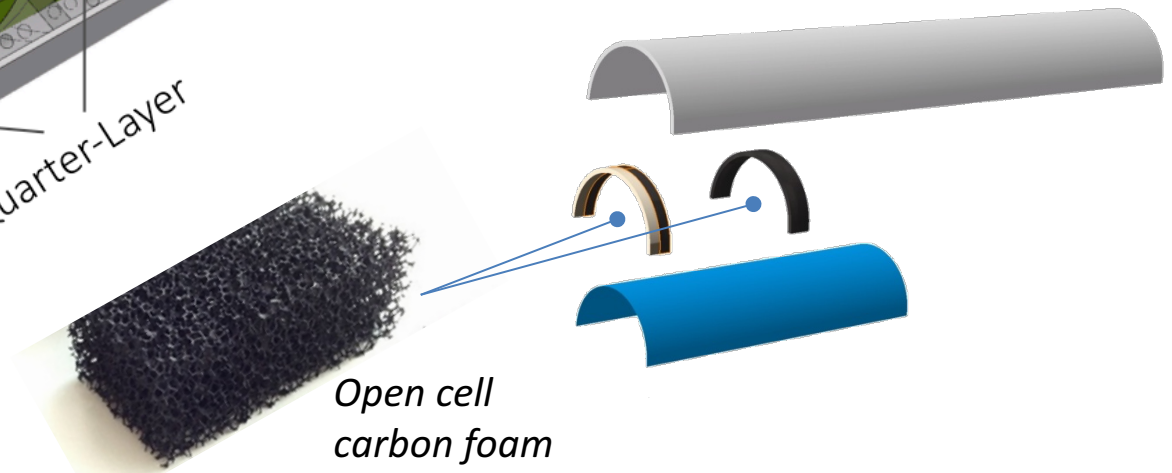
Beam pipe inner/outer radius (mm)	16.0/16.5		
IB Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	270	270	270
Pseudo-rapidity coverage[a]	±2.5	±2.3	±2.0
Active area (cm^2)	305	408	508
Pixel sensors dimensions (mm^2)	140×56.5	140×75.5	140×94
Number of pixel sensors / layer		4	
Pixel size (μm^2)		$O(30 \times 30)$	

Markus Keil (CERN), LHCP 2019

ITS3 Mechanical Layout

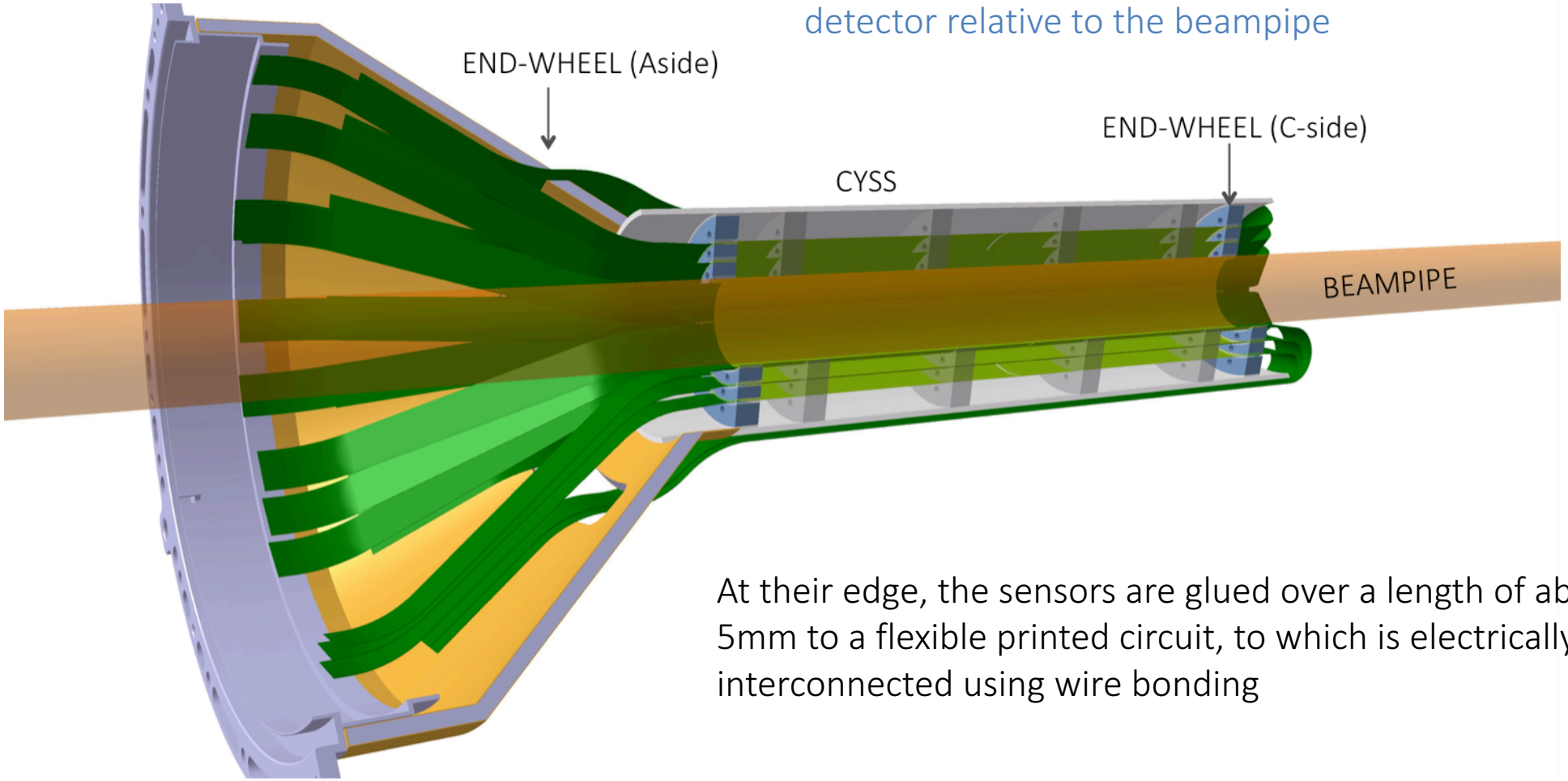


Layers supported by high-thermal conductive carbon foam (half-ring)



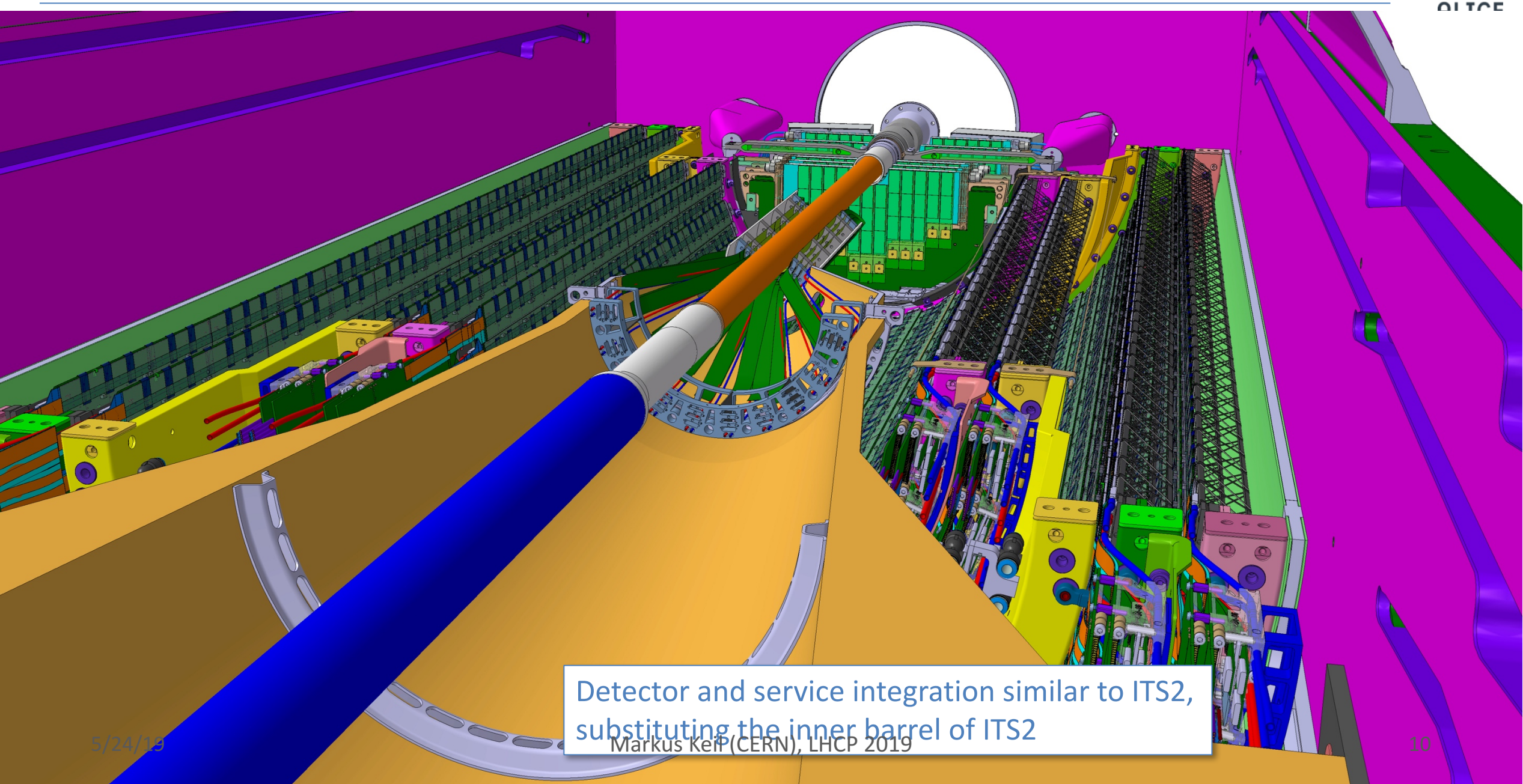
ITS3 Mechanical Layout

Two end-wheels provide precision and fixation of the detector relative to the beampipe



At their edge, the sensors are glued over a length of about 5mm to a flexible printed circuit, to which is electrically interconnected using wire bonding

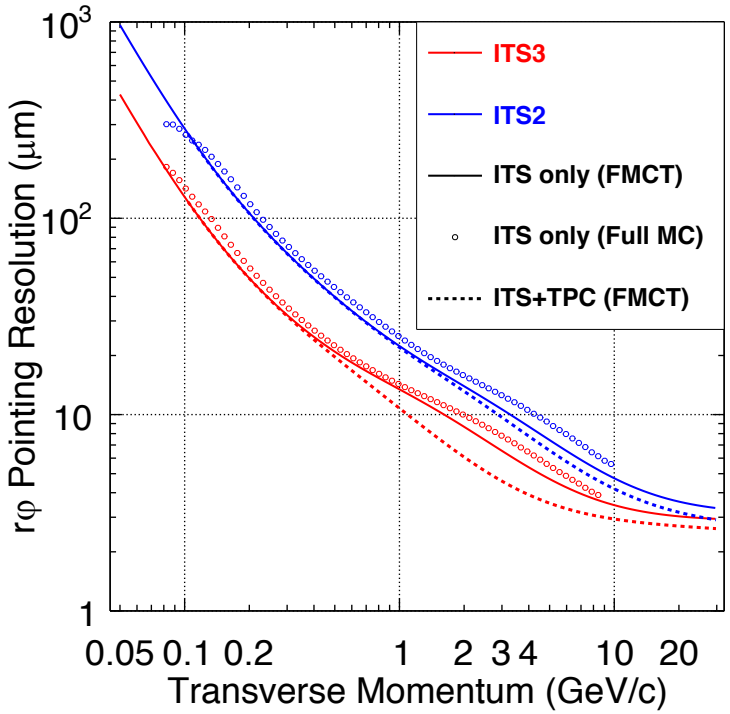
ITS3 System Integration

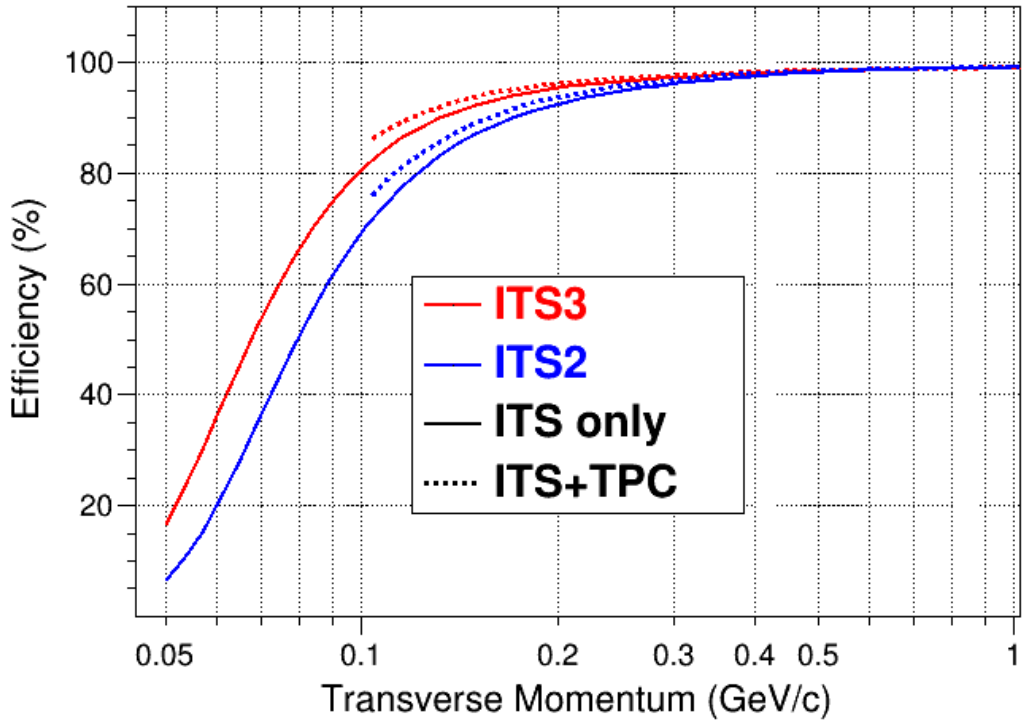


Detector and service integration similar to ITS2, substituting the inner barrel of ITS2

Tracking Performance

Pointing resolution and tracking efficiency (charged pions) for ITS2 and ITS3





FMCT: semi-analytical, includes QED hits, but no energy loss fluctuations

Full MC: simplified ITS3 geometry, full MC simulation (GEANT3), Cellular Automaton ITS Tracker

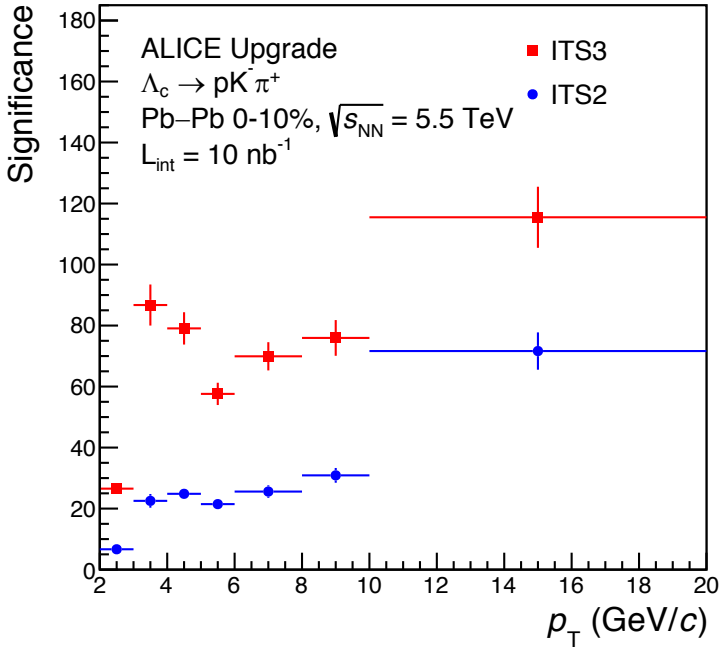
⇨ Improvement of ≈ factor 2 at all p_T's

Efficiency increases factor 1.2 – 2, for p_T < 100MeV

Physics Performance Studies – Λ_c and thermal dielectrons

Measurement of charm baryons (smallest cτ)

⇨ vertexing precision



ITS3/ITS2 improvement
x 10 (S/B) , x 4 (significance)

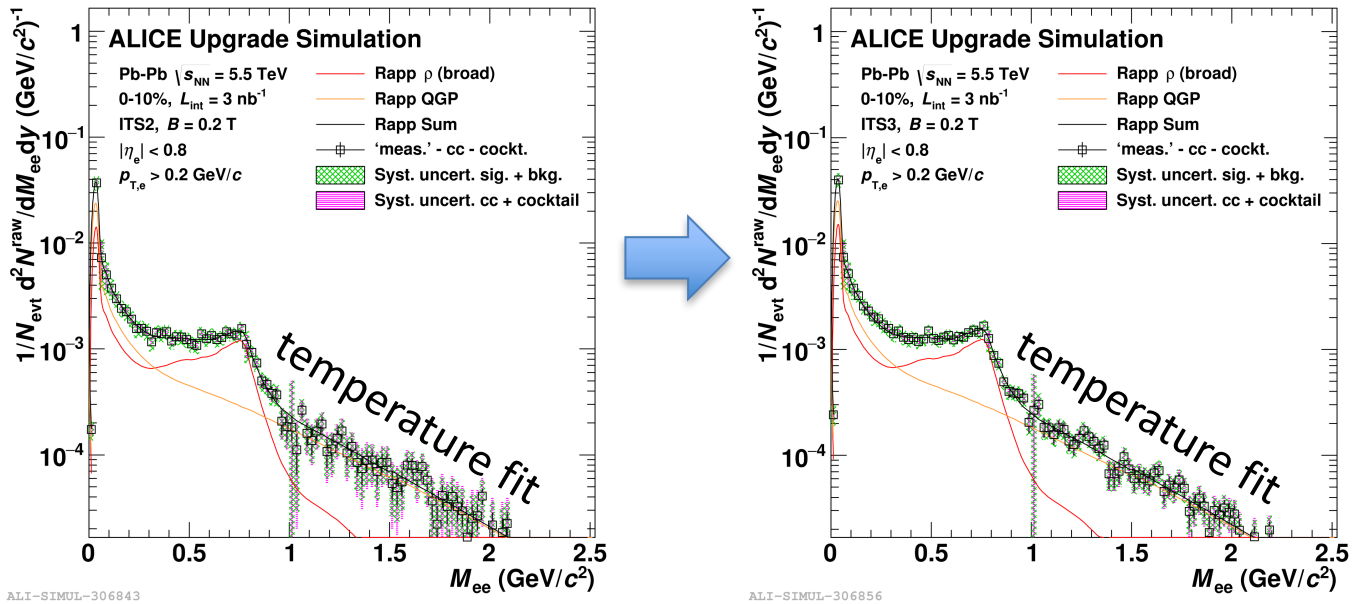
Low-mass dielectrons

⇨ vertexing (better charm rejection)

⇨ material thickness (less conversion)

⇨ Higher low-p_T efficiency (better conversion rejection)

⇨ Lower syst. uncertainty in region used for temp. fit



T (QGP)	Stat. error	Syst. (BG)	Syst. (Charm)
ITS3 / ITS2	1/1.3	1/2	1/2

Summary

Proposal for the construction of a novel vertex detector:

- New beam pipe with IR = 16mm, ΔR = 0.5mm
- Three truly cylindrical layers based on curved ultra-thin sensors ($x/X_0 < 0.05\%$ per layer)
- The three layers would replace the innermost three layers of ITS2 in LS3 and differ only by their radii, with the innermost layer at R = 18 mm

The ITS3 will reduce the material budget to the bare minimum for a silicon tracker and provide a large improvement of the tracking precision and efficiency at low p_T

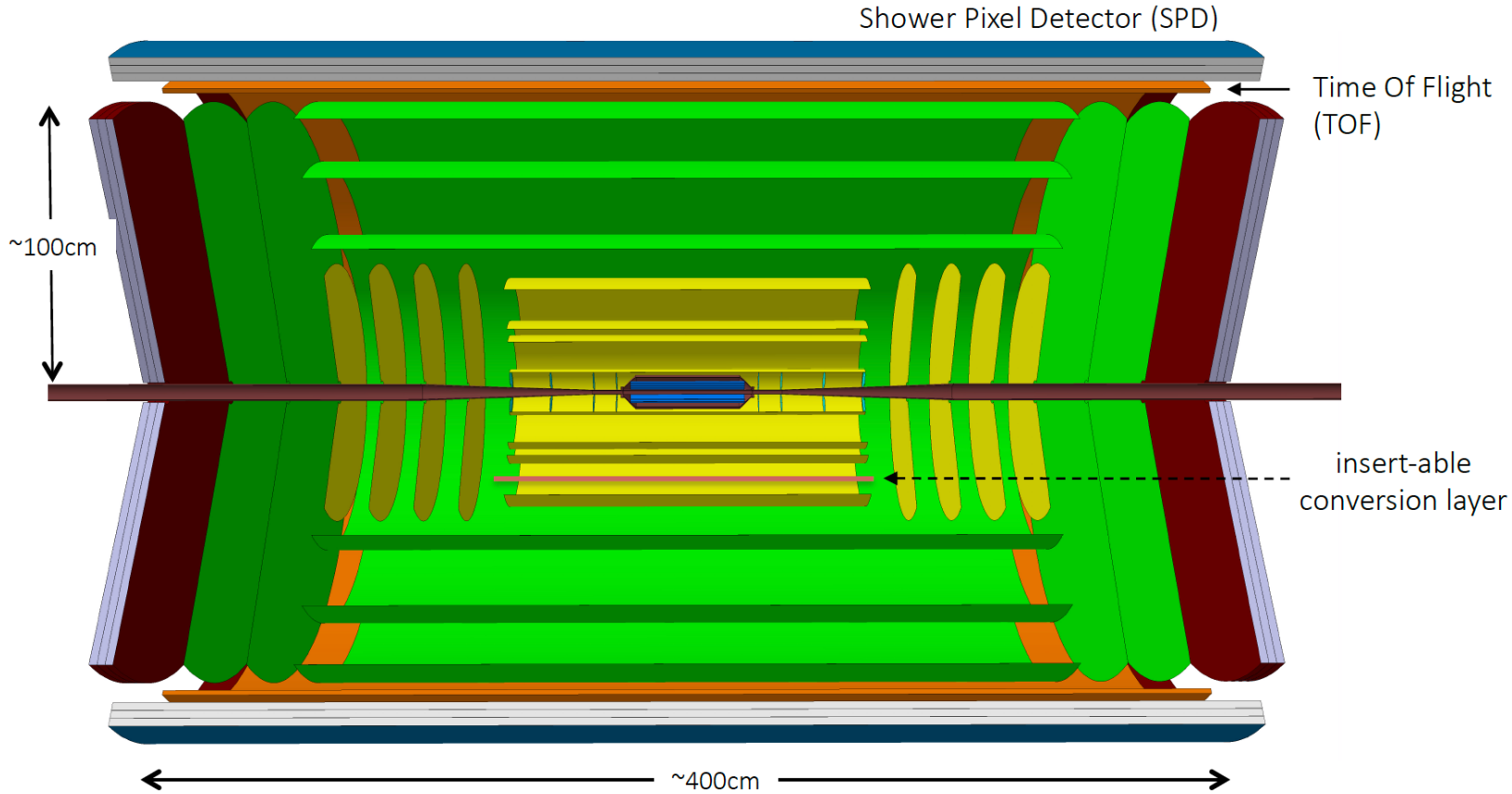
The combination of these improvements will lead to a significant advancement in the measurement of low p_T charmed hadrons and low-mass dielectrons

Tentative timeline:

January 2019	Expression of Interest (ALICE-PUBLIC-2018-013)
2020 – 2023	R & D
2022	TDR
2024 – 2025	Construction
2025 – 2026	Pre-commissioning and Installation

Outlook

+ A test-bed in view of a future heavy-ion detector

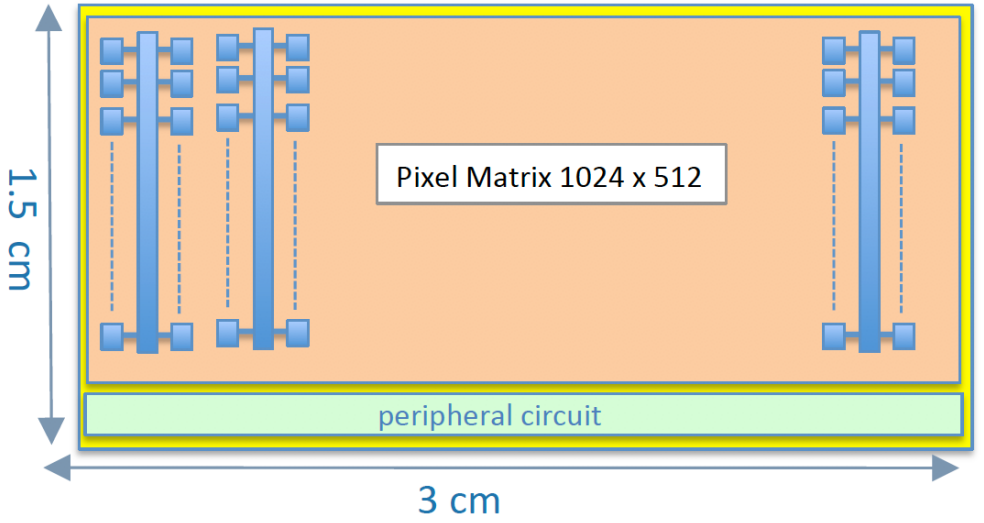


[*A next-generation LHC heavy-ion experiment*, arXiv:1902.01211]

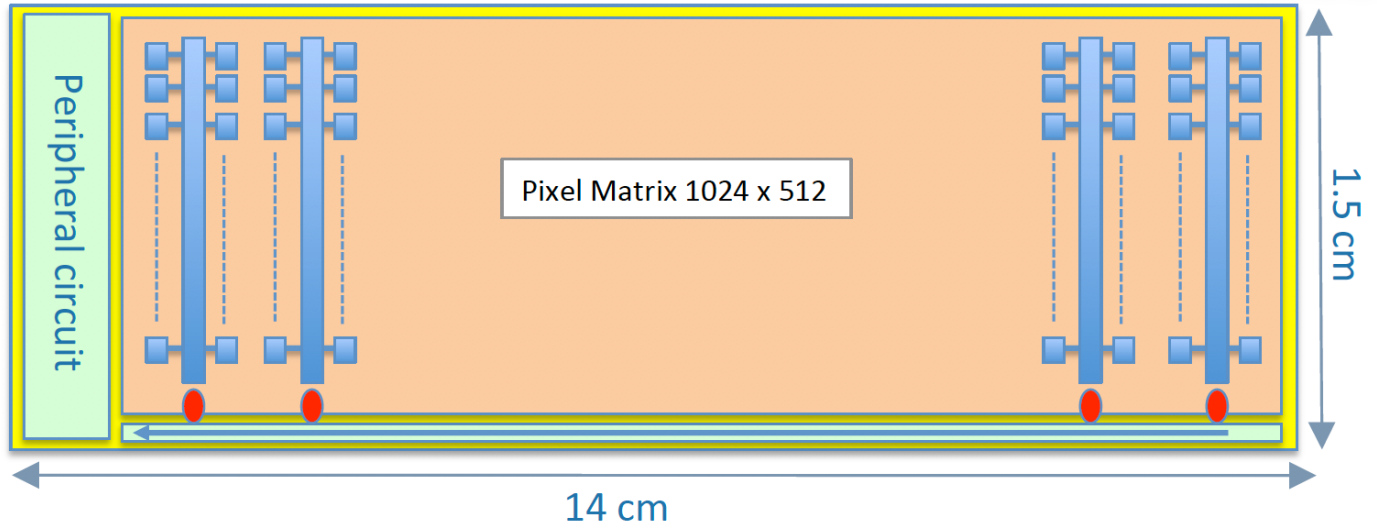
Backup

ALPIDE Architecture and Stitching

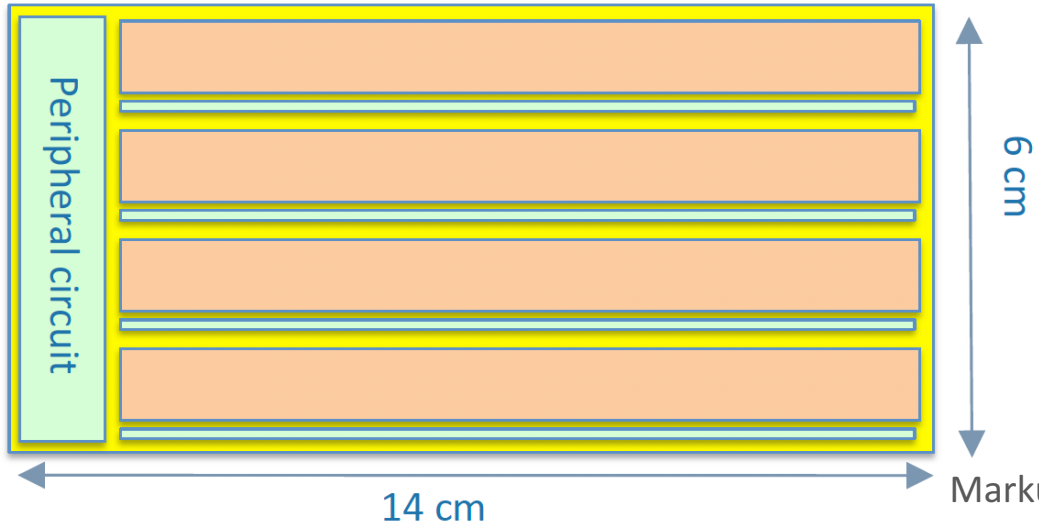
ALPIDE Chip:



1D stitched sensor (z-direction)



2D stitched sensor – wafer-scale



By instantiating multiple times the same circuits in the second dimension (ϕ) one can realize the sensors for the different layers. For example

- L0 = 14 cm x 6.0 cm
- L1 = 14 cm x 7.5 cm
- L2 = 14 cm x 9.0 cm