Data transmitting ASIC for liquid Argon TPC for the DUNE experiment

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Front End Electronics, Jouvence, 21 May 2018

Outline

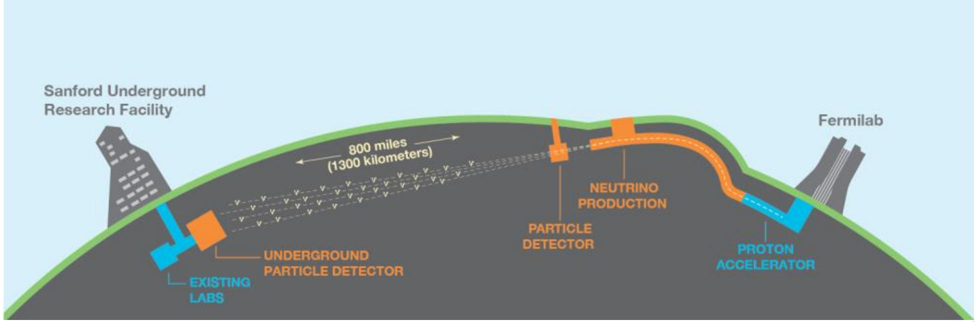
- Cold electronics for DUNE
- Requirements for cryogenic operation, HCE and choice of technology
- Development of custom cryogenic Spice models
- Development of a custom library of standard cells for cryogenic operation
- LVDS Transmitter and Receiver
- COLDATA
- CDP1: COLDATA Prototype chip
  - Test setup and results
- Conclusions

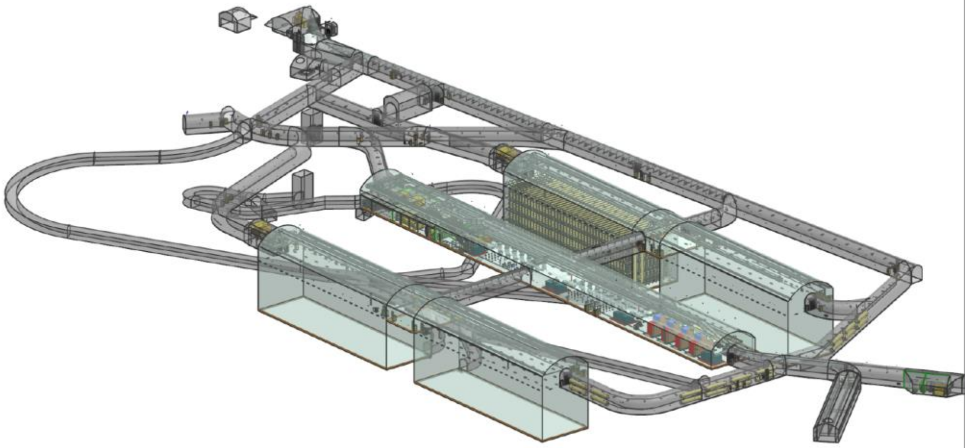
DUNE: Deep Underground Neutrino Experiment

Flagship project for HEP and Fermilab: over 1000 collaborators from 175 institutions in 30 countries plus CERN.

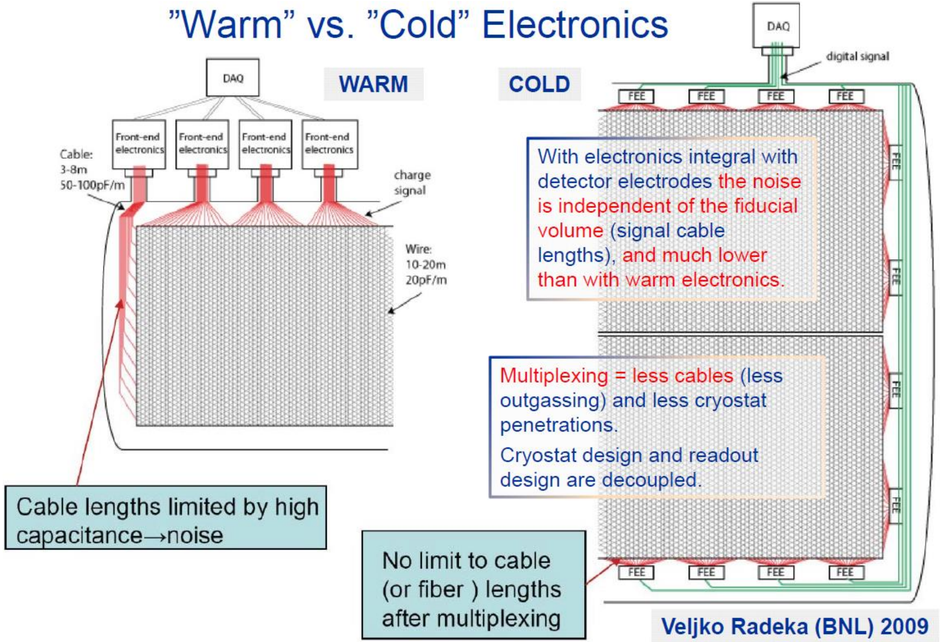
67000 tons of Lar, 1.5km deep

Liquid Argon Time-Projection Chamber (LArTPC) technology





Operation in liquid Argon



Requirements

- negligible risk of failure due to the hot carrier effect (less than 0.7% channel failure in 30 years of operation)
- a total power consumption of less than 50 mW/channel.
- fully functional at both room temperature and liquid argon temperature;
- both control and data links must operate with negligible error rate over cables up to ~30m in length.

Benefits of operating in liquid Argon:

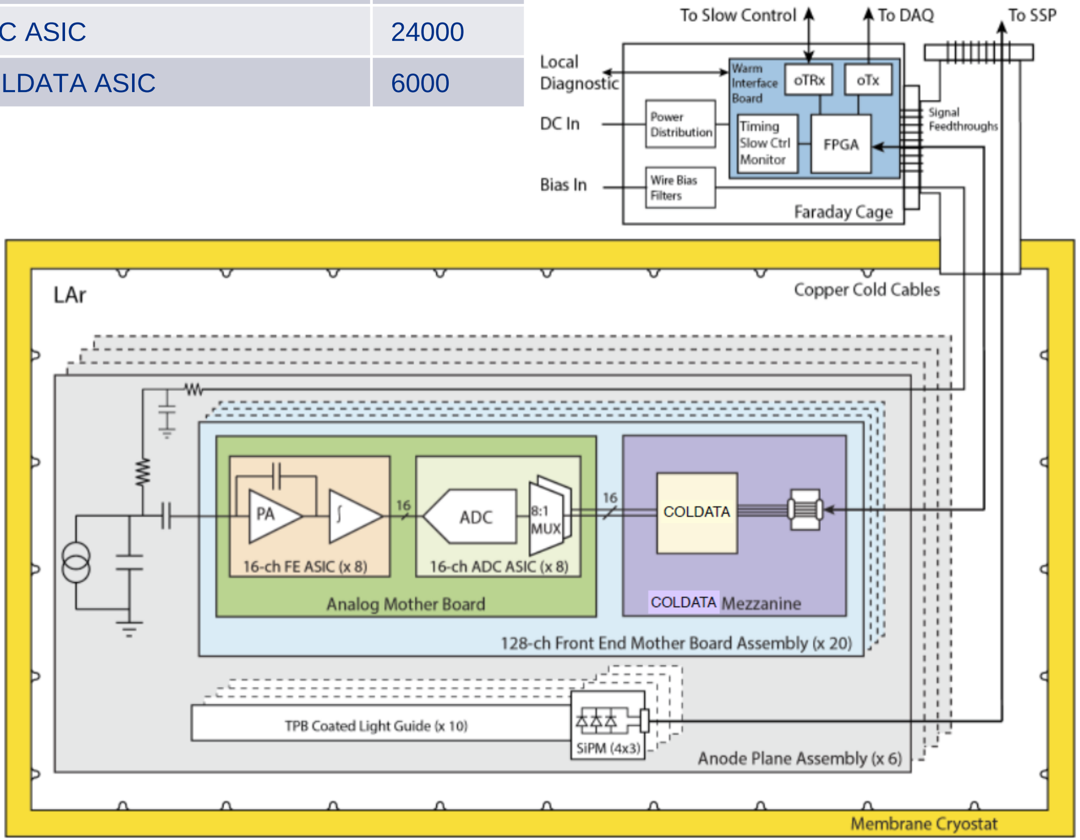
- The **charge carrier mobility** in silicon is higher and thermal fluctuations are lower at liquid argon temperature than at room temperature. For CMOS electronics, this results in substantially **higher gain** and **lower noise** (by about a factor of two) at liquid argon temperature than at room temperature, which greatly extends the reach of the DUNE physics program.
- Mounting the front-end electronics on the anode plane array (APA) frames also **minimizes the input capacitance**.
- Placing the digitizing and multiplexing electronics inside of the cryostat allows for a **reduction in the total number of feed-throughs** into the cryostat, **reducing the expense and complexity** of the experiment.

DUNE readout

Element	Quantity
Anode plane array (APA)	150
Front End Mother Board (FEMB)	3000
FE ASIC	24000
ADC ASIC	24000
COLDATA ASIC	6000

The basic module for the baseline readout of the single-phase DUNE detector are the Front End Mother Board (FEMB), each of which consists of:

- 8 16-channel front-end ASICs for amplification and pulse shaping (**LArASIC** - BNL);
- 8 16-channel 12-bit ADC ASICs operating at 2 MHz (**ColdADC** – LBL+BNL+FNAL);
- 2 64-channel control and communications ASICs (**COLDATA** – FNAL+SMU)



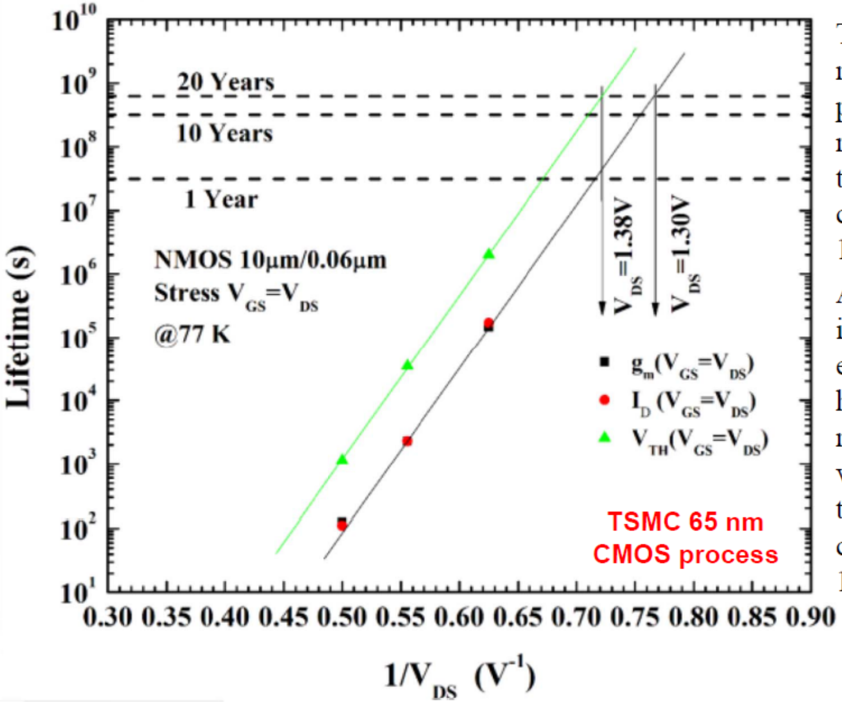
65nm choice

Process of choice for HEP (LHC upgrades).

Alignment with other projects and sharing of resources (IPs, experience…).

Sufficient speed to accommodate lifetime enhancement guidelines (L, Vdd) without pushing the design.

Long term investment for custom models and libraries.



The predicted lifetime for 130 nm nMOS devices reaches 20 years provided the drain voltages are reduced from the nominal, room temperature value of 1.5 V to a cryogenic temperature value of 1.49 V.

As noteworthy as this prediction is, the 65 nm nMOS device is even more resistant to cryogenic hot carrier degradation. Its nominal, room temperature voltage of 1.2 V is already lower than the maximum allowable cryogenic temperature voltage of 1.3 V.

FERMILAB/SMU: J. R. Hoff, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.59, NO.4, AUGUST 2012

BNL: Shaorui Li, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.60, NO.6, DECEMBER 2013

FERMILAB/SMU: Guoying Wu, et al., IEEE TRANS. ON DEV. AND MATERIALS RELIABILITY, VOL.14, NO.1, MARCH 2014

FERMILAB/SMU: J.R.Hoff, et al., „Cryogenic Lifetime Studies of 130nm and 65nm CMOS Technologies for High-Energy Physics Experiments, *in publishing in IEEE TRANS. ON NUCLEAR SCIENCE*

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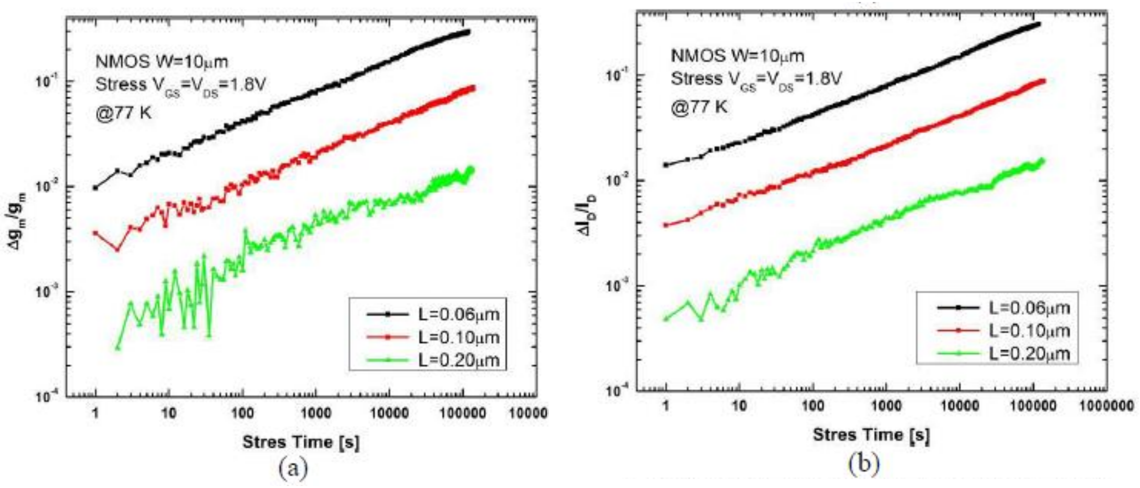
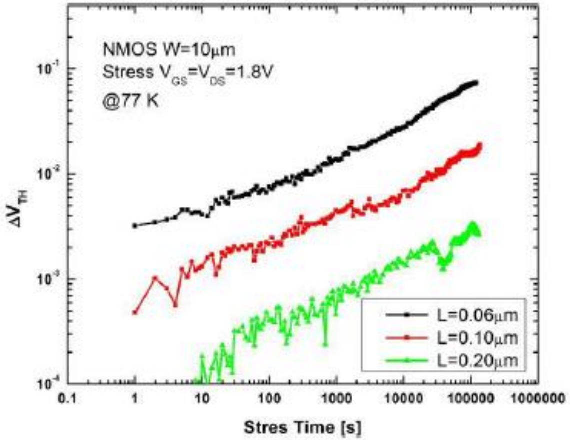


Normalized change in *a)* transconductance, *b)* drain current, and *c)* increase in threshold voltage with stress time (Vgs=Vds=1.8V; T=77K)



Custom CMOS models for liquid Argon operation

Creation of cryogenic CMOS models by **Logix Consulting, Inc.** (Texas) based on test structures and data collected by FNAL, SMU, BNL groups.

- Macro model: all simulations should point to the '**nch_mac**' and '**pch_mac**' models.
- **Valid for T=25C and T=-189C only**.
- Because of limited test structures, this model is valid for **0.06um < length <=10um**.
- **Flicker noise** parameters were verified with low temperature data in this release.
- The model supports the following simulation corners: **tt, ss, ff, sf, fs and mismatch**.
- **Mismatch** variations are from the original foundry model and have not been validated at low temperature.
- Validation of the junction capacitances at low temperatures was not possible due to limited test structures. An extra coefficient was included to assist in quantifying the sensitivity of the circuit to the uncertainty in junction capacitance temperature coefficients of the original foundry model.

Example of Spice model simulation with foundry models vs. measured data.

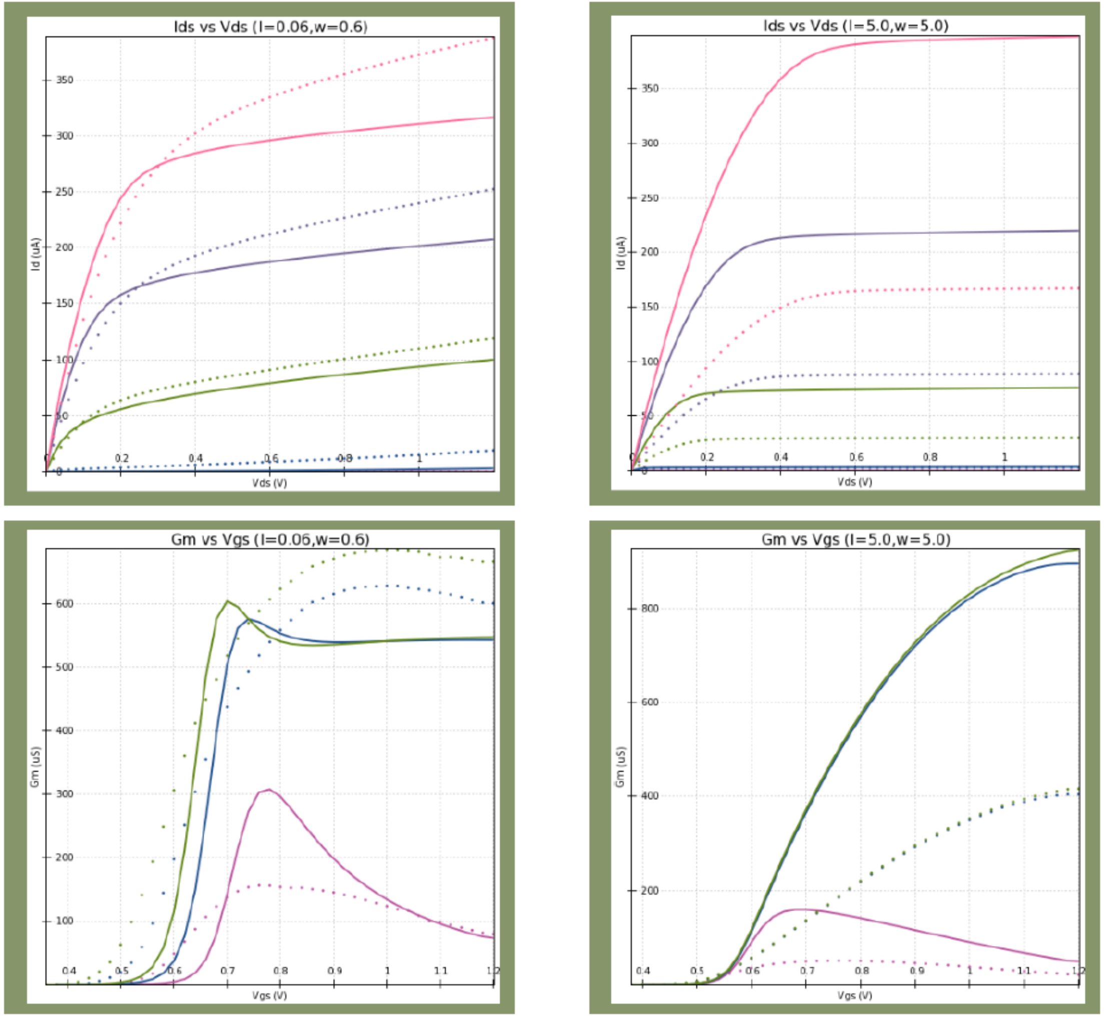
Thin oxide NMOS, -189°C, V_{BS}=0

Points: measurement (= custom models)
Lines: foundry models at -189C

The foundry models, when extrapolated to liquid argon temperature, are wildly off-the-mark.

No obvious trend is visible

W/L=0.6/0.06 W/L=5/5



Example of measurement points and model parameter fit

Foundry documentation includes:

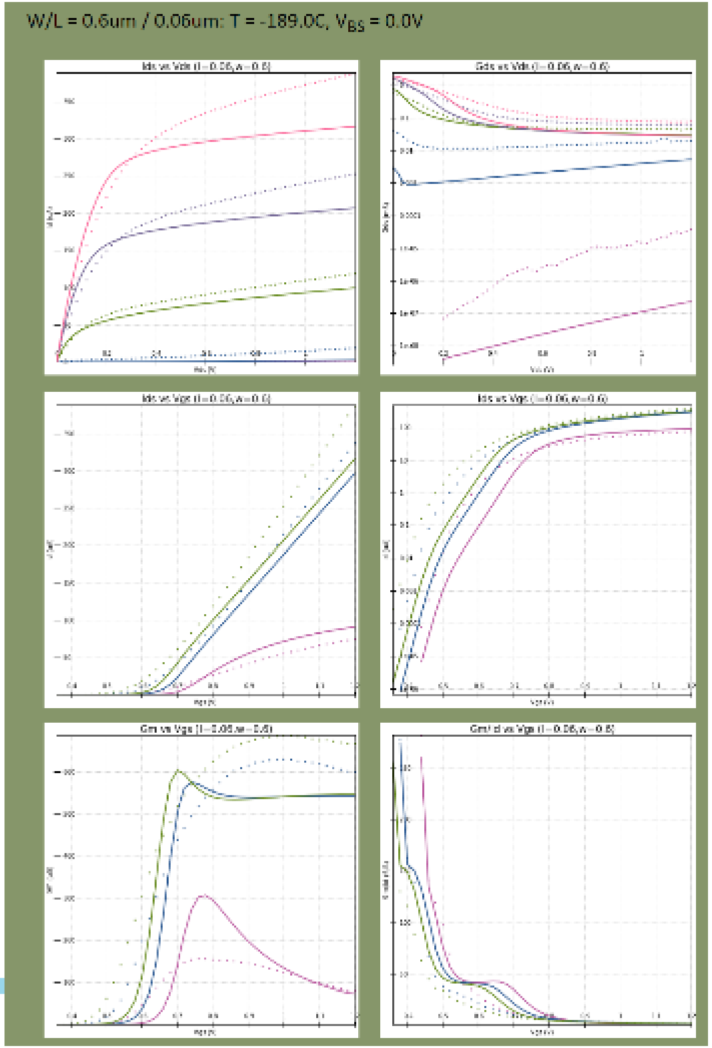
I_{DS} vs. V_{DS}
G_{DS} vs. V_{DS}
I_{DS} vs. V_{GS}
G_m vs. V_{GS}
G_m/I_D vs. V_{GS}

For: T 25C
-189C

V_{BS} ±0
±0.6
±1.2

W/L: from 5µm/5µm down to 0.12µm/0.06µm

thin and thick oxide



Custom Standard Cells Digital Library (L=90nm)

- A modified version of the standard cell library tcbn65lp from Foundry/IMEC PDK
- All lengths increased from 60nm to **90nm** to reduce HCE
- pMOS also increased to maintain balance
- Cells' height has not changed at 1.8um (**9-track**)
- Cells' width increased by 10 to 20%
- Only M1, pins on grid

- **Inherently slower**/with less drive strength than original 60nm library (30% slower)

- All transistors in the schematic have been replaced with their ***_mac** counterpart, which is needed to simulate the design with the LOGIX custom models
- Each cell contains **layout**, **schematic** and **abstract** views.

Design Dimension	Physical Dimension
Drawn Gate Length	**0.09 µm**
Layout Grid	0.005 µm
Vertical Pin Grid	0.20 µm
Horizontal Pin Grid	0.20 µm
Cell Power & Ground Rail Width	0.33 µm
Track Number	9

Cell categories

Includes ~230 cells

Includes 4 or 5 different drive strengths per logic function

Type	Sub-type	Cells
Combinatorial	Simple Logic	INV, BUFF, BUFT, ND, NR, AN, OR, XNR, XOR
	Complex Logic	AO, OA, AOI, IAO, IOA, OAI, IND, INR, MUX
Storage	Latch	Latch LH (Latch with High Enable), LN (Latch with Low Enable)
	Flip-Flop	DF (D Flip-flop), DFK (synchronized set/reset D Flip-Flop), DFN (negative clock trigger D Flip-Flop)
Special	Delay cell	DEL
	Clock Buffer	CKB, CKN
	Clock And	CKND2, CKAN2
	Clock XOR	CKXOR2
	Adder	FA1 (1-Bit Full Adder), HA1 (1-Bit Half Adder)
	Antenna Diode	ANTENNA
	Tie-high / Tie-low Cell	TIEH, TIEL
	Filler Cell for Core	FILL
	Decoupling Cell	DCAP, DCAP4, DCAP8, DCAP16, DCAP32, DCAP64

List of cells (in red the cells in the original library not included in tcbn65lp_90nm_mac)

Combinatorial Elements

Code	Description
AN	AND Gate
AO	AND-OR Gate
AOI	AND-OR-Inverter Gate
BUFF	Non-Inverting Buffer
BUFT	Non-Inverting Tri-State Buffer with High Enable
IAO	Inverter-AND-OR Logic Function Gate
IND	NAND with 1 Inverted Input
INR	NOR with 1 Inverted Input
IIND	NAND with 2 Inverted Inputs
IINR	NOR with 2 Inverted Inputs
INV	Inverter
IOA	Inverter-OR-AND Logic Function Gate
MAOI	Modified AOI Logic
MOAI	Modified OAI Logic
MUX	Multiplexer
MUXxN	Multiplexer with Inverted Output
ND	NAND Gate
NR	NOR Gate
OA	OR-AND Gate
OAI	OR-AND-Inverter Gate
OR	OR Gate
XNR	Exclusive NOR Gate
XOR	Exclusive OR Gate

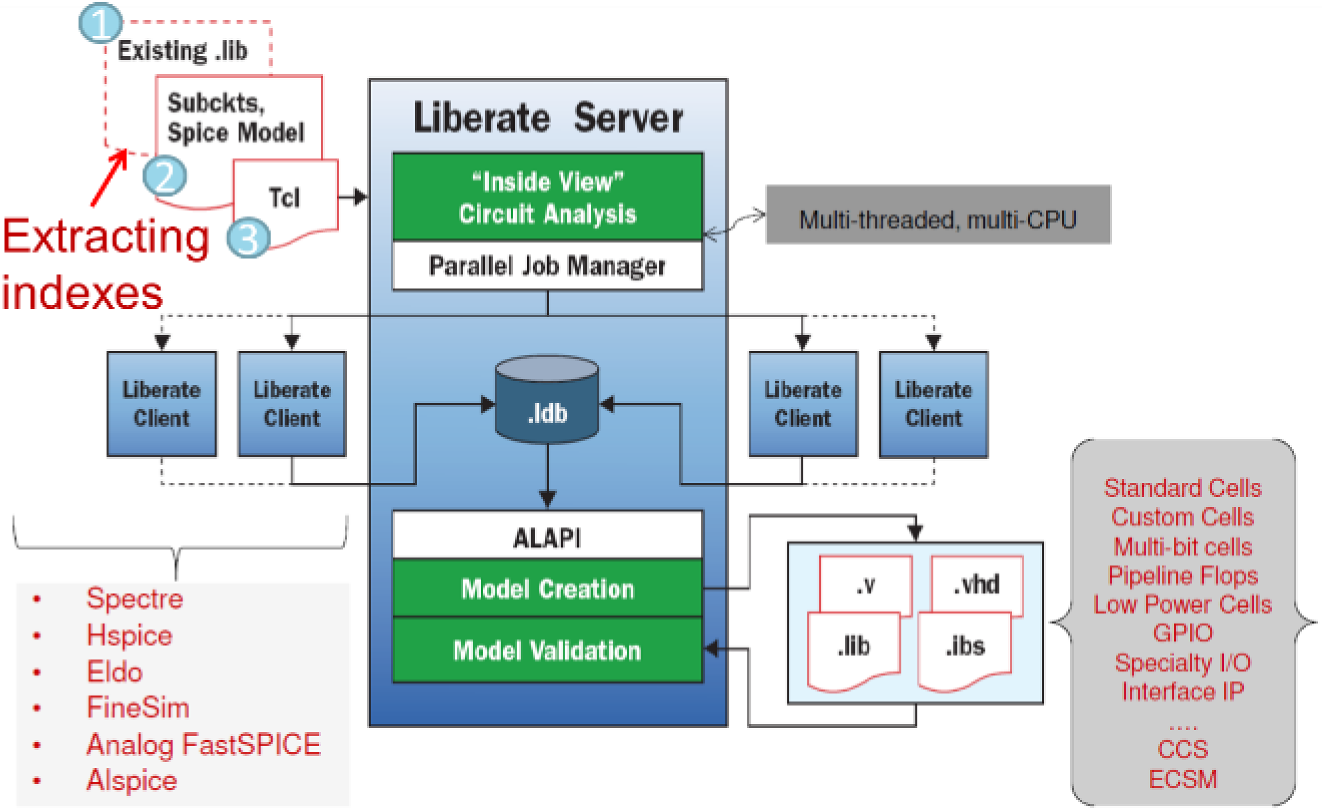
Special Function Cells

ANTENNA	Antenna Diode
BHD	Bus Holder, Bus Repeater Cell
CKBX	Balanced Clock Driver
CKLNQ	Positive-edge Gated Clock Latch with Q Output Only
CKLHQ	Negative-edge Gated Clock Latch with Q Output Only
CKNX	Balanced Clock Driver with Inverted Output
CKND2	Balanced clock cell for 2 input NAND type
CKAN2	Balanced clock cell for 2 input AND type
CKXOR2	Balanced clock cell for 2 input XOR type
CLMUX2	Balanced clock cell for 2 to 1 multiplexer type
DCAP	De-coupling Cell
DEL	Delay Cell
FA1	1-Bit Full Adder
HA1	1-Bit Half Adder
FILL	Filler cell for Core
TIEH	Tie-High Cell
TIEL	Tie-Low Cell

Storage Elements

DF	D Flip-flop
DFN	Negative trigger D Flip-flop
DFK	D Flip-flop with Synchronous Clear / Set
DFX	D Flip-flop with 2-Inputs MUX
EDF	Enable D Flip-flop
EDFK	Enable D Flip-flop with Synchronous Clear / Set
LH	Latch with Active High Clock
LN	Latch with Active Low Clock

Cadence Liberate Flow



Library Characterization: Essential for Static Timing Analysis (STA)

- Cadence Liberate (v15.1) and associated Tcl scripts
- LVS/QRC extraction of the cells
  - Script to modify the model name (nch → nch_mac, pch → pch_mac)
- Foundry and custom model files

Type of library
- Non Linear Delay Model (NLDM)
- Effective Current Source Model (ECSM)

Timing
- Combinational
  - Delay & Transition Time
- Sequential
  - Delay & Transition Time
  - Hold and Setup
  - Recovery and Removal

Power
- Leakage
- Internal Power

Data is arranged in Look Up Table (LUT) format

Name	Process	Voltage	Temp	Models
UPenn-TT	tt	1.2	27	Foundry model
BC	ff	1.32	0	Foundry model
UPenn	ff	1.2	27	Foundry Model
WC	ss	1.08	125	Foundry Model
UPenn	ss	1.2	27	Foundry Model
TC_COLD	tt	1.2	-189	Logix Model
UPenn	tt	1.2	-186	Logix Model
BC_COLD	ff	1.32	-189	Logix Model
UPenn	ff	1.2	-186	Logix Model
WC_COLD	ss	1.08	-189	Logix Model
UPenn	ss	1.2	-186	Logix Model

Corners Identification

LVDS Transmitter and Receiver for liquid Argon

- Designed to comply with LVDS standard (2.5V → thick oxide transistors), but also to operate reliably down to VDD=1.8V
- Programmable output current
- Non-minimum length transistors for lifetime operation at liquid argon temperature (89K)
- Include level shifters to interface to 1.2V core voltage

Both Tx and Rx have been prototyped and proven to work at both room and LAr temperatures, but have yet to be stress tested and characterized. In this prototype, Rx and Tx are linked through a I2C slave block, which limits the data rates.

A dedicated test structure has been manufactured and is expected soon.

LVDS Tx

- All L ≥ 90nm
- Input voltage: 1.2V (chip core)
- Output voltage: 2.5V to 1.8V (I/O)
- Compatible with LVDS standard (2.5V supply, +-3.5mA into 100 Ohm external termination, 1.25V typical common mode output (1.125V<=V_{CM}<=1.375V)
- Programmable output current for low power operation: +-2mA, +-4mA, +- 6mA, +-8mA.
- Temperature range: -189C<=T<=+125C
- Output common mode voltage: ½ VDD, stabilized by active common mode feedback (CMFB)

- Low profile layout: ~180µm x 65µm (excluding output pads). Top metal is M6 (in MOM capacitors, could go to M4)
- External termination

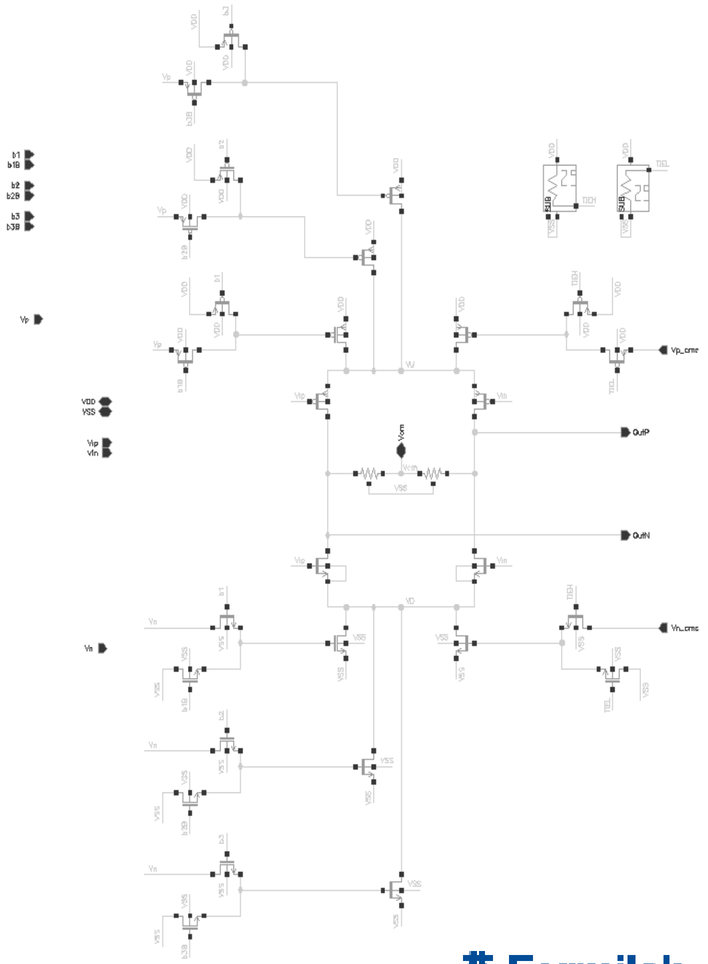
LVDS Tx

- **Predriver**: includes a $Vdd_{core} \rightarrow Vdd_{IO}$ level shifter + buffers to drive the large capacitive load of the Tx bridge switches

- **Driver**: bridge architecture with selectable current

- **Common Mode Feedback** (CMFB) with resistive sensing (10KΩ) for baseline correction (LVDS spec: $1.125V \leq V_{CM} \leq 1.375V$)
  - PM φ~90°, WC φ~60° for T=-189C and VDD=1.8V

- Level shifters for the configuration bits
- PDB2Ax analog I/O pads (as recommended by Foundry), passive protection diodes only for low impedance



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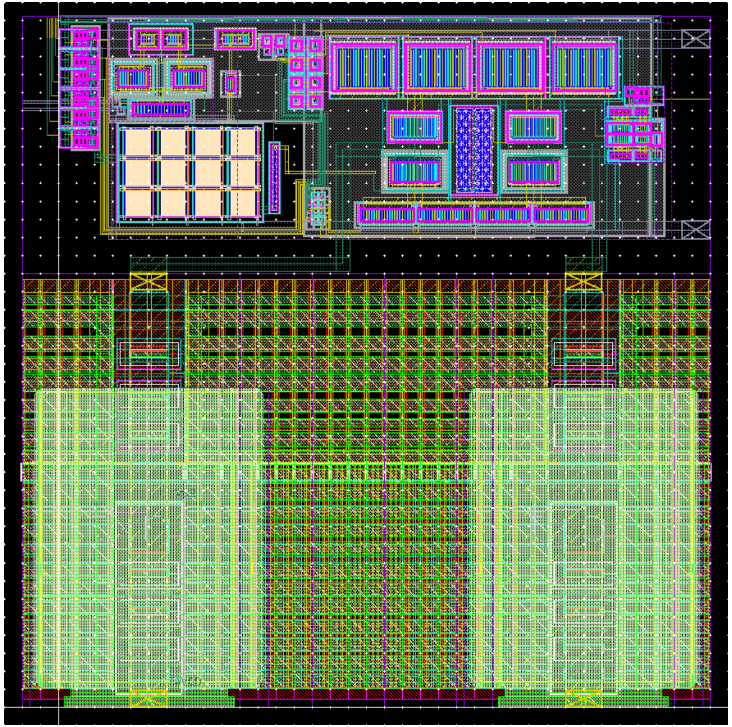
Layout:

- DFM + guardrings for all transistors

180µm



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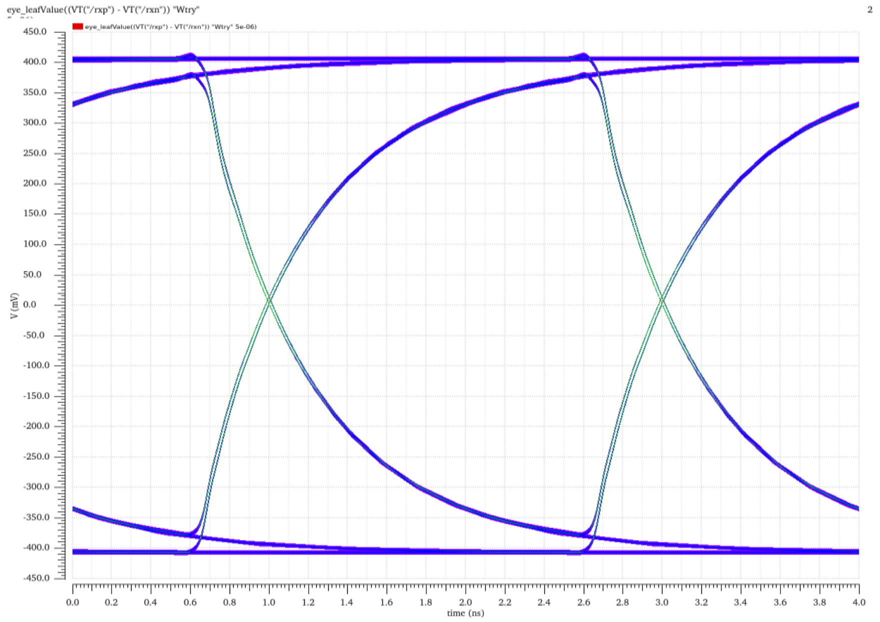
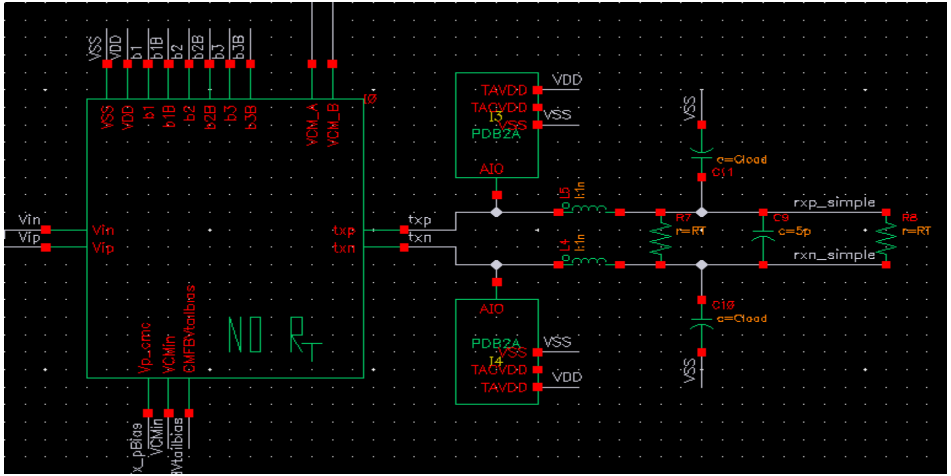
LVDS Tx Performance

To characterize this block, I follow what Texas Instruments does in their LVDS datasheet and use a simple RC load (5pF in parallel to 100 Ohm termination), but still accounting for the wirebonds at both ends (both with or without source termination).



Simulated eye diagram for VDD=2.5V, TT, 27C, Iout=± 4mA, at 500 Mbps.



Schematic of the output load following Texas Instruments LVDS Tx datasheets, with just RC load, but including LC to simulate bondwires (with or w/o source termination).

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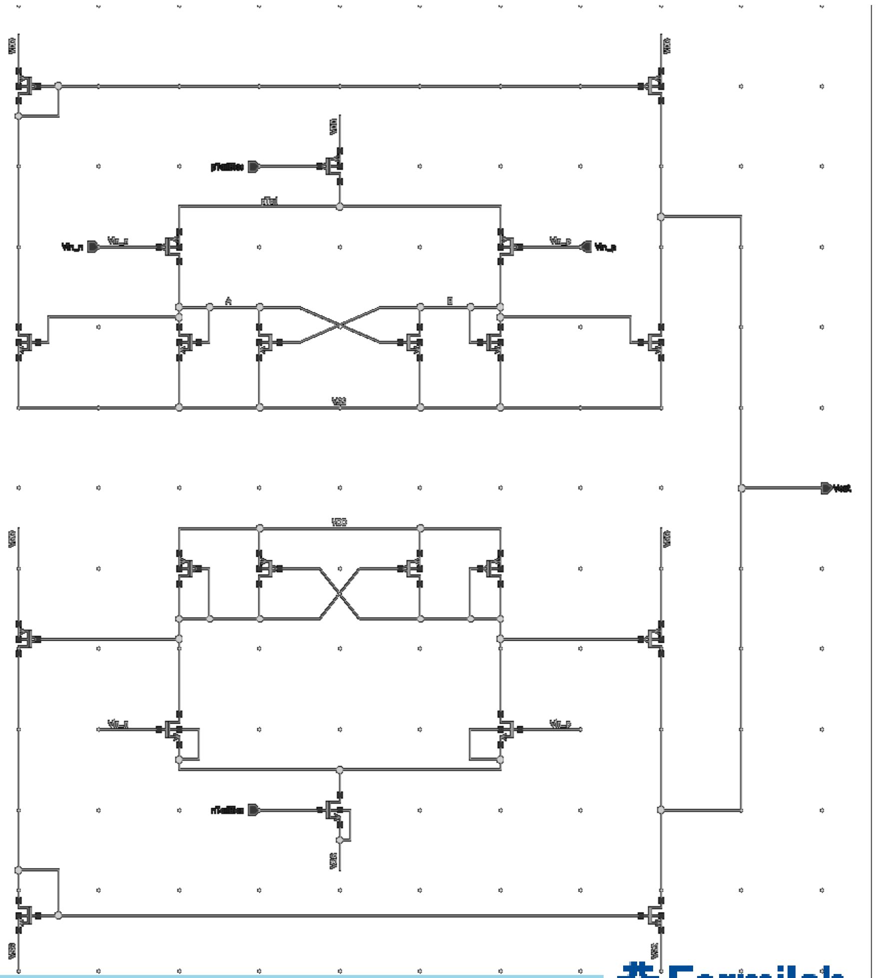
LVDS Rx

- All L ≥ 90nm
- Input voltage domain: 2.5V to 1.8V (I/O)
- Input differential voltage V_{ID} from ±100mV up to rail-to-rail
- Output voltage: 1.2V (chip core)
- Compatible with LVDS standard (2.5V supply, +-3.5mA into 100 Ohm external termination, 1.25V typical common mode input (1.125V<=V_{CM}<=1.375V)
- Temperature range: -189C<=T<=+125C

- Low profile layout: ~115µm x 20µm (excluding output pads). Top metal is M4
- No Internal termination



LVDS Rx

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- **Driver**: bridge architecture with selectable current
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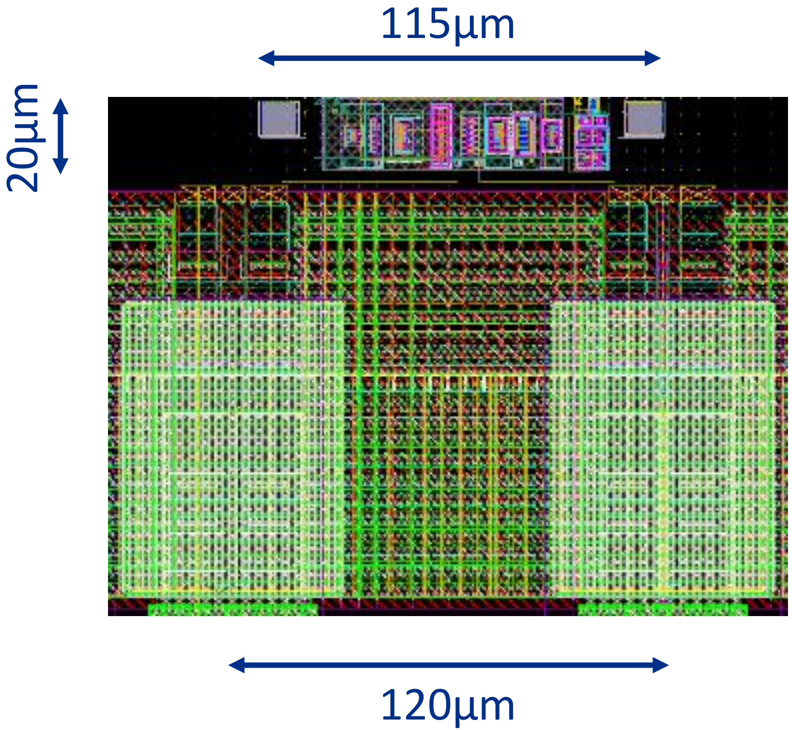
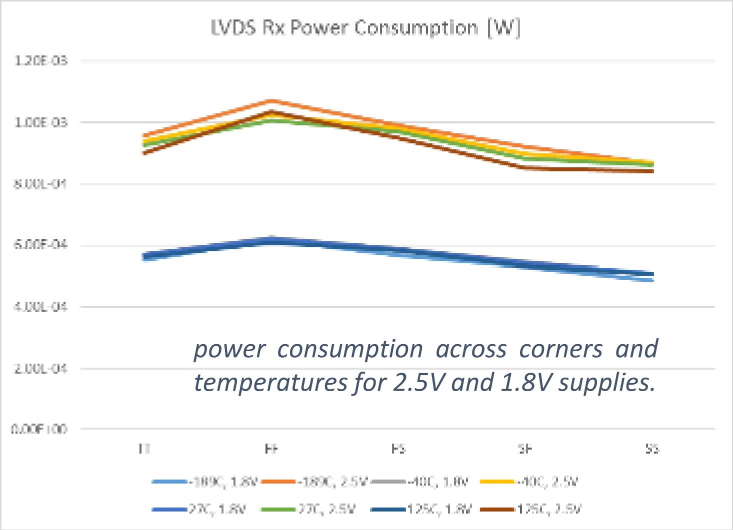
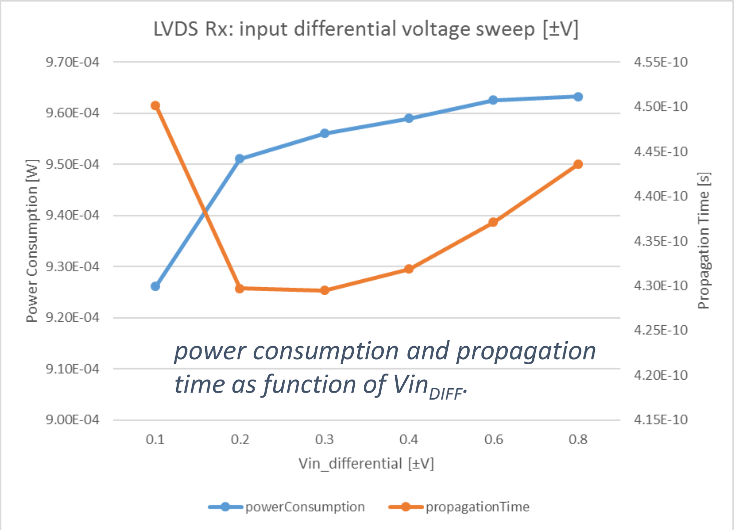
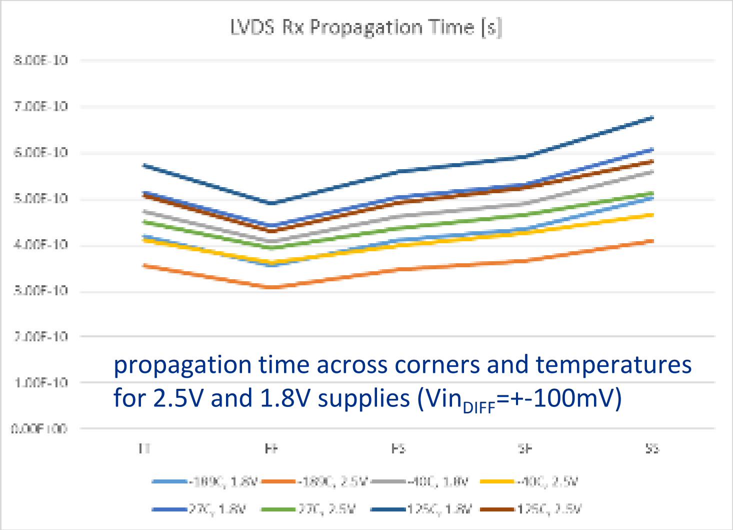


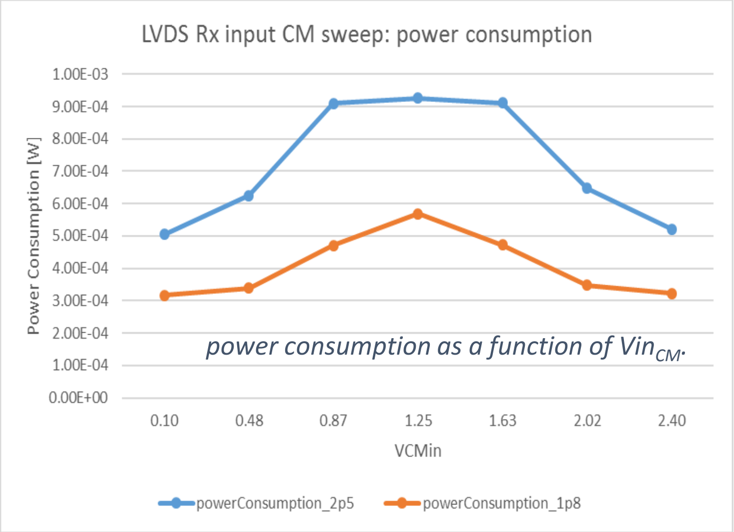
LVDS Rx Performance

Simulations at 1Gbps



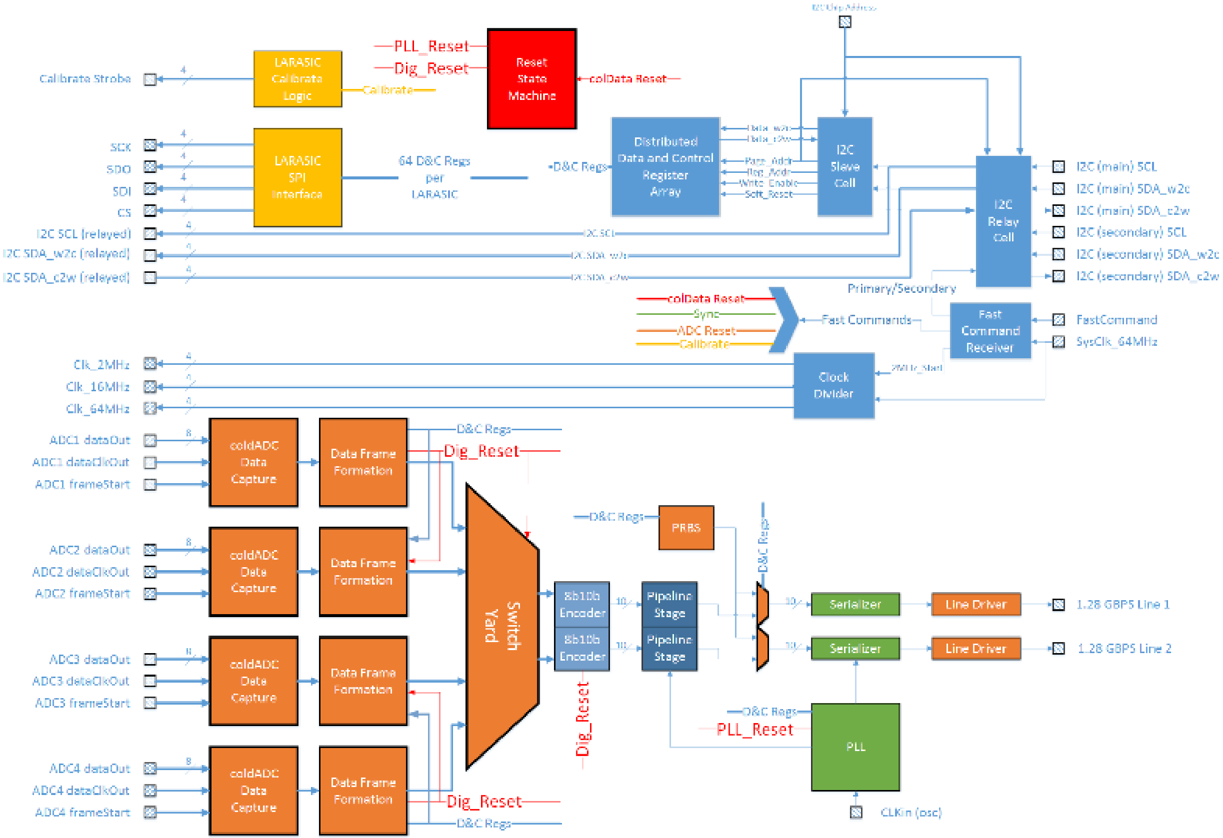






COLDATA

- Responsible for all communication between warm and cold.
- Receives command and control information.
- Provides clocks to the Cold ADC ASICs and relays commands to the LArASIC front-end and to the Cold ADC ASICs to set operating modes and initiate calibration procedures.
- Receives data from the ADC ASICs, reformats these data, merges data streams, formats data packets, and sends these data packets to the warm electronics using 1.28 Gbps links. These links are designed for use with 30 m long cables [1], and include line drivers with pulse pre-emphasis.



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COLDATA main blocks - 1:

I^{2}C Slave Cell: standard single-master, except for

- no clock extension;
- LVDS instead of CMOS (→ bidirectional SDA replaced by two lines);
- 3-word communication (<chipID/page><register address><data>) instead of 2-word communication (<address><data>)

- No reset line: resets through Fast Command Interface (+ one from state of SCL & SDA_w2c to reset I2C to “idle”)

I^{2}C Relay Cell:

- Relays I^{2}C commands from LVDS to CMOS to the internal and the Cold ADC’s I^{2}C Slave Cells
- Can switch between primary and secondary I^{2}C lines (for reliability) via Fast Command Receiver

Fast Command Receiver:

- Serial input for commands synchronous to the 64 MHz system clock: *Adjust 2MHz Rising Edge, Calibrate, Sync, Switch I2C, COLDATA reset.*

Clock Divider: creates the 2MHz and 16MHz clocks from the 64MHz

COLDATA main blocks - 2:

LARASIC Calibrate Logic:
controls the generation of the Calibrate Strobes required by LARASIC in response to the factors and mode commands downloaded to COLDATA

LARASIC SPI Interface:
LARASIC uses a custom control interface for its configuration bits, in an SPI-like configuration. It also implements certain actions like Soft Reset and Hard Reset depending on the state of the four signals. The configuration bits are arranged as one large daisy chain that cannot directly be read out. Instead, to ensure transmission of any new configuration, data must be transmitted twice and read back on the second transmission. The LARASIC SPI Interface in COLDATA implements all the special functions of the LARASIC Interface like Soft Reset and Hard Reset. It also implements a group of 8-bit I2C Control Registers that collectively hold the entire LARASIC SPI daisy chain. Finally, it contains a state machine that when ordered will download the daisy chain bits into LARASIC twice, read back the second transmission and compare the bits read back with the bits transmitted.

ColdADC Data Capture: Each coldADC outputs 256 bits of data every 2MHz period. The interface includes a frame start signal, a data output clock and 8 data output lines, all LVDS. coldADC Data Capture has the job of grabbing whole 256 bit data frames and passing them forward to the Data Frame Formation block.

COLDATA main blocks - 3:

Data Frame Formation:
Every rising edge of the 2MHz clock, the data from two coldADC Data Capture blocks must be stripped of unnecessary bits, packed into a data frame, given a header and given a CRC. The block also implements a Pseudo-Random Binary Sequence (PRBS) that can be used to test the line drivers.

Switch Yard:
For the time being, a place holder only. It may be used to redirect data frames to different line drivers in the event of a loss of viable cables over the lifetime of the experiment.

Serializer:
high-speed parallel to serial conversion (10 to 1)

Line Driver

PLL: This block generates the 128MHz readout clock and the 1.28GHz serializer clock.

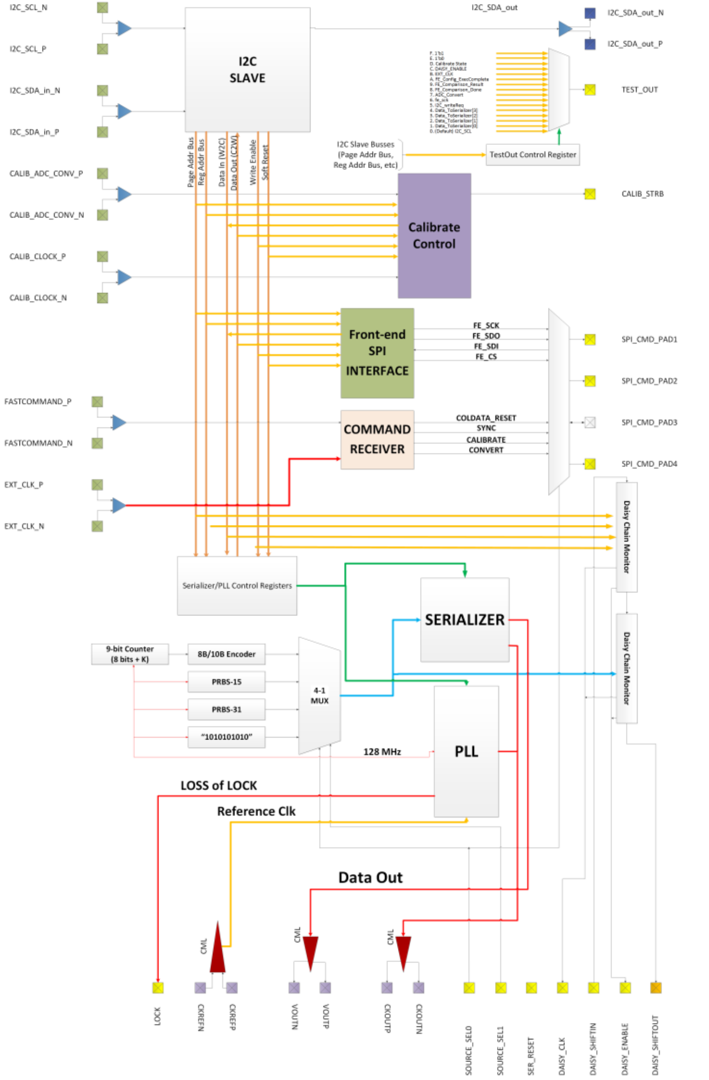
CDP1: COLDATA first Prototype

To advance the project at a time when the specs for COLDATA were still changing, we designed a <u>prototype chip with all the blocks certain to be included in the final full chip</u>.
Left out are the blocks related to the framing of the data from the ADC.

Main blocks:

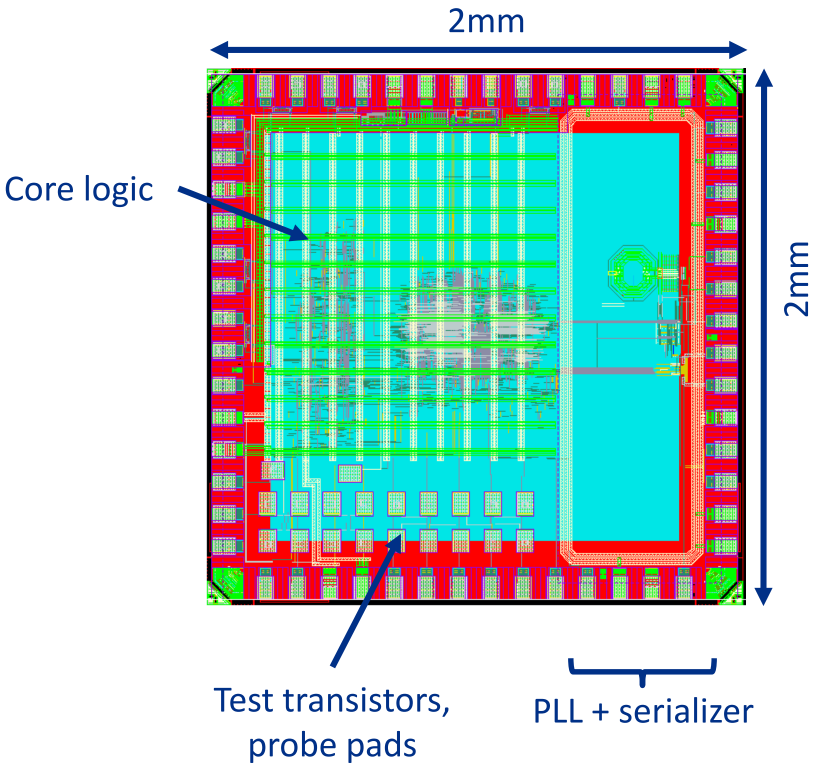
- LVDS Tx & Rx
- Slow-control I2C and SPI
- Calibration logic for the front end ASICs
- Fast command receiver
- 8b10b encoder
- 1.285 Gbps serializer
- PLL

Digital logic verified through Assertions and UVM
All the registers in the digital logic (I2C, calibration, fast command etc') are triplicated



CDP1: COLDATA Prototype 1

- 2 x 2 mm, 65nm 9metal
- Received and tested in mid-2017
- Fully digital assembly



Fermilab Test Setup

DUT on **Cold Board** and interface electronics on **Warm Board**

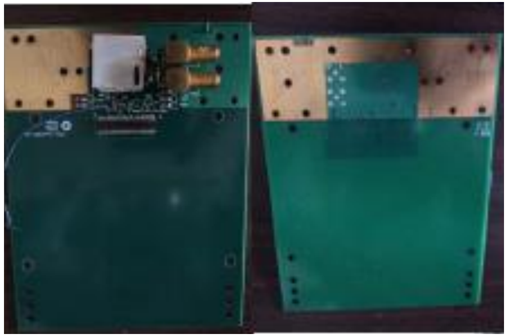
National Instruments Test System

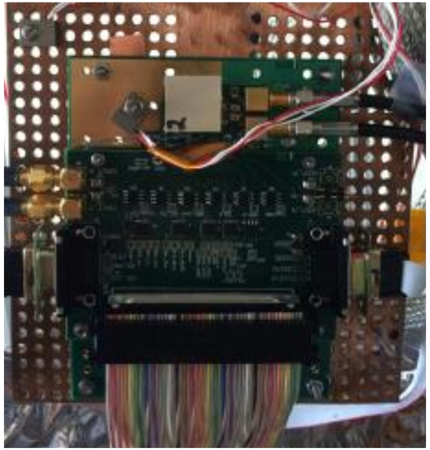
- **PXIe crate**: NI PXIe 1085
- FPGA modules: NI-6583 (Digital I/O adapter module) on NI PXIe-7976R (FPGA)
- Source Measurement Unit (SMU) modules: NI-4141 and NI-4145
- Custom **LabView** VIs

Tektronix Oscilloscope: DSA72004C **Digital Signal Analyzer** with jitter analysis software

Agilent Oscilloscope MSO7104B

Fermilab 14^{th} floor **cryostat** (+ LN2 dewars)





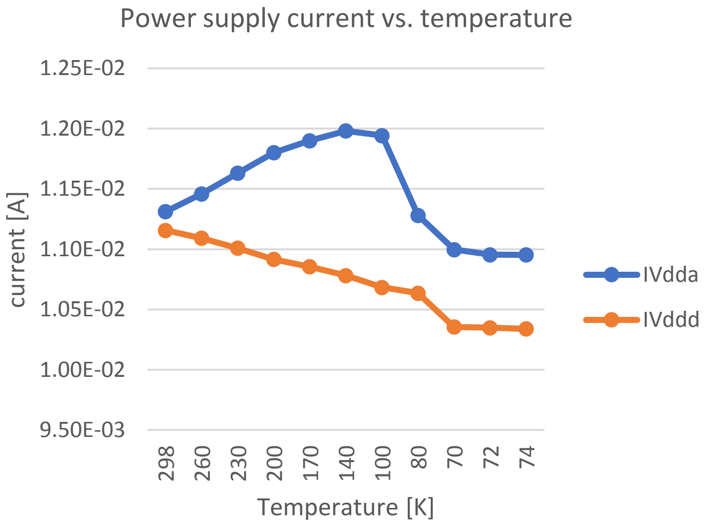
CDP1 Test Results

1. Quick verification of operation in LN2 bath in dewar
   - checked power: negligible increase in power supply currents
   - checked I2C communication – W/R registers

2. Verified operation at room Temperature
   - Serial (I2C) Slave
   - PLL/Serializer (Xiaoran, SMU)
   - Fast Command Receiver
     - All 4 Fast Commands were received and appropriate response was found at the SPI CMD Pads.
   - Calibrate Control
   - Front-end SPI Interface

3. Verified operation at 77K Temperature

   All operations at Room Temperature repeated
   Tests were repeated with the power cycled off and then on
   Tests were repeated with the power cycled off and then on after 5 minutes



Example of monitoring of the power supplies as temperature was lowered in cryostat (the last two points taken after power down and power up, without waiting and after 5 mins respectively)

Conclusions and Future Developments

- COLDATA designed in 65 nm CMOS using “cold” transistor models based on data collected by members of the FNAL, BNL, and SMU ASIC groups.
- A special library of standard cells, based on these models and using a minimum channel length of 90 nm, was developed by members of the FNAL and UPENN groups, to eliminate the risk posed by the hot carrier effect.
- **Both the models and the standard cell library can be made available upon request, provided the NDA with Foundry is in place.** Fermilab could manage and maintain such library in a centralized database.
- The key circuit elements of COLDATA, including the control interface and the PLL and serializer, were prototyped and tested successfully in 2017. The serializer and the PLL have been extensively characterized. All other blocks were also proven functional at both room and LAr temperatures.

- A test structure for speed and stress tests of the LVDS Tx and Rx is expected soon
- Submission of COLDATA is expected later this year.

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