A 256 SPAD readout ASIC with embedded digital signal processing for time of flight positron emission tomography

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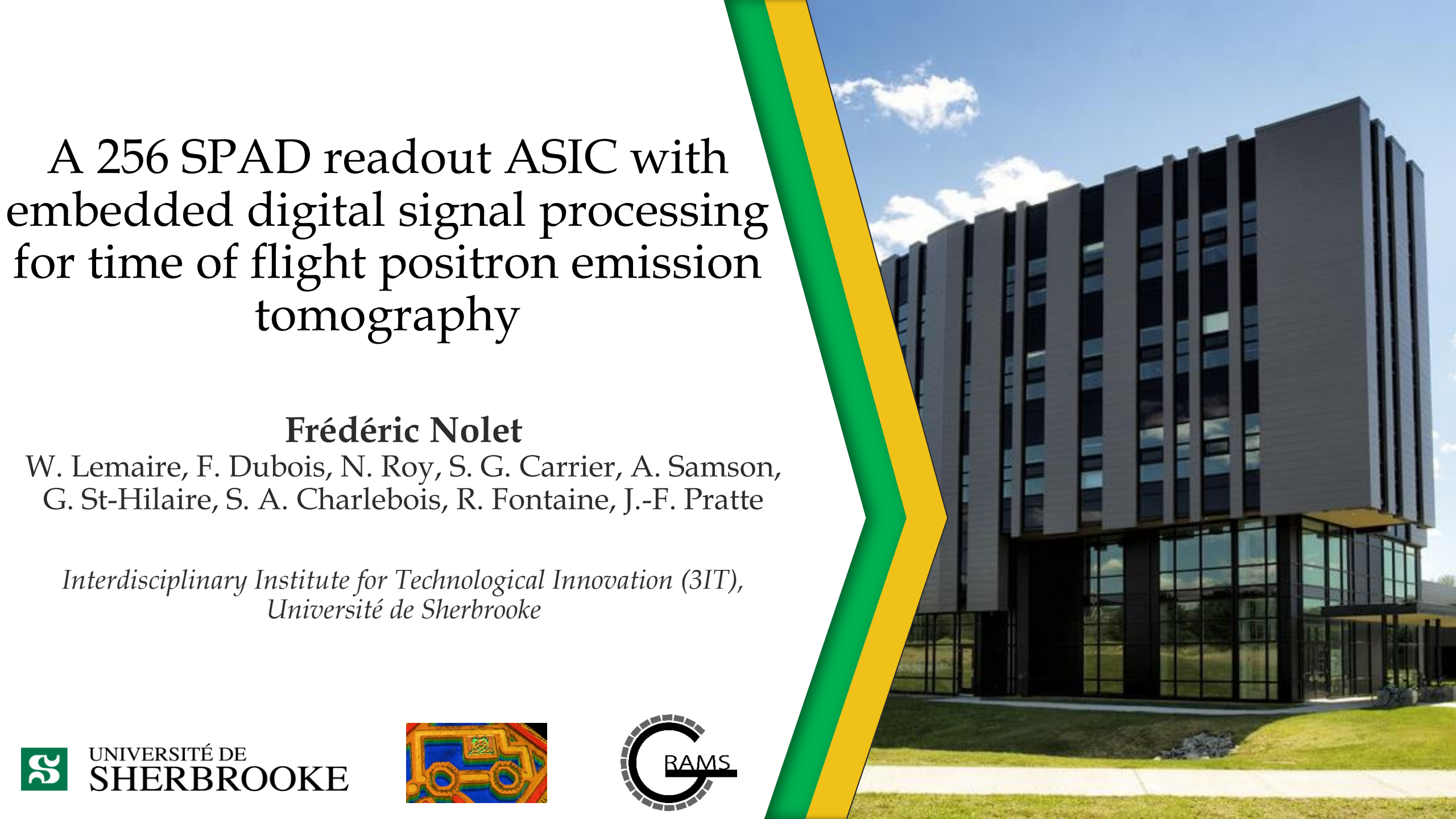

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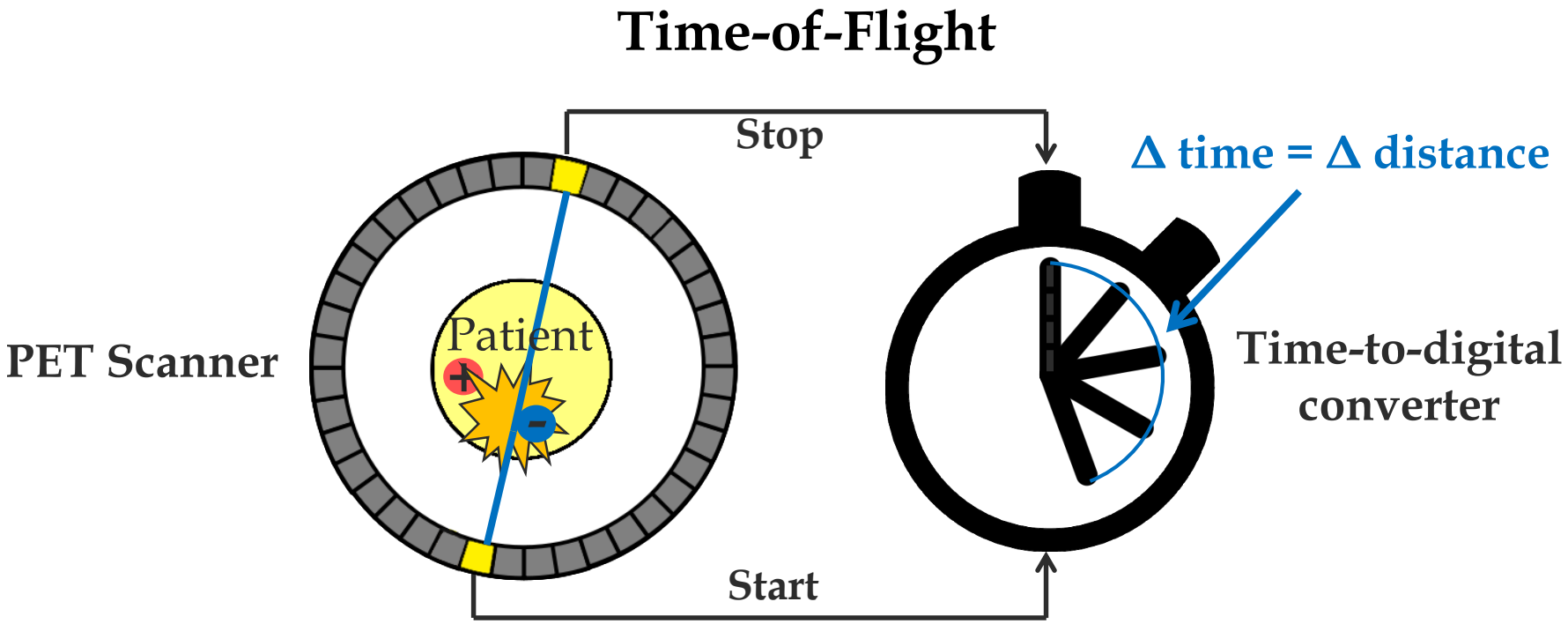
RAMS

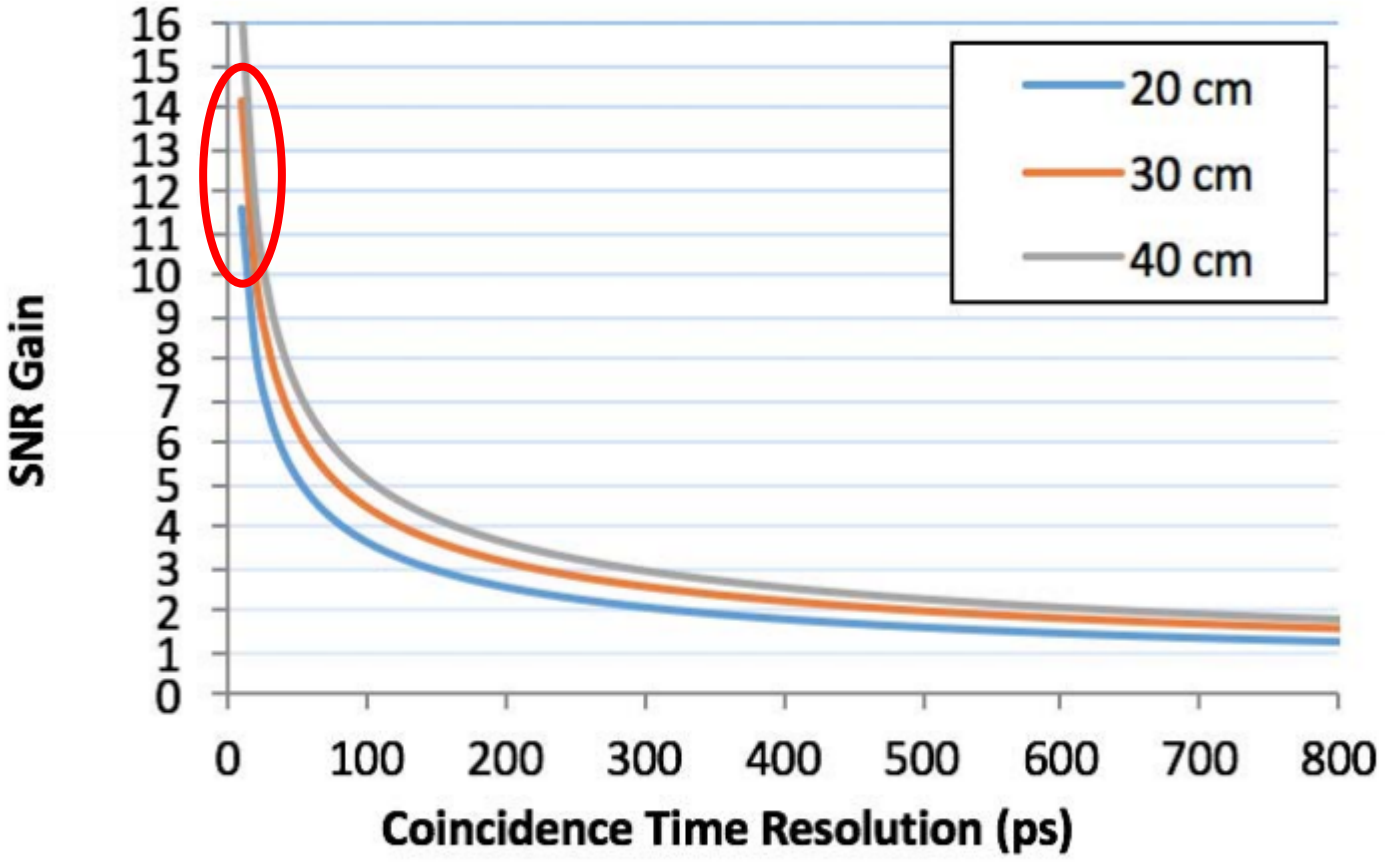
Introduction Time of flight for PET



10 ps coincidence timing resolution (CTR) => 1.5 mm of precision

SNR gain as a function of the CTR

- In our case, a 10 ps CTR would represent a CNR gain of **>10** in the image
- Could lead to real time imaging in PET
- Many challenges:
  - Scintillator with prompt photons
  - Photodetectors and **electronics** with 10 ps SPTR (Single Photon Timing Resolution)



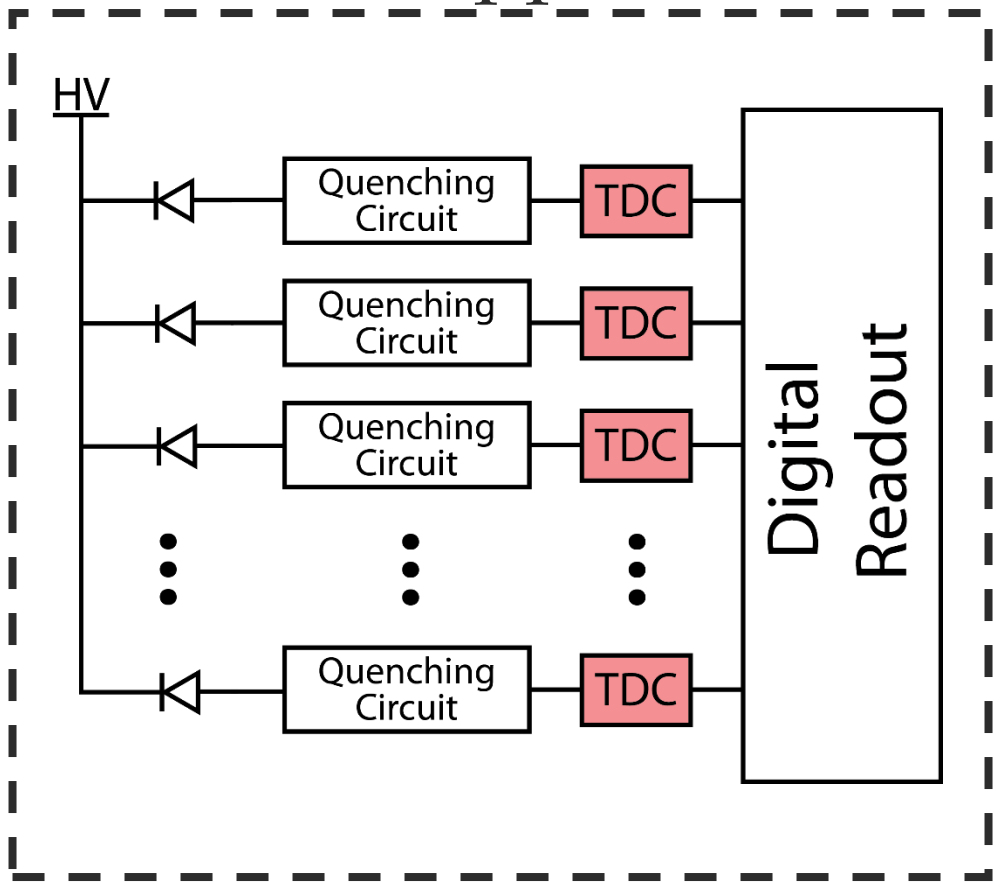
P.Lecoq, 2017, IEEE TRPMS

Architecture for the detector

Advantages
- TDC per SPAD
- Low SPTR per pixel
- SPAD to SPAD skew correction

Cons
- Low fill factor
- High complexity

Our Approach



Digital SiPM

3D digital SiPM with CMOS 65 nm readout

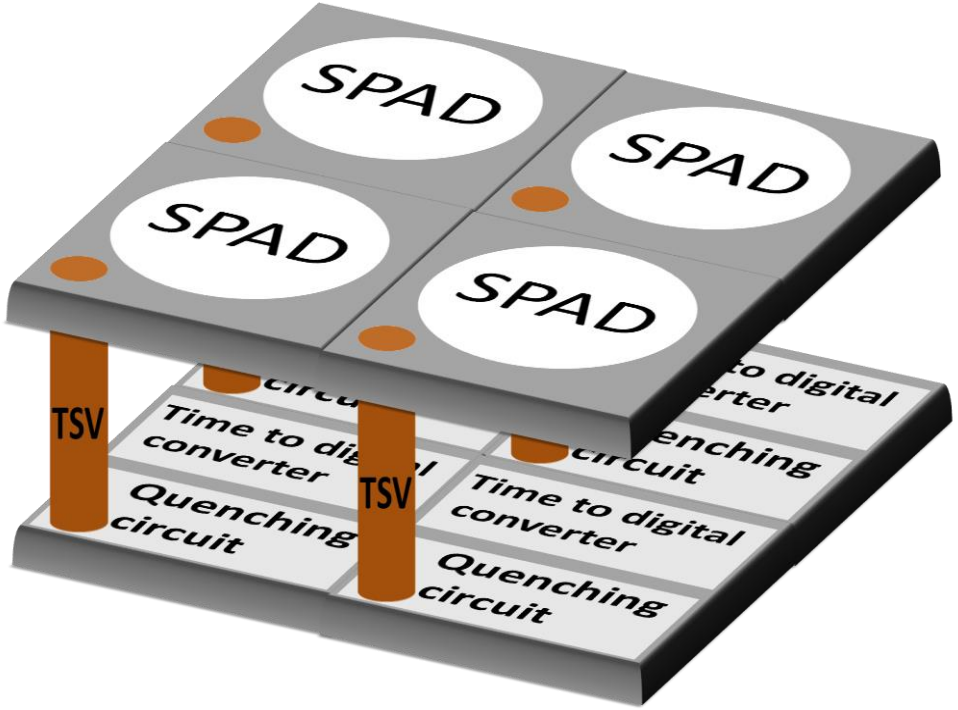
3D Integration

- High fill factor
- Heterogeneous technologies integration

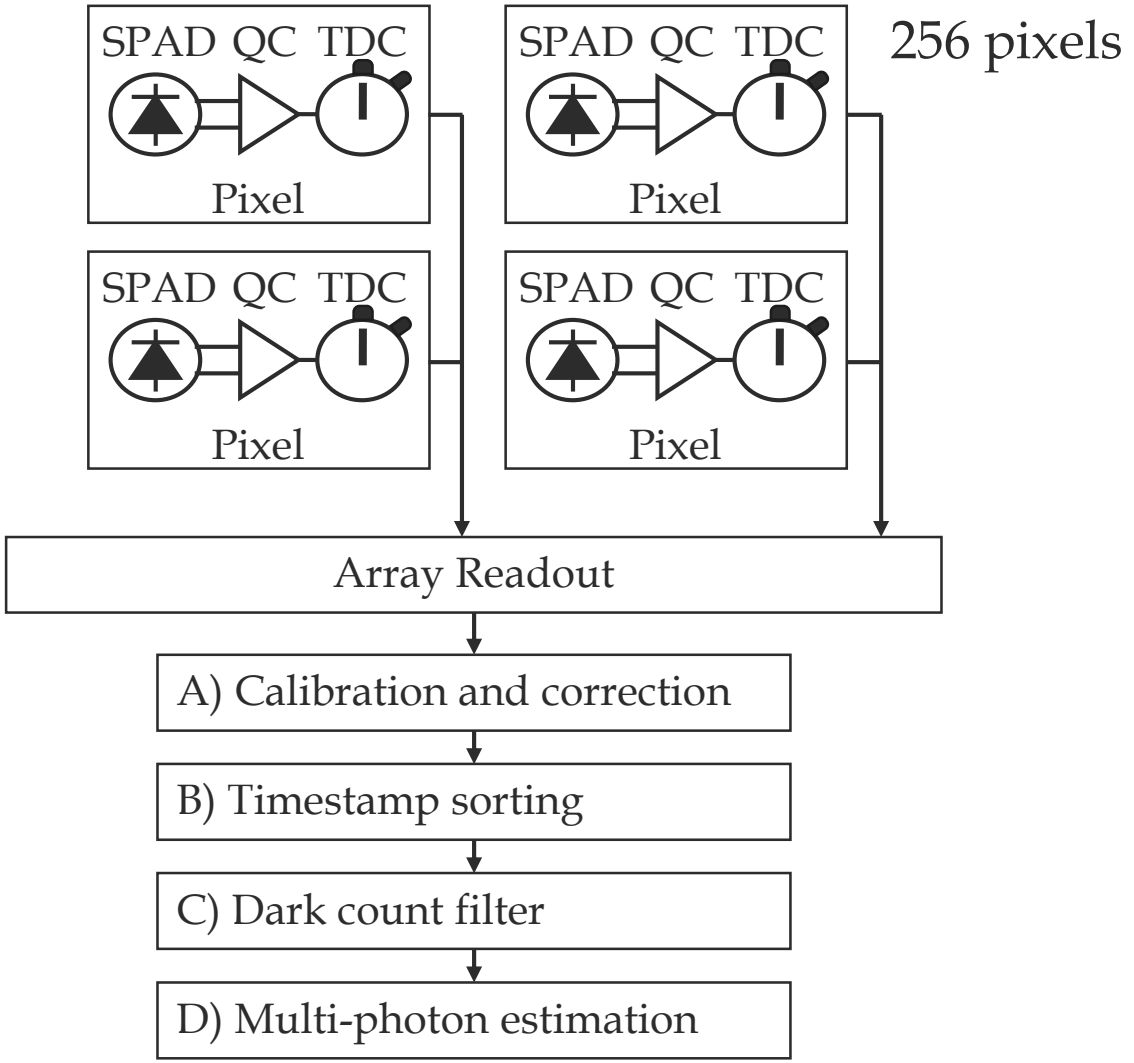
Teledyne Dalsa
Custom process

TSMC CMOS 65 nm

256 SPAD readout ASIC



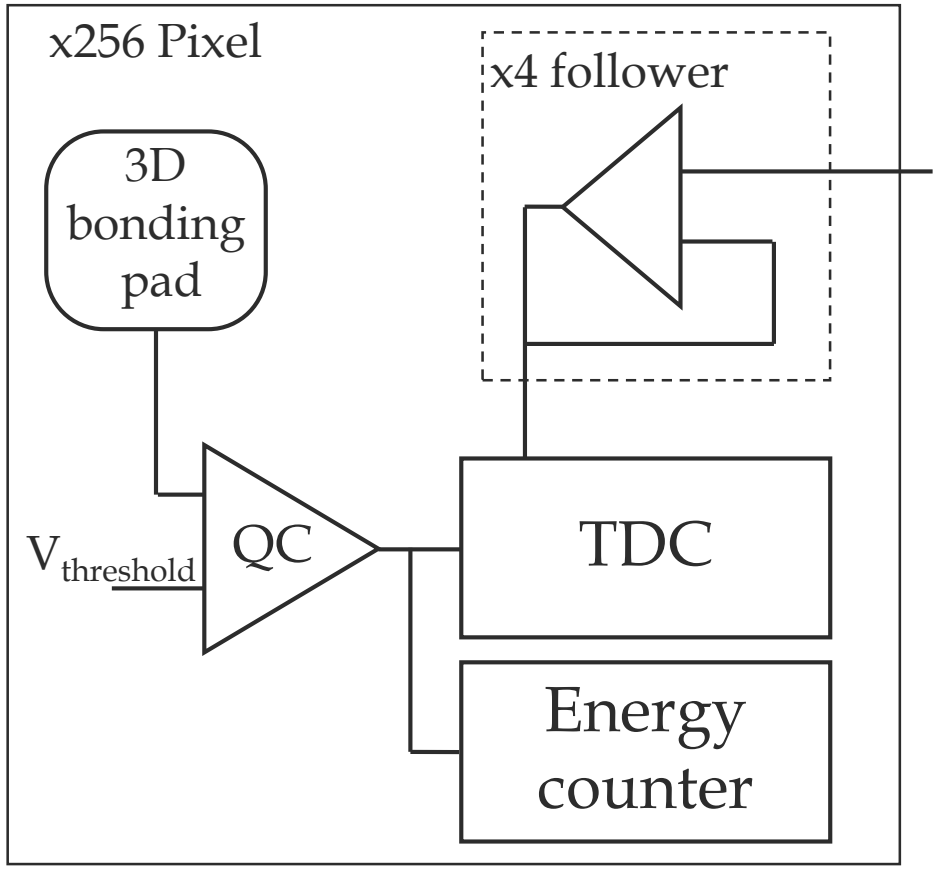
Digital SiPM readout architecture



- Informations per packet:
  - Pixel address
  - Timing of the first photon detected
  - Photon count over period of time

- Trigger mode
  - Time driven
    - Camera mode, timing of the first photon + photon count at a fixed time rate
  - Event trigger
    - X columns must trigger to detect an event
    - Energy count for an adjustable period of time

Pixel overview



Quenching circuit

- Optimized for timing jitter and low walk
- Based on a operational amplifier in open-loop

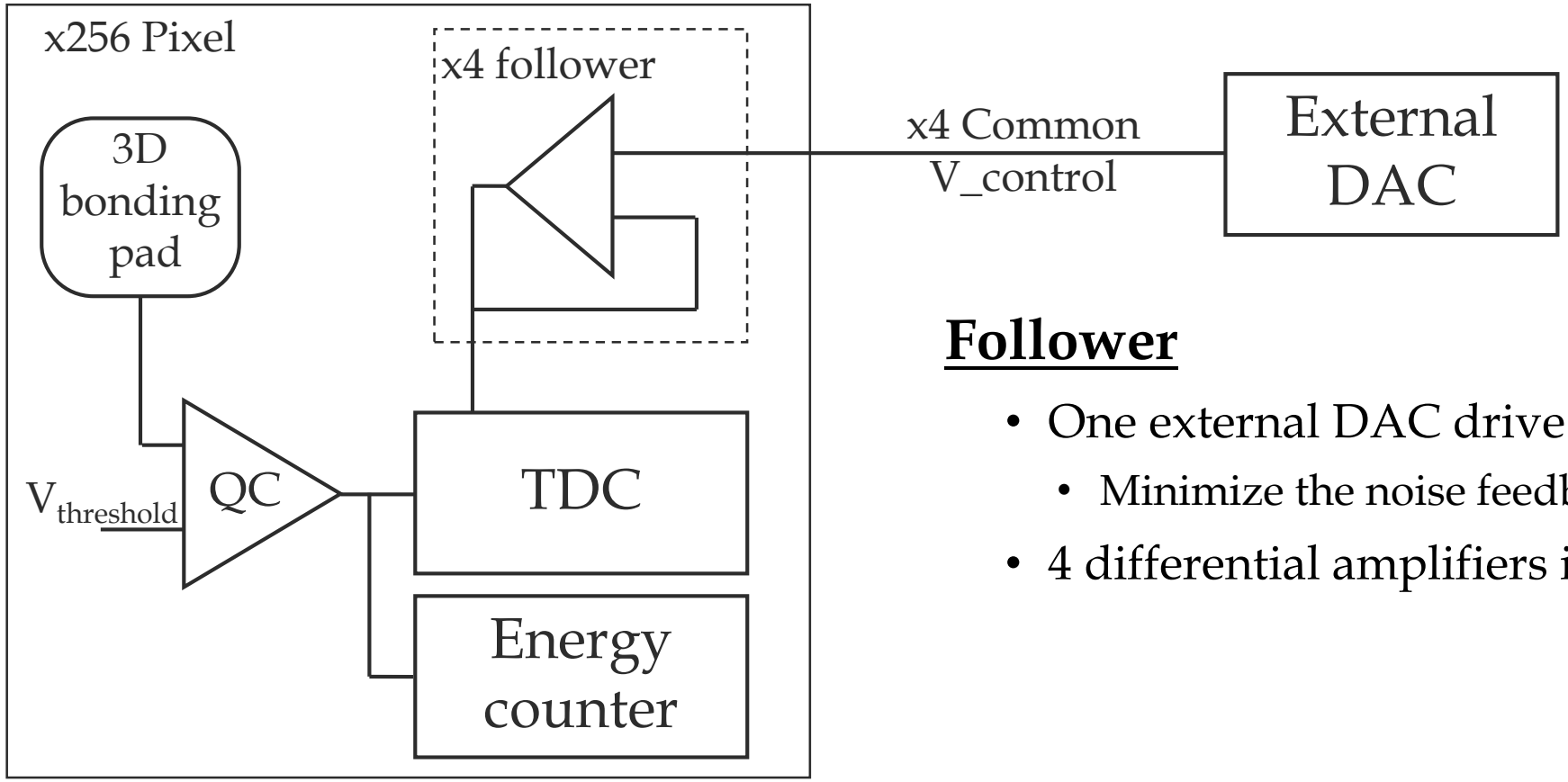
Time to digital converter

- Ring oscillator-based Vernier with single coincidence circuit

Local energy counter

- 8 bits depth

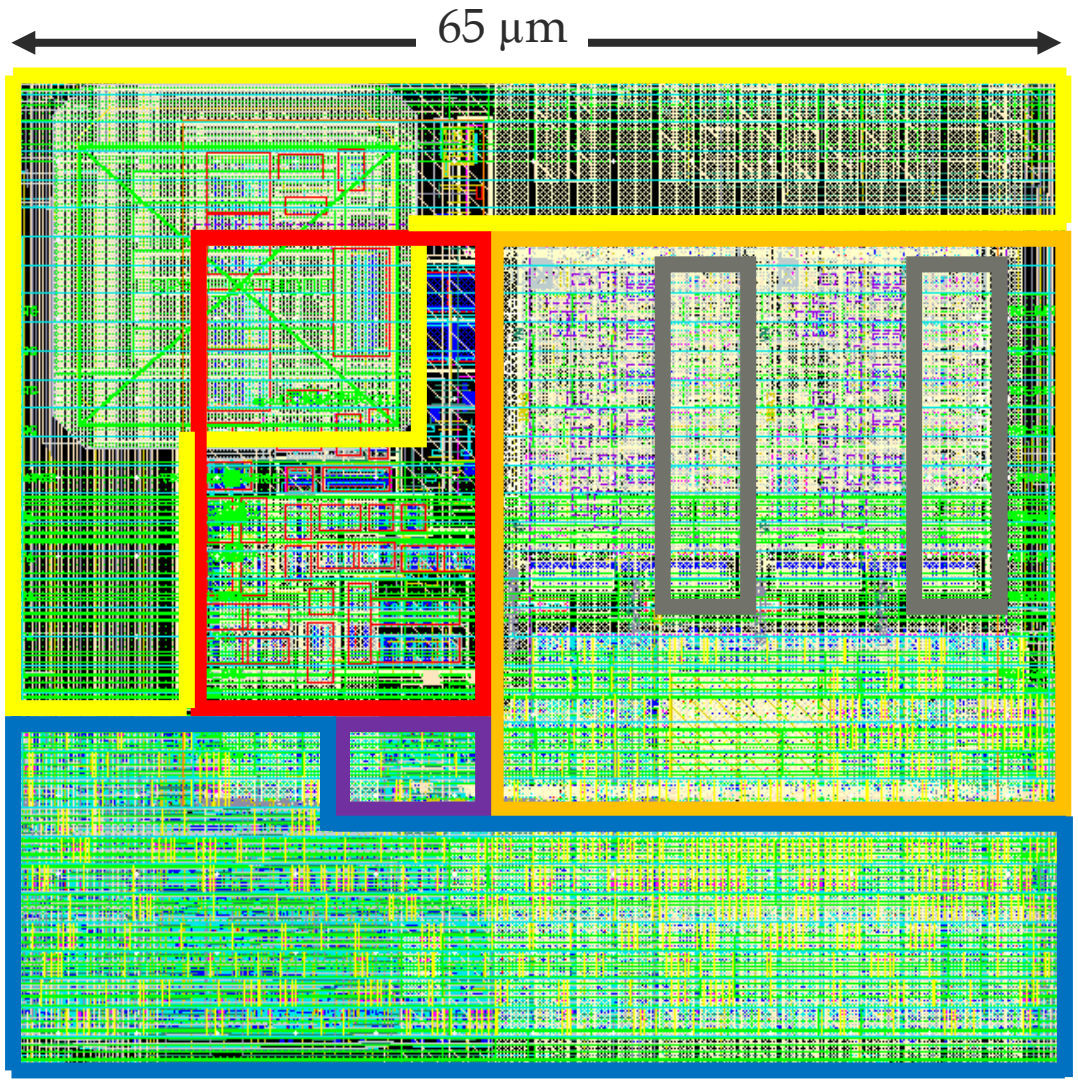
Pixel overview



Follower

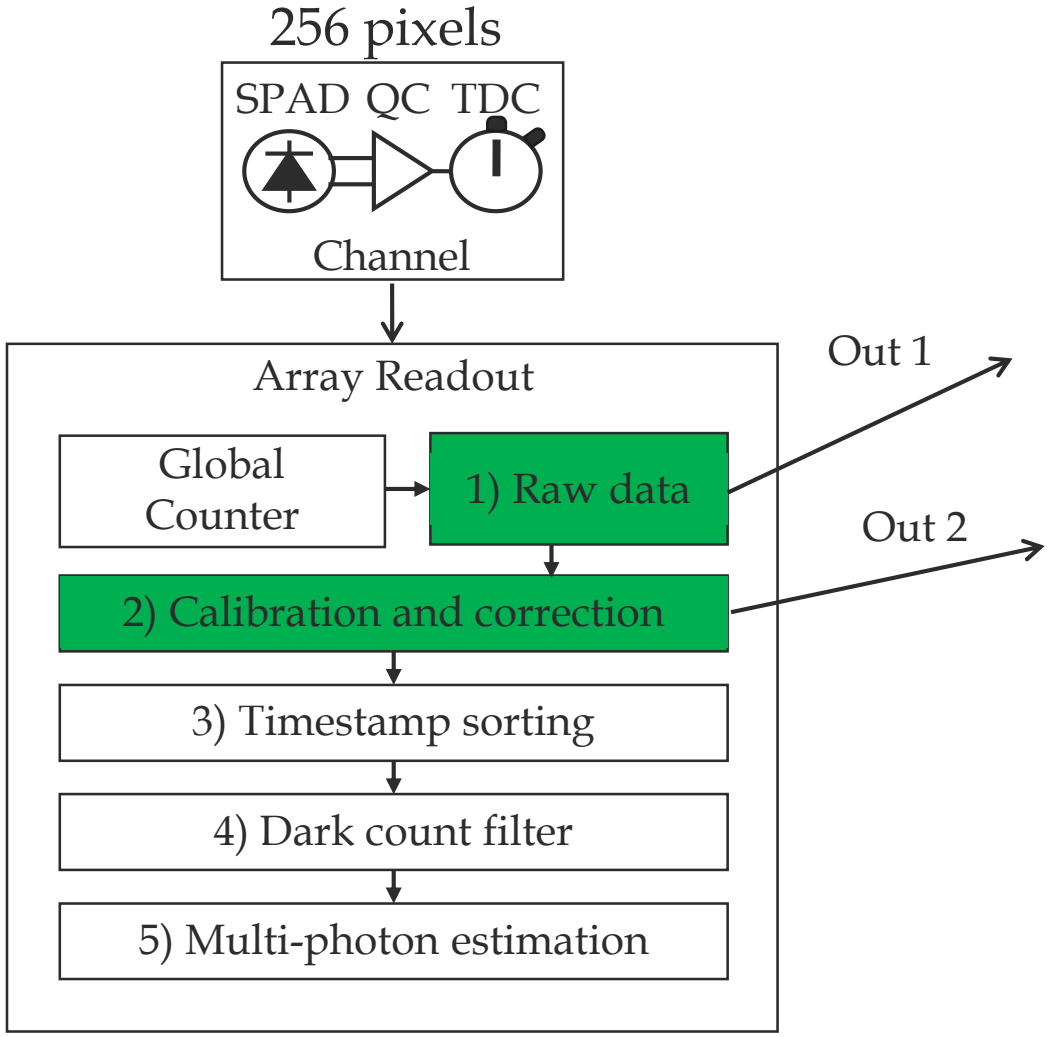
- One external DAC drive the 256 oscillators
  - Minimize the noise feedback from the oscillator
- 4 differential amplifiers in follower configuration

Pixel overview



Circuit	Power consumption (µW)	Area (µm²)
3D bonding and ESD clearance	-	950
QC	180	740
TDC	160	1000
Energy counter	5	80
Follower (x4)	88	400
Space available for digital circuit		**1100**
Pixel	443	4225

Array readout – Raw Data



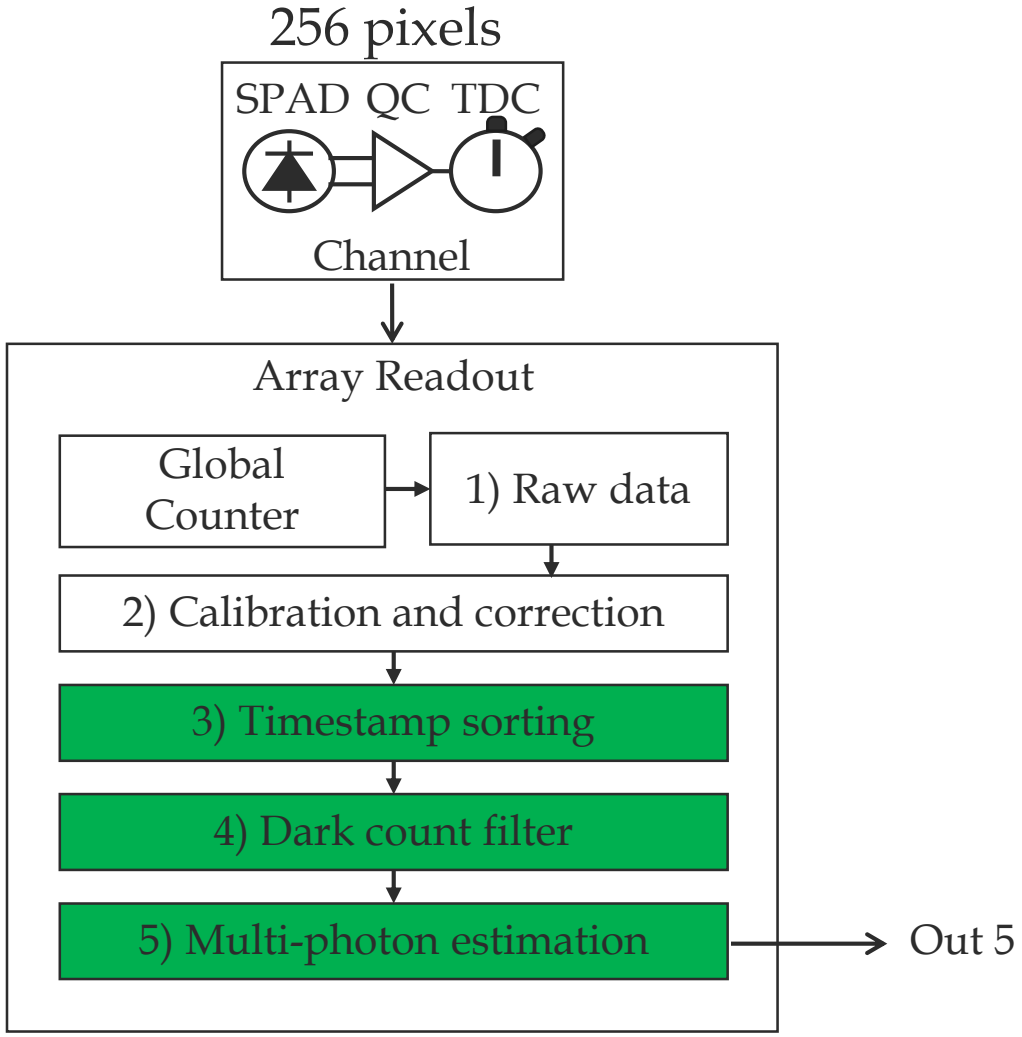
1st Mode of data transmission

Raw data information

- Raw data (address, timestamp, count)
- Corrected raw data
  - TDC LSB correction (look-up table)
  - Skew correction (look-up table)

- **Measured bandwidth**
  14 kcps for 1.1 × 1.1 mm^2

Array readout – Raw Data



2nd Mode of data transmission

- Multi-photon time estimator based on BLUE (Best linear unbiased estimator)
  - Sort the 32 first timestamp
  - Filter dark count
- Output is:
  - Timing information of 32 pixels combined
  - Energy (counts) sum of 256 pixels
- **Measured bandwidth**
  0.5 Mcps for 1.1 × 1.1 mm²

Timing jitter contribution within the array

What are the contribution to the SPTR ?

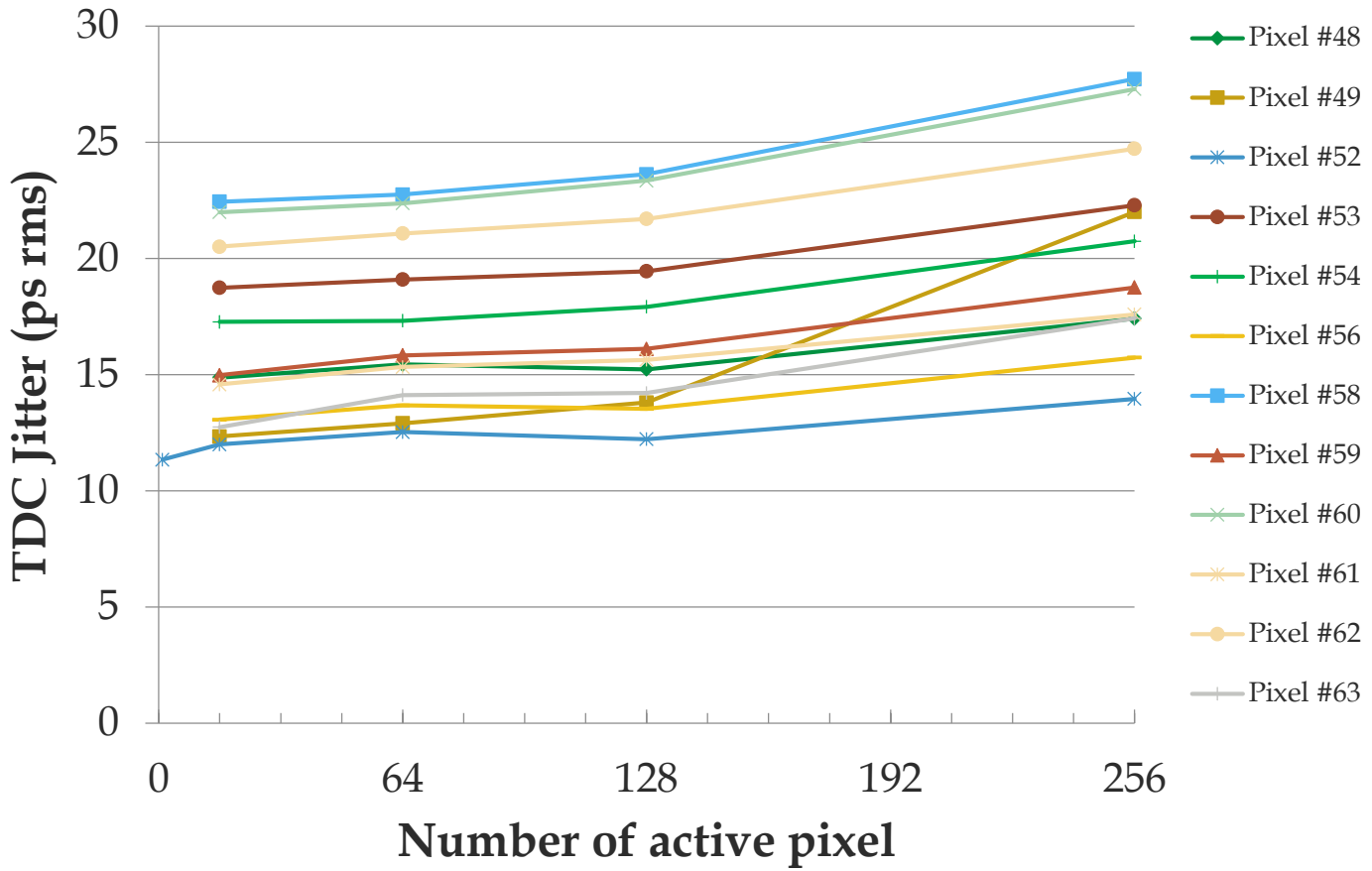
- Timing jitter
  - SPAD ⟶ N/A since the digital SiPM is not yet integrated in 3D
  - QC ⟶ **< 3 ps rms** with a pulse generator at its input
  - TDC ⟶ **8 ps rms** for a TDC LSB of 15 ps
- Array level contribution
  - Noise between pixel
  - TDC LSB non-uniformities
  - Pixel-to-pixel skew

Impact of the number of active TDC on the jitter

What's in the ASIC

- Triple well isolation
- Separated power supplies for TDC – QC – digital core
- Analog buffer in each pixel

- The jitter worsen from 2 ps to 5 ps
  - Small variation from 1 to 64 (less common noise)



TDC LSB uniformity

Fine (ps)																
Coarse period avg			550	Coarse period std			21	Fine period avg			35	Fine period std			17	classe
24	39	20	37	52	13	19	20	50	63	2	20	32	19	3	36	0.00
6	59	46	71	57	19	9	43	47	21	30	45	21	8	15	47	10.00
15	69	41	51	7	45	5	64	44	44	45	31	43	7	19	47	20.00
11	29	24	58	33	52	53	35	29	50	32	38	33	17	17	41	30.00
55	19	42	23	72	24	40	27	31	30	39	35	48	40	49	36	40.00
43	58	62	41	52	40	23	15	57	18	18	36	48	15	39	63	50.00
2	20	3	22	47	20	35	67	36	41	38	46	21	57	45	37	60.00
30	10	11	42	42	21	26	18	42	37	33	42	21	47	30	42	70.00
19	24	51	70	39	23	19	58	52	47	22	49	7	66	3	43	80.00
30	43	36	21	45	58	65	43	44	39	21	32	49	47	7	24	90.00
5	57	26	42	3	43	45	15	46	20	21	4	16	8	64	46	100.00
35	47	31	9	44	27	59	20	38	3	57	12	44	66	46	33	
52	48	45	43	28	34	17	57	9	17	40	21	27	23	45	42	
3	42	26	57	16	38	42	40	4	20	57	52	62	30	37	48	
33	47	20	63	52	51	42	52	57	10	24	50	57	20	51	44	
39	40	57	11	5	59	51	22	3	20	48	30	18	20	60	19	

TDC LSB	**(ps)**
Mean	35
STD	17
Min	2
Max	72

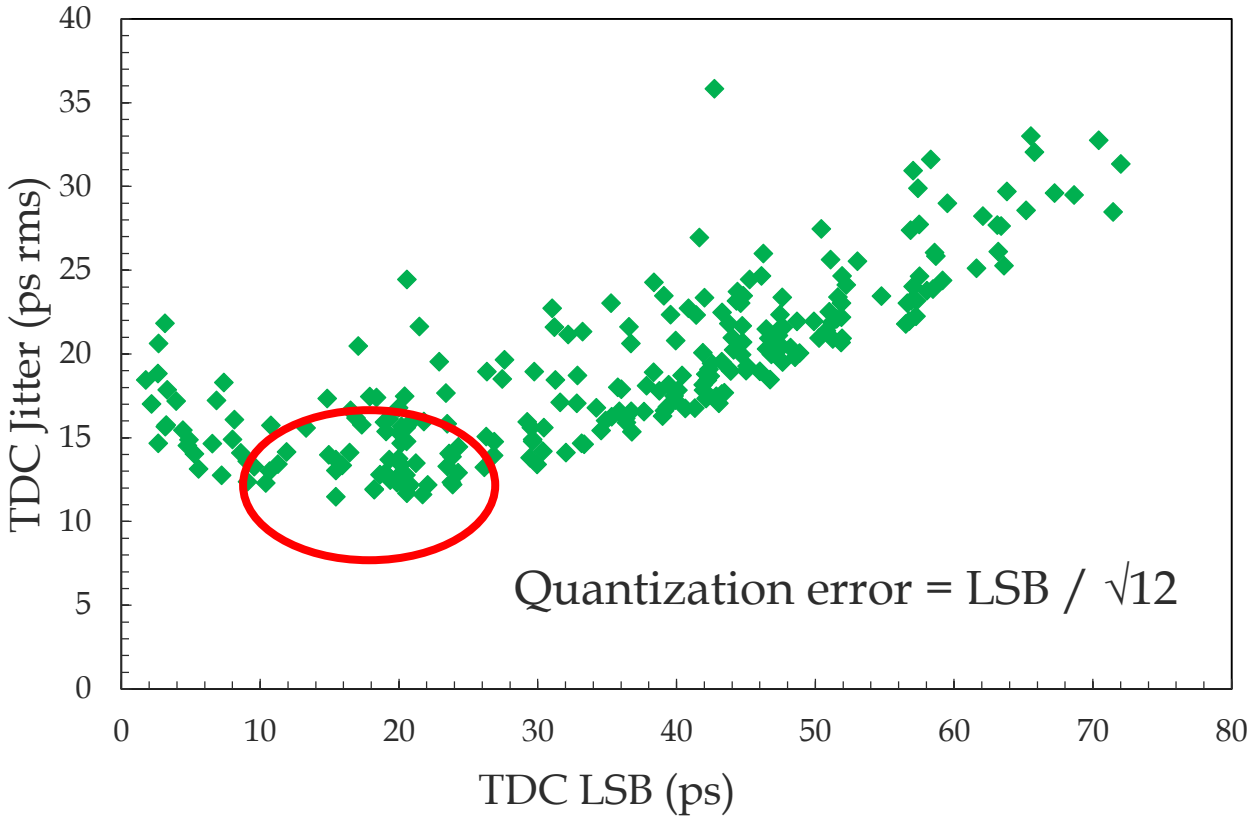
- Same voltage control applied to all TDC
- These non-uniformities are due to the mismatch (simulated)
  - Follower (11 ps std contribution)
  - Ring oscillator (3 ps std contribution)

Impact of the TDC LSB mismatch

- Is the TDC LSB variation a limitation to reach 10 ps SPTR ?
- The TDC LSB impacts directly its timing jitter

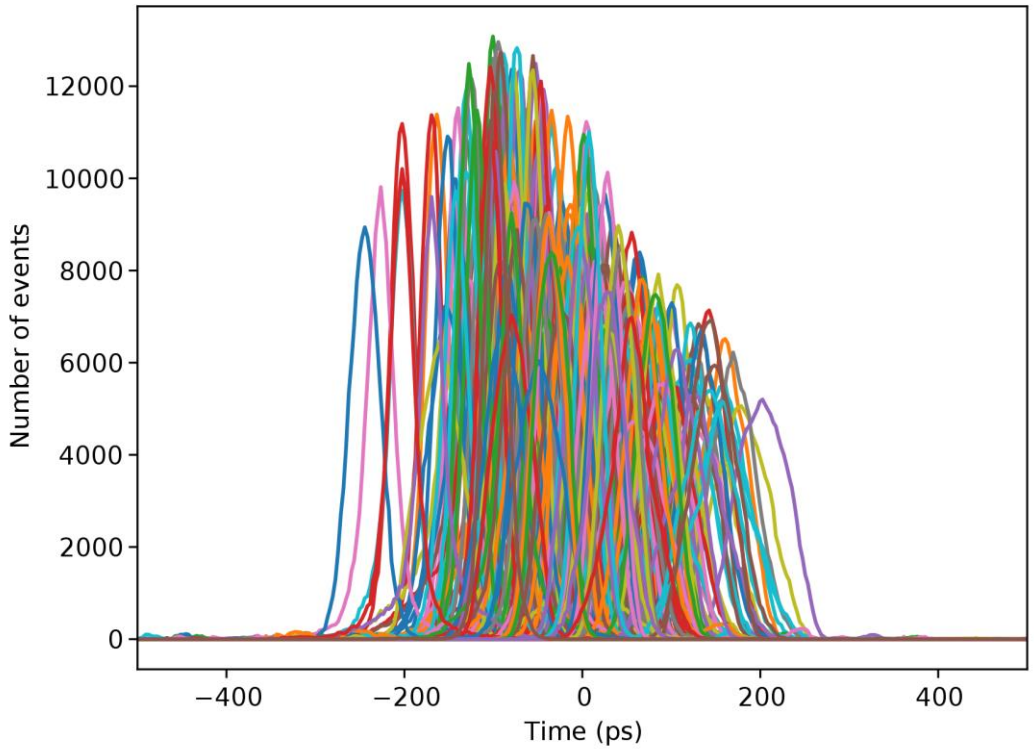
TDC LSB	(ps)
Mean	35
STD	17
Min	2
Max	72

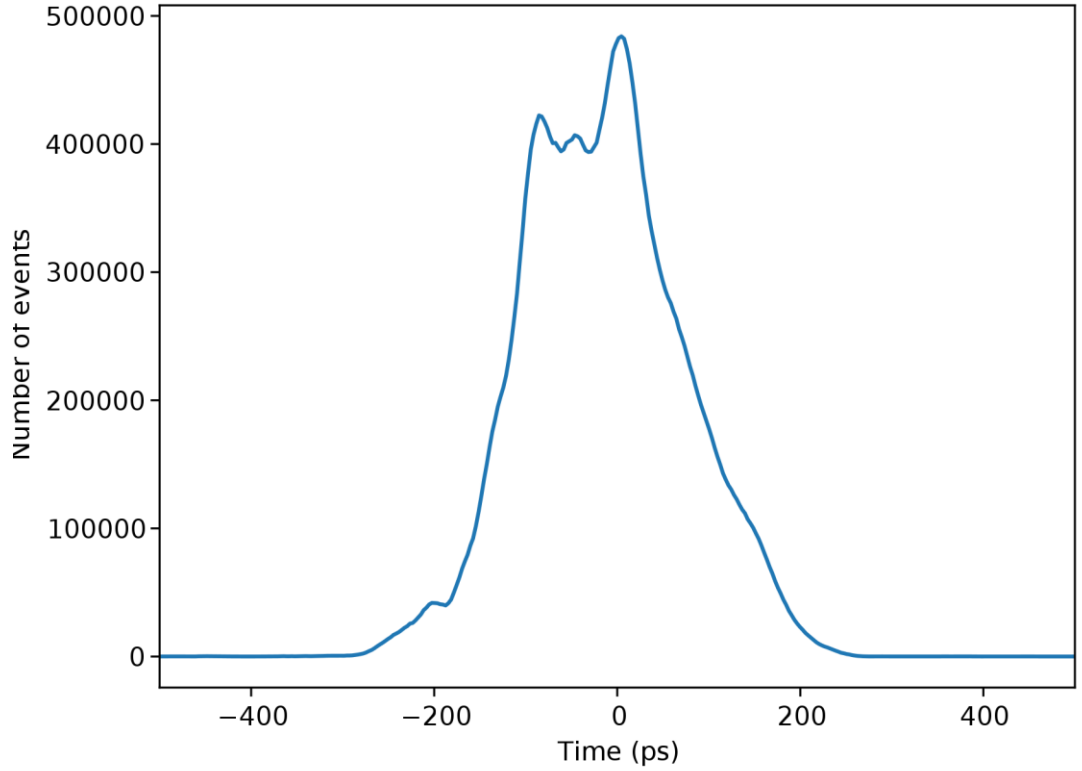
TDC jitter	(ps)
Mean	18
STD	5
Min	11
Max	36



Timing jitter – Array level

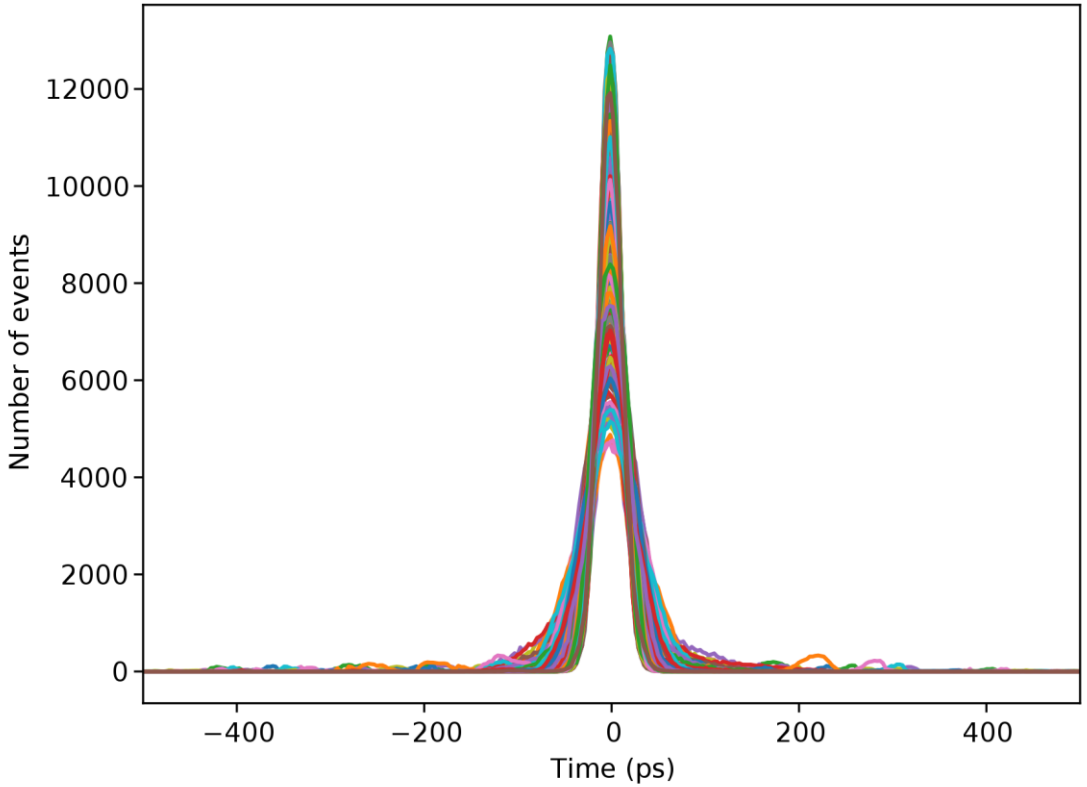
- Skew contribution: clock tree, trigger tree, pixel mismatch
- Skew max of 500 ps within 1.1 × 1.1 mm^2
- Total Jitter is **87 ps rms**



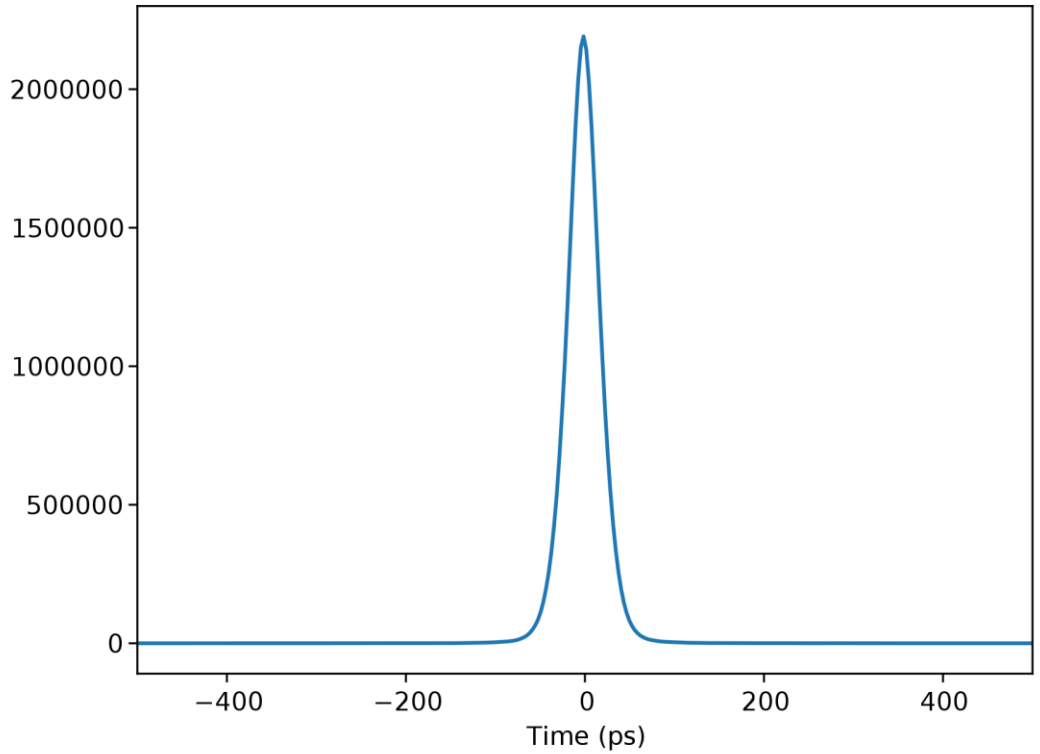


Timing jitter – Array level

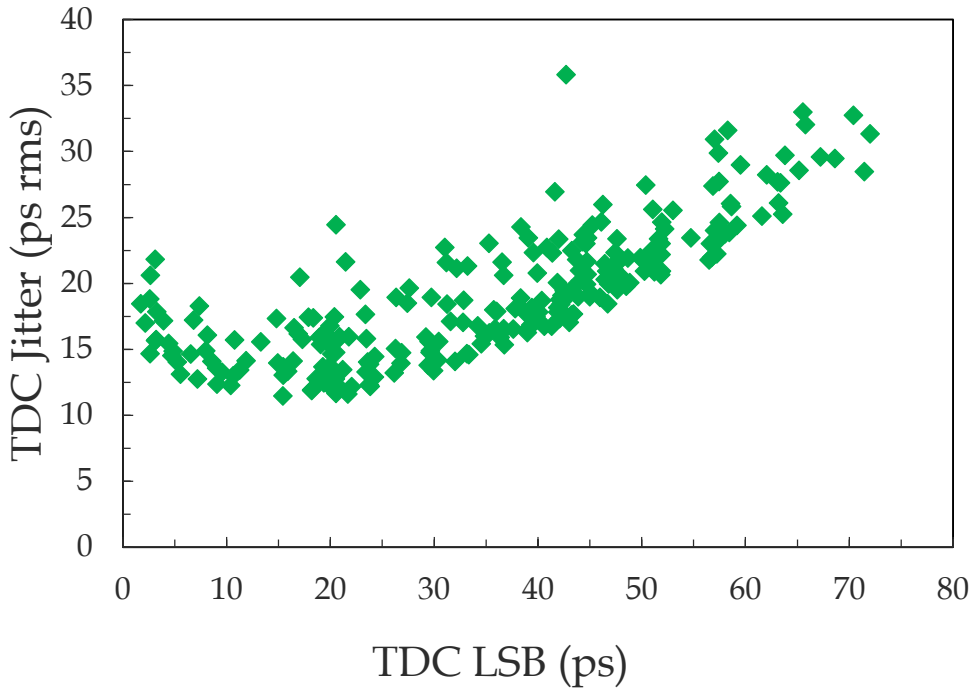
- Since each pixel address is known, it can be characterize and corrected
- Skew corrected (1 ps max skew)



- Total Jitter is **18 ps rms**



Is it possible to achieve 10 ps ?



	TDC LSB (ps)	TDC Jitter(ps)
Mean	34.8	18.0
STD	17.1	4.9
Min	1.7	11.5
Max	72.0	35.8

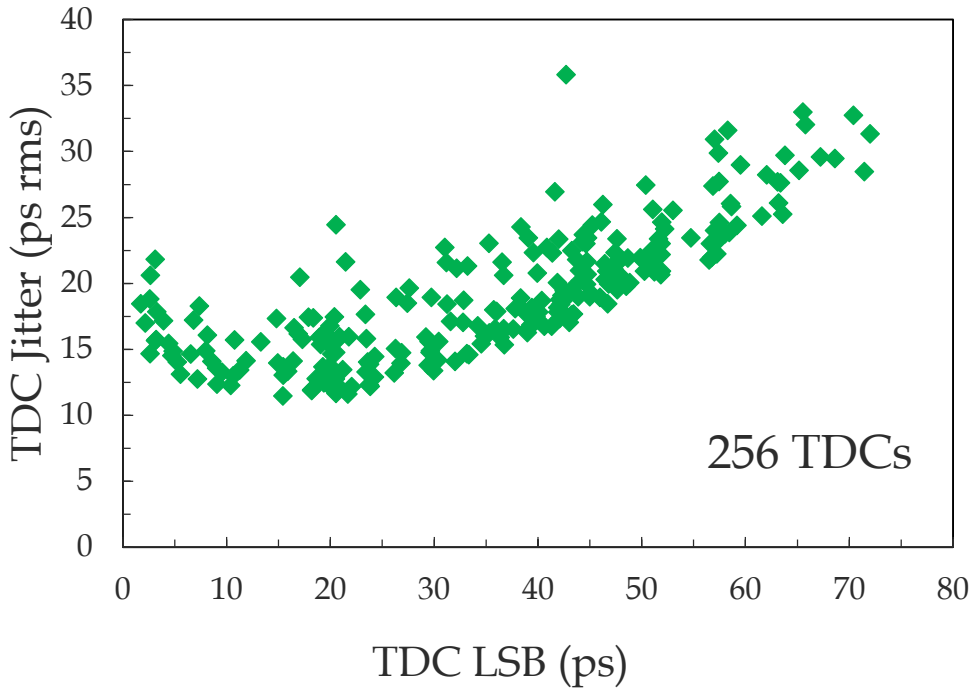
Reduce de TDC LSB mismatch

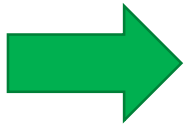
- 17 ps std to 3 ps std (simulated)

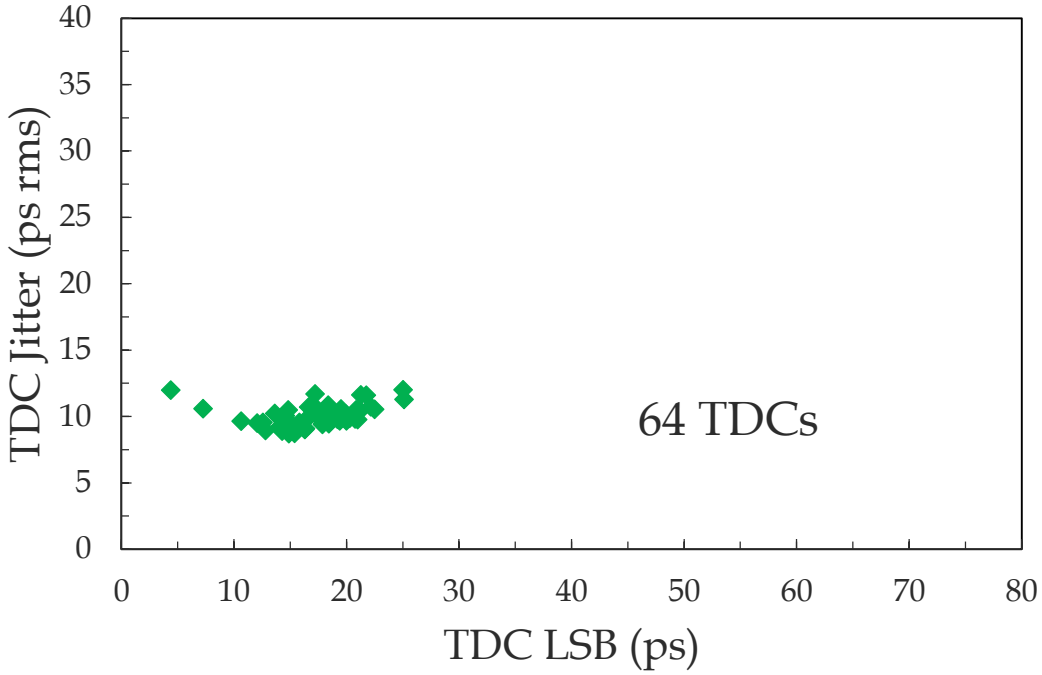
Use of 1 TDC / 4 SPAD (Total 64)

- Reduce common mode noise

Is it possible to achieve 10 ps ?





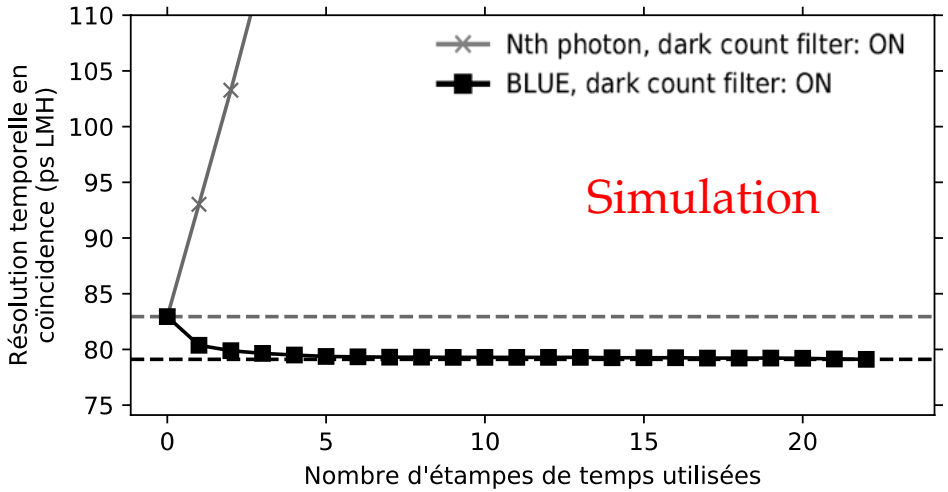


	TDC LSB (ps)	TDC Jitter(ps)
Mean	34.8	18.0
STD	17.1	4.9
Min	1.7	11.5
Max	72.0	35.8

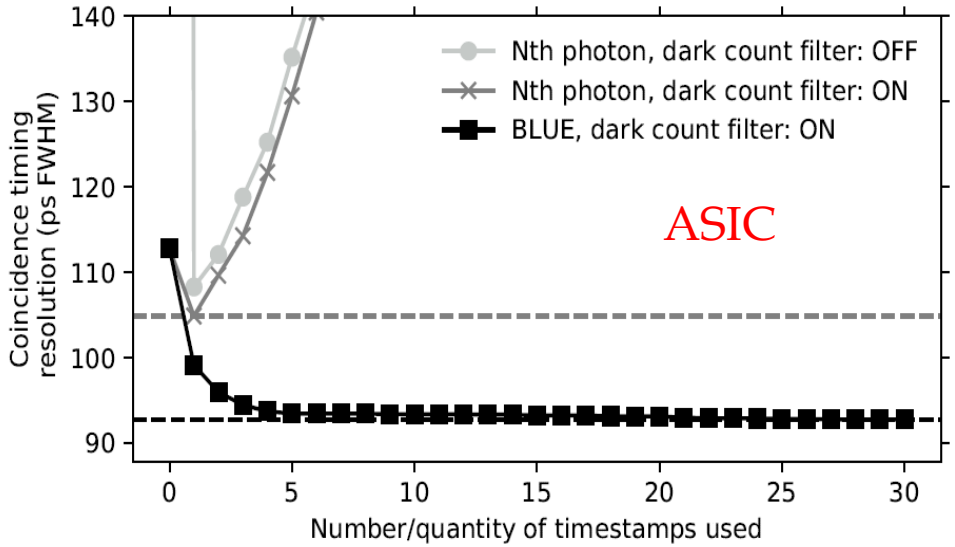
	TDC LSB (ps)	TDC Jitter(ps)
Mean	17.3	9.9
STD	3.8	0.8
Min	4.4	8.7
Max	25.1	12.1

BLUE - preliminary results with electronic readout only

- Simulation with Geant4 for LYSO scintillator statistic
- Load parameter in Cadence to see the impact in Simulation



- Load the parameter in the ASIC and see the impact of the TDC jitter and the post-processing
- Difference = Higher TDC jitter



Future works

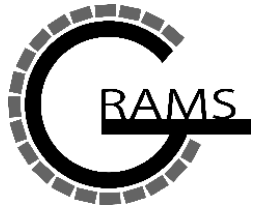
- Minimize the impact of non-uniformities caused by mismatch
  - Review the analog buffer to minimize the input offset
  - Improve the mismatch in the ring oscillators
- Integrate 1 TDC per 4 SPAD to allocated more area for the mismatch consideration AND the impact of common noise (more TDC = more jitter)
- Reduce the power consumption (current: ~200mW per 1.1 × 1.1 mm^2 detector)
  - Eliminate the static power consumption in the QC
  - Modify the TDC architecture
  - Clock gating of the memory and other circuit not used during measurement

Conclusion

- We developed Digital SiPM readout in CMOS 65 nm for Time-of-Flight Measurements with one QC and one TDC per pixel
- With the implemented correction circuit, the timing jitter is **18 ps rms,** close to our objective to 10 ps array wide.
- Each step of the post-processing scheme is fully functional
- Next revision focus
  - Non-uniformities correction
  - Power optimization
  - Calibration system

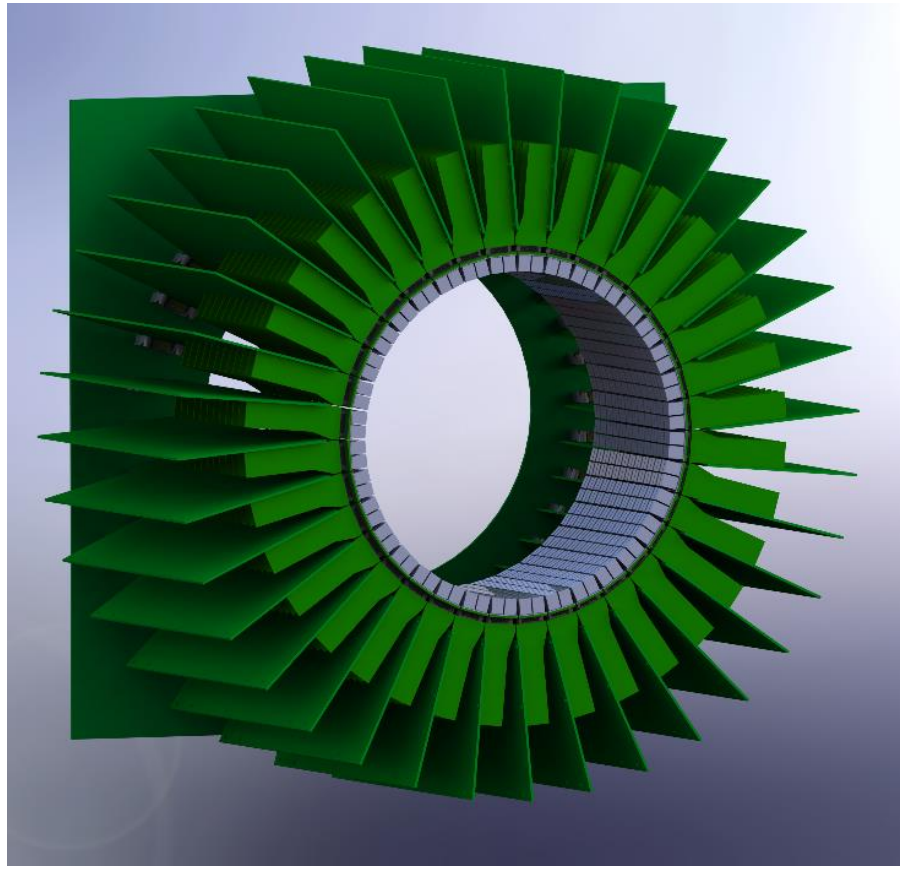
Acknowledgements

- Thank you for your attention



Back-up slides

System integration – Power consumption



LabPET II rabbit scanner

50 000 detectors of 1.1 × 1.1 mm^2

↓

12.8 × 10^6 Pixel @ 65 µm pitch

↓

5.7 kW @ 443 µW/Pixel
4.9 kW for the digital readout
10.6 kW for the total power consumption
(520W for current detectors in LabPET II)

↓

Reduce the power consumption of the pixel
No static power consumption in the QC
New TDC architecture
The digital circuit
Power gating the memory and other circuit not used during measurement

Digital SiPM Overview