ALTIROC
ASIC for HGTD ATLAS

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Front End Electronics - Jouvence – 21 May, 2018

Organization for Micro-Electronics desiGn and Applications

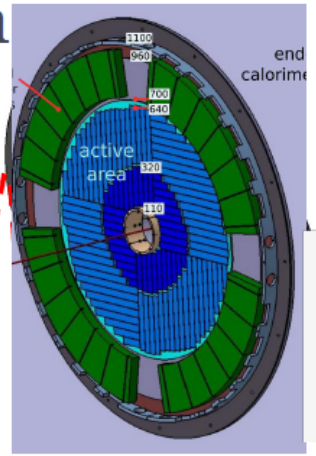
High Granular Timing Detector (HGTD) for ATLAS Phase II

HGTD : 30 ps timing detector for pile up mitigation
Placed in the **forward region**, between the **Inner Tracker** and the **End Cap of EM Calorimeter**

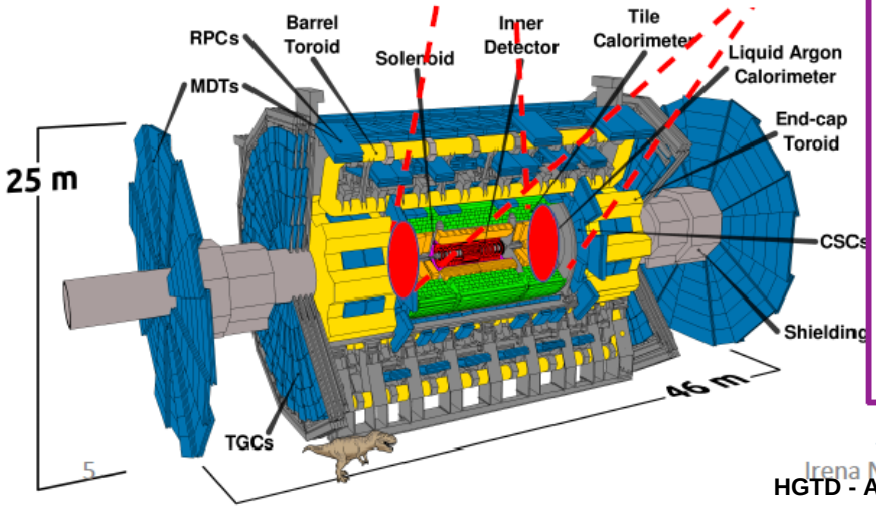
- **Time resolution: 30 ps / track**
- **Granularity (<10% Occupancy)**: 1.3 x 1.3mm^2

HGTD System

- z: +-3500 m
- 2 layers per side
- z MBTS enveloppe: 75 mm

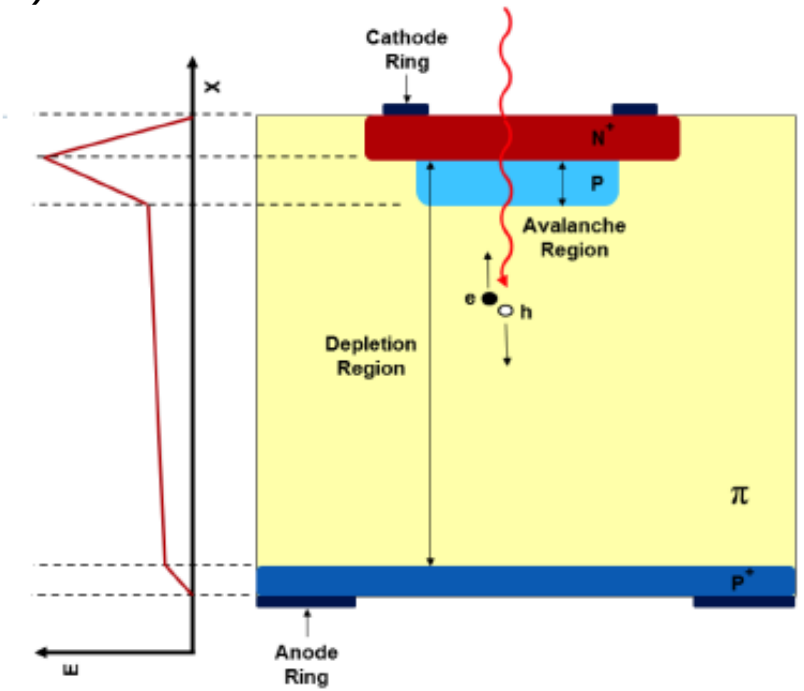


Radial extension:(active area)
- η <4.0 (R = 120 mm)
- η >2.4 (R = 640 mm)

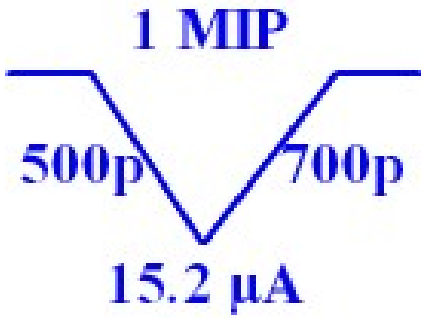


Baseline:
- Time resolution : σ_t=30 ps per track over the lifetime of HL-LHC
- Radiation hardness: 3.7x10^{15} n_{eq}/cm^2, 4MGy
- Granularity : Pad 1.3 x1.3 mm^2 for occupancy <10% pad
- Thickness 50 µm, 35 µm is being studied.
- Nu of channels : 3.54 M
- Active Area: 6.3 m^2

2 disks, 2 layers/disk equipped on both sides with **Low Gain Avalanche Diodes (LGAD)**
n-on-p Si detector with gain (extra highly doped p-layer) and excellent time resolution

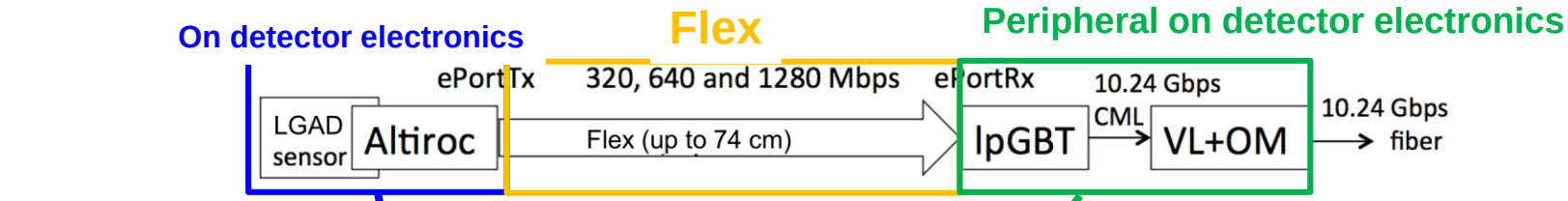


MIP signal with LGAD sensor thickness = 50 µm and G = 20

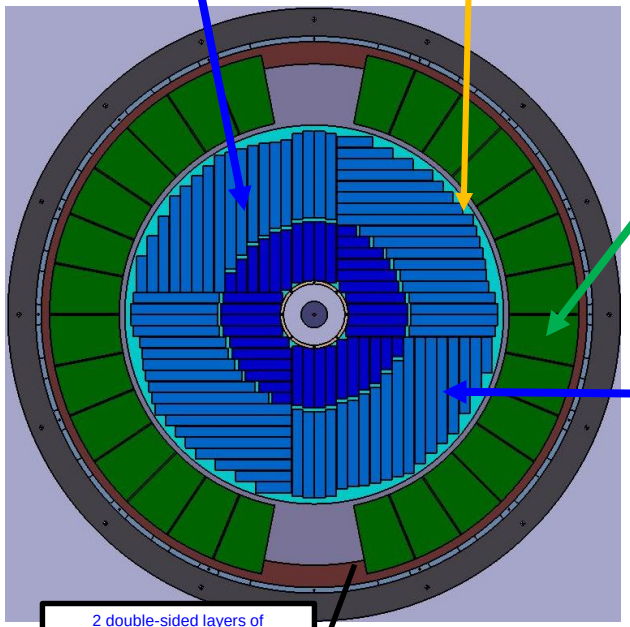


HGTD electronics: General architecture

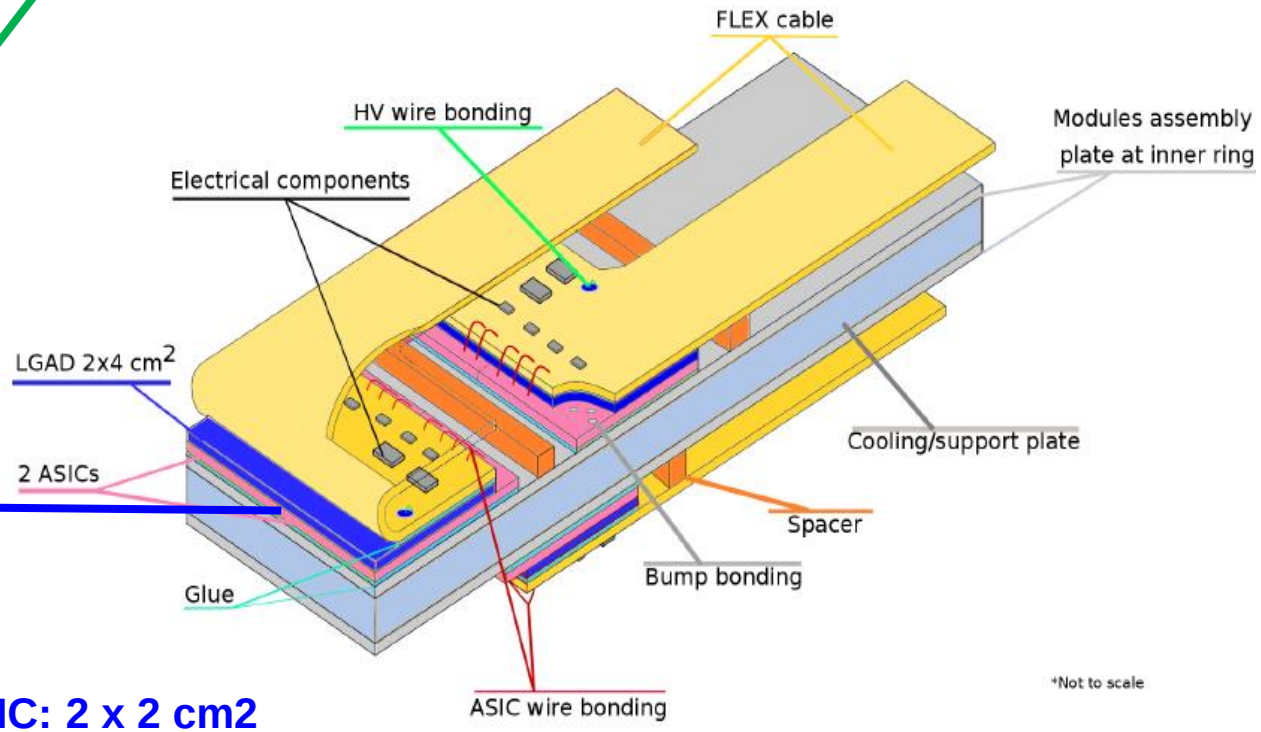
FE ASIC (ALTIROC): to readout LGAD sensors. Provides a time measurement of each hit of events selected by L0/L1 trigger with a resolution smaller than 30 ps/MIP



On detector electronics



z



Final ASIC: 2 x 2 cm2
225 channels to readout 225 pixels of 1.3 x 1.3 mm2

- 2 disks/EC, 2 double sided Layers of LGAD sensors & ASIC /disk, Rin/Rout = 120/640 mm
- 3 952 modules of 2 x 4 cm2 /End Cap => total of 15 810 ASIC (23 000 with yield)

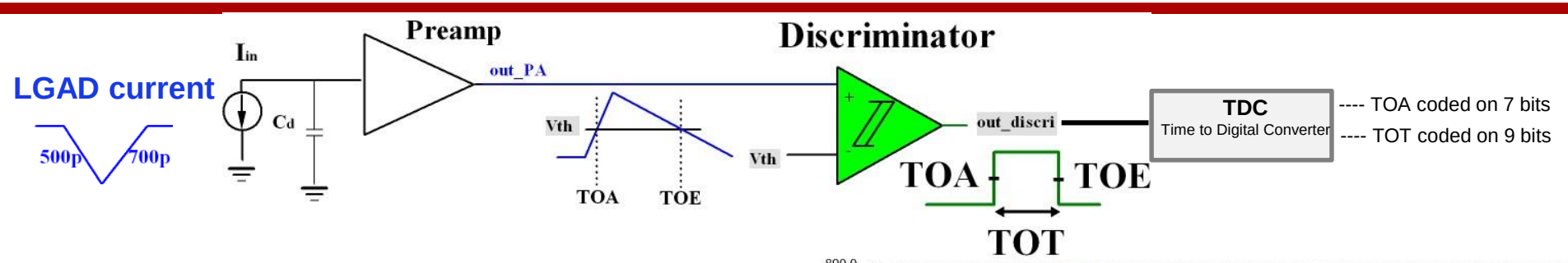
ASIC requirements

LGAD pixel size (thickness ~ 45 µm)	**1.3 x 1.3 mm^2**
Detector capacitance	**3.4 pF**
Collected charge (1 MIP) at gain = 20	**9.2 fC**
Dynamic range	20 MIPs
Preamplifier-discri jitter at gain = 20	**< 20 ps**
Time walk contribution	**< 10 ps**
TDC binning	20 ps (TOA) and 40 (or 80) ps (TOT)
TDC range	2.5 ns (TOA) and 20 ns (TOT)
Number of bits / hit	7 for TOA and 9 for TOT
FIFO latency	10 µs/ 35 µs latency for L0 (L1) trigger
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)
Number of channels/ASIC	**225**
elink driver bandwidth	320 Mb/s, 640 Mb/s and 1.28 Gb/s
Total power per area (ASIC)	**< 300 mW/cm^2 (< 1.2 W) => 5 mW/ch or 4 mA/pixel**
TID and neutron fluence	Inner region: **4.5 MGy, 4.5 x 10 ^{15} n/cm^2** Outer region: **2.1 MGy, 4.0 x 10 ^{15} n/cm^2**

Electronics ime contribution < 30 ps

=> CMOS 130nm

Electronics time resolution: Time Walk, Jitter, TDC bin



$$\sigma_t^{TDC} = \frac{TDC_{bin}}{\sqrt{12}}$$

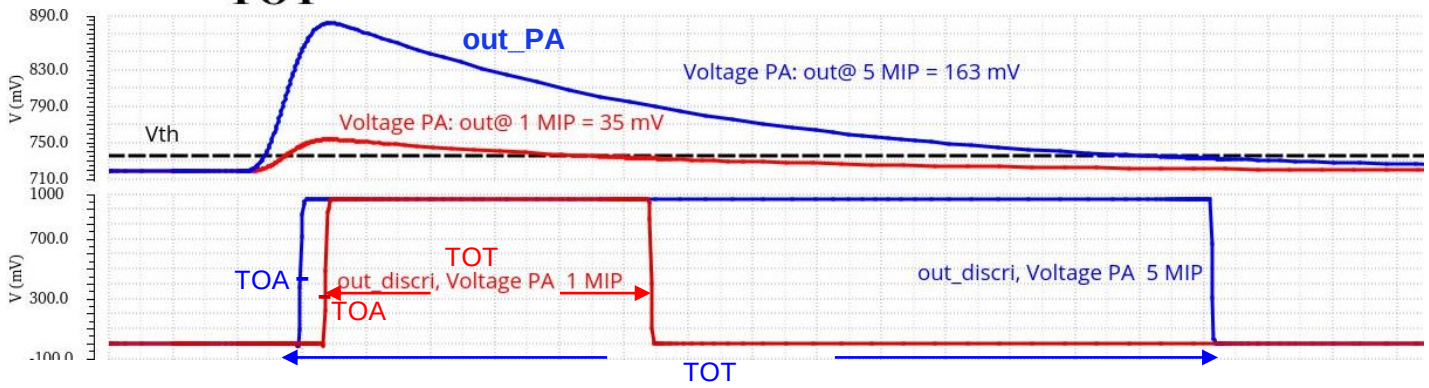
Time Walk

Due to physics signal duration and preamp speed

Time walk: the voltage value Vo is reached at different time for signal of different amplitudes

$$\sigma_t^{TW} = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$

Can be corrected offline

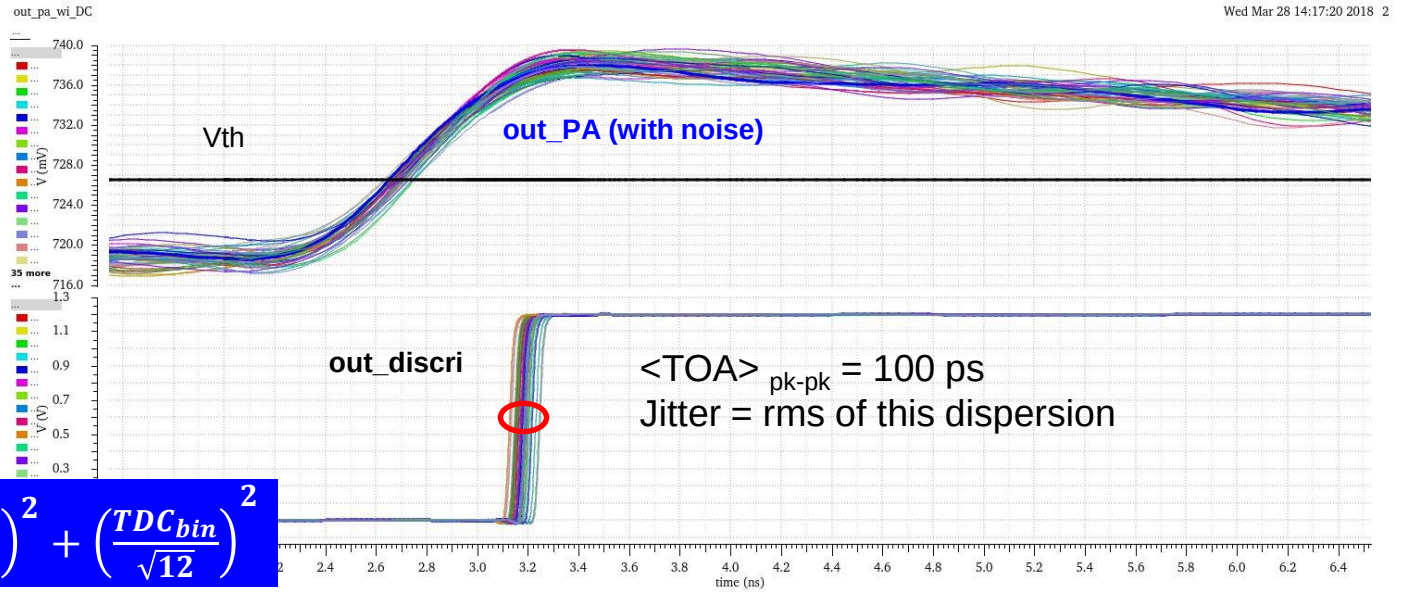


Jitter

Mostly due to electronic noise

Jitter: the noise is summed to the signal, causing amplitude variations

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}} = \frac{t_{rise}}{S/N}$$

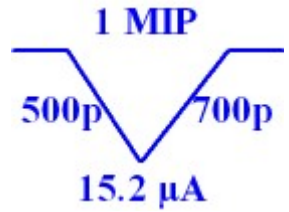


Total Time resolution : $\sigma_t^2 = \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$

Jitter

- Jitter calculation (Voltage preamp):

$$\sigma_t^J = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$



LGAD signal (G=20)

- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

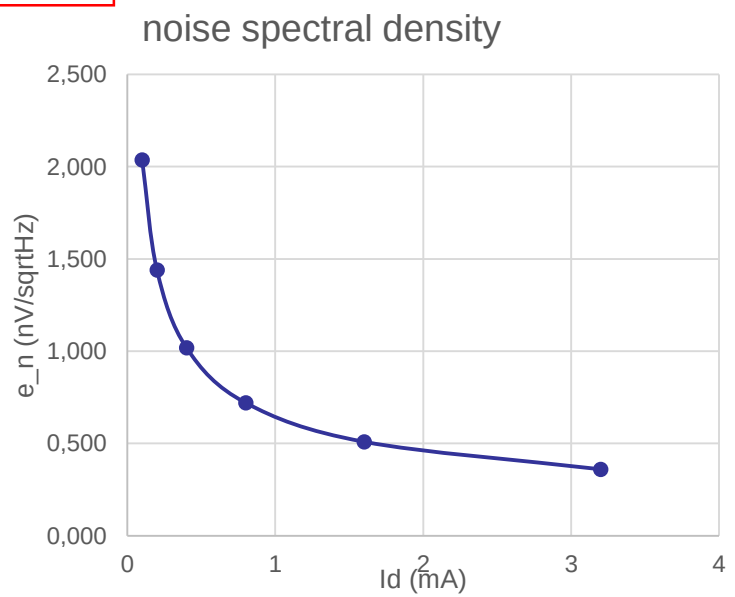
Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d= drift time of the detector
e_n preamp noise density

Dominated by sensor
Electronics only gives the spectral density of the input transistor e_n

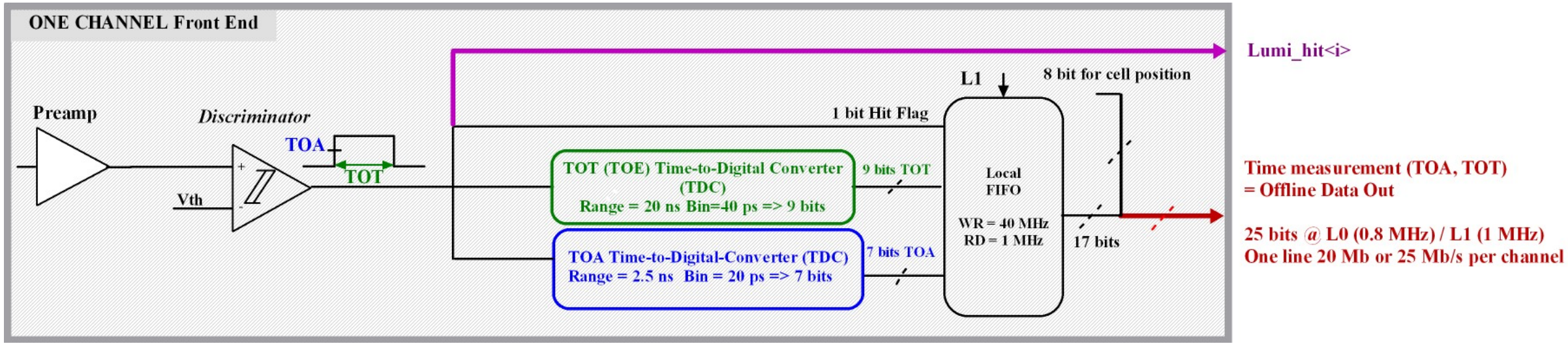
- Gives ps/fC as scales with 1/Qin

- Electronics noise e_n given by the input transistor transconductance g_m

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$



ALTIROC: Front-End Channel/pixel

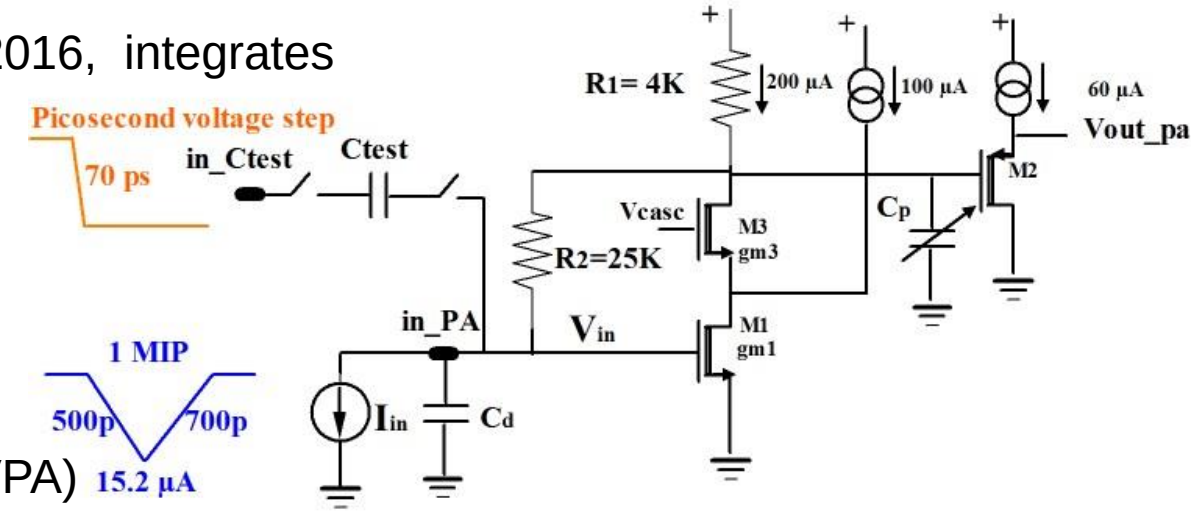


Each FE channel made of

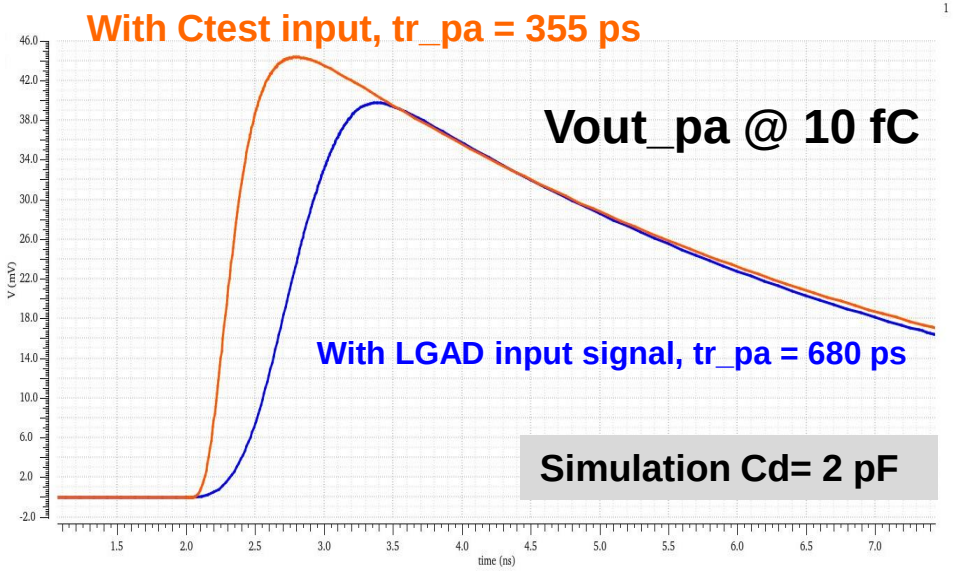
- A preamplifier followed by a discriminator: Time walk correction made with a Time over Threshold (TOT) architecture
- Two TDC (Time to Digital Converter): Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
  - ✓ TOA: range of 2.5 ns and a bin of 20 ps (7 bits)
  - ✓ TOT: range of 20 ns and a bin of 40 ps (9 bits)
- One Local memory (FIFO): to store the 17 bits of the time measurement until L0/L1 trigger (~ 1 MHz)
- Data transmitted/pixel: 17 bits + 8 bits for channel number = 25 bits @0.8MHz or 1MHz + discri output for the luminosity measurement

ALTIROC0

- First prototype designed in CMOS130 nm submitted in Dec 2016, integrates only the analog part
- 8 channels:
  - 4 channels for 1x1 mm2 sensors (2pF)
  - *4 channels for 3x3 mm2 sensors (20 pF): NOT USED*



- 2 pF Preamp: Common source configuration (Voltage PA = VPA)
  - Power < 500 µW: Id (M1) = 300 µA, I (M2)= 60 µA
  - Low input capacitance: ~ 300 fF, Low noise: 1.2 nV/√Hz
  - BW tuneable with Cp: 1 GHz down to 200 MHz
  - R2=25K: for DC bias, Rin ~ 1.6 KΩ, Fall time= 2.2 RinCd
  - I leakage sensor: absorbed by R2
  - Can be disabled by Slow Control



PA BW tuned with Cp, tr_pa (δ) = td/2

POST LAYOUT SIMULATIONS (LGAD)	C_d = 2 pF	C_d = 4 pF	C_d = 10 pF
Preamplifier Bandwidth (MHz)	550	560	500
Noise (mV)	0.54	0.57	0.57
S/N	93	54	30
Jitter (ps) 1 MIP=10fC (LGAD G=20)	10	16	32

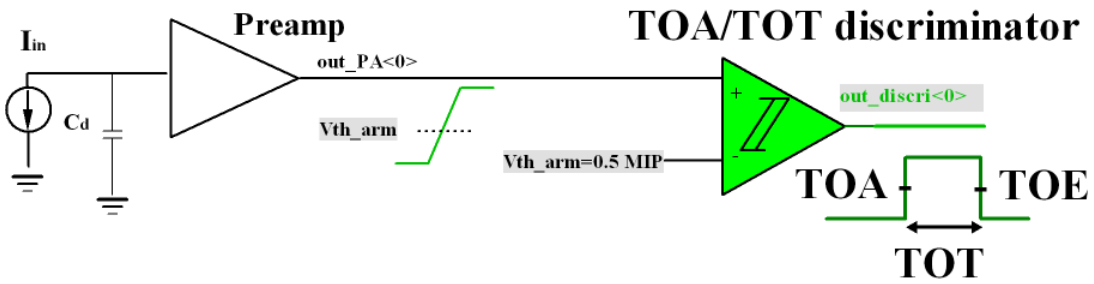
$$\sigma_t^J = \frac{C_d}{Q_{in}}\sqrt{\frac{2kT}{g_m}t_d}$$

ALTIROC0 measurements

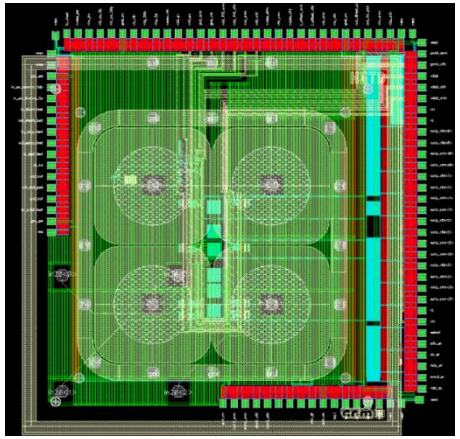
- Submitted mid **December 2016, received in March 2017**

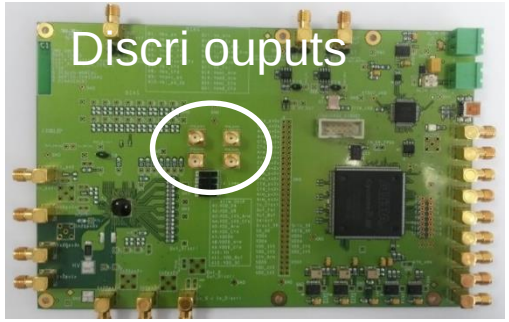
- **Area = 3.4 x 3.4 mm2**, thickness=300µm: **large chip** to fit 1 x 1 mm2 sensors (for testbeam)

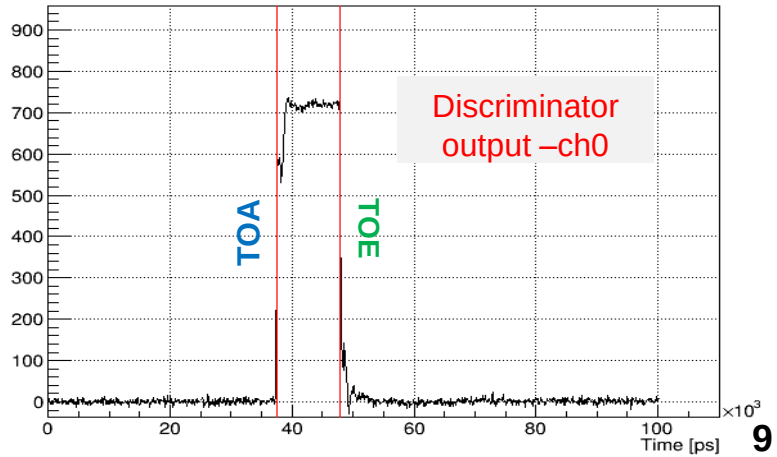
- **8 channels**: Four 2pF-channels and four 20 pF-channels
  - Characterization of 2 pF-channels only
  - Characterization of the TOT architecture only. CFD architecture also tested but tunings quite tricky and performance similar to the TOA/TOT architecture
  - Scope measurements, injection through internal Ctest



- **Identical test boards** for testbench and test beam measurements:
  - Testbench: **ASIC alone, wire bonded on the board**
  - Testbeam: **ASIC bump bonded on the sensor** (1 x 1 mm2 sensor, 42 µm thickness => C sensor ~ 2.5 pF)







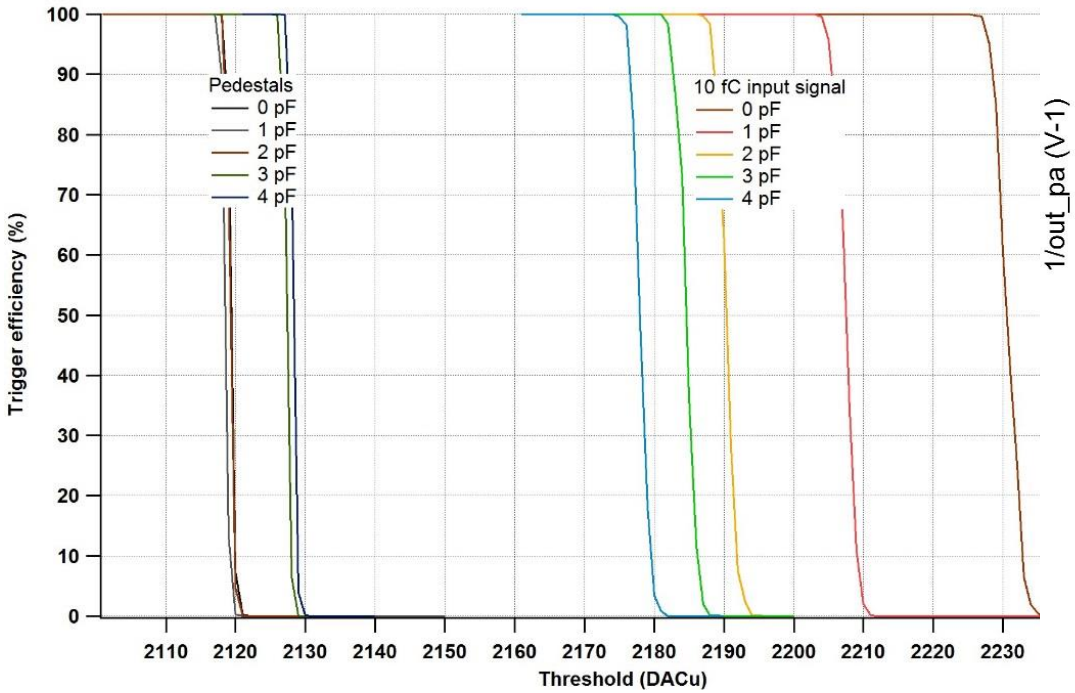
ASIC and testboard parasitic capacitance measurement

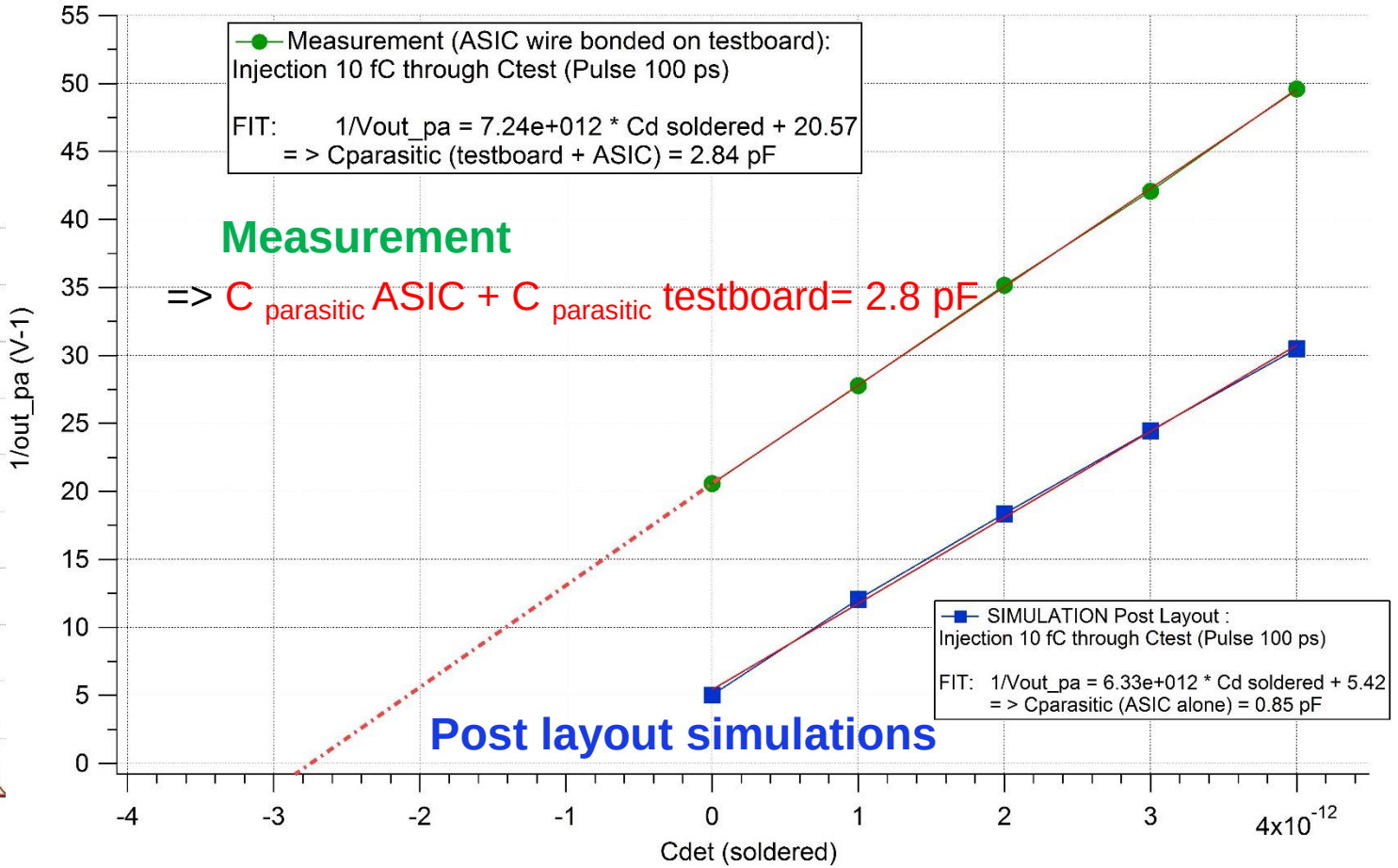
As the jitter is proportional to Cd, it is Important to extract the parasitic capacitance (Testboard, ASIC ..)

Cparasitic extracted from the fit of 1/Vout_pa versus Cdetector:

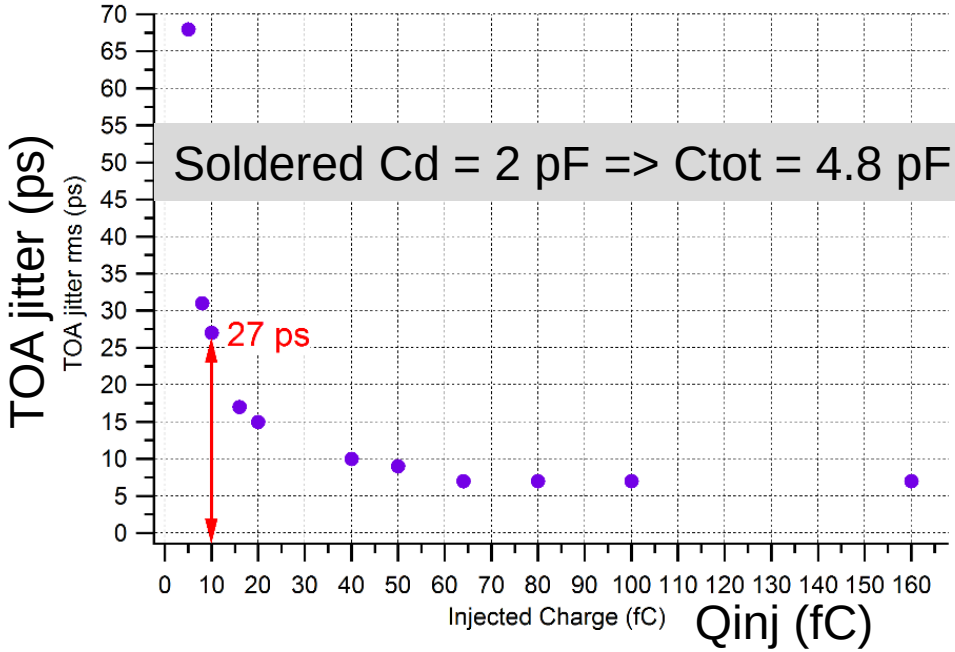
- Vout_pa measured (Scurves) for various Cd (soldered on the testboard) and Qinj=5 fC, 10 fC , 20 fC (Injection of 50 mV, 100 mV or 200 mV through internal Ctest = 100 fF)

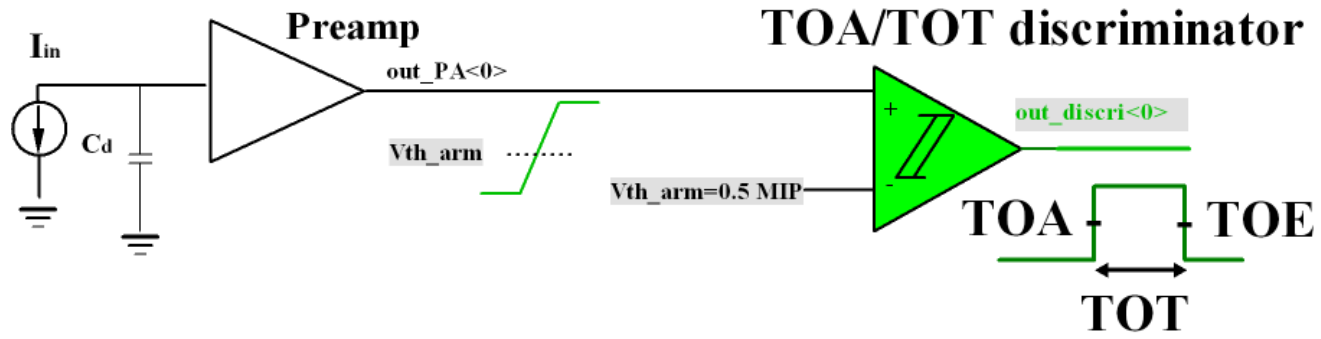
$$\frac{1}{V_{out\_pa}} = \frac{C_d}{G_{pa} * Q_{inj}} + \frac{C_{parasitic}}{G_{pa} * Q_{inj}}$$

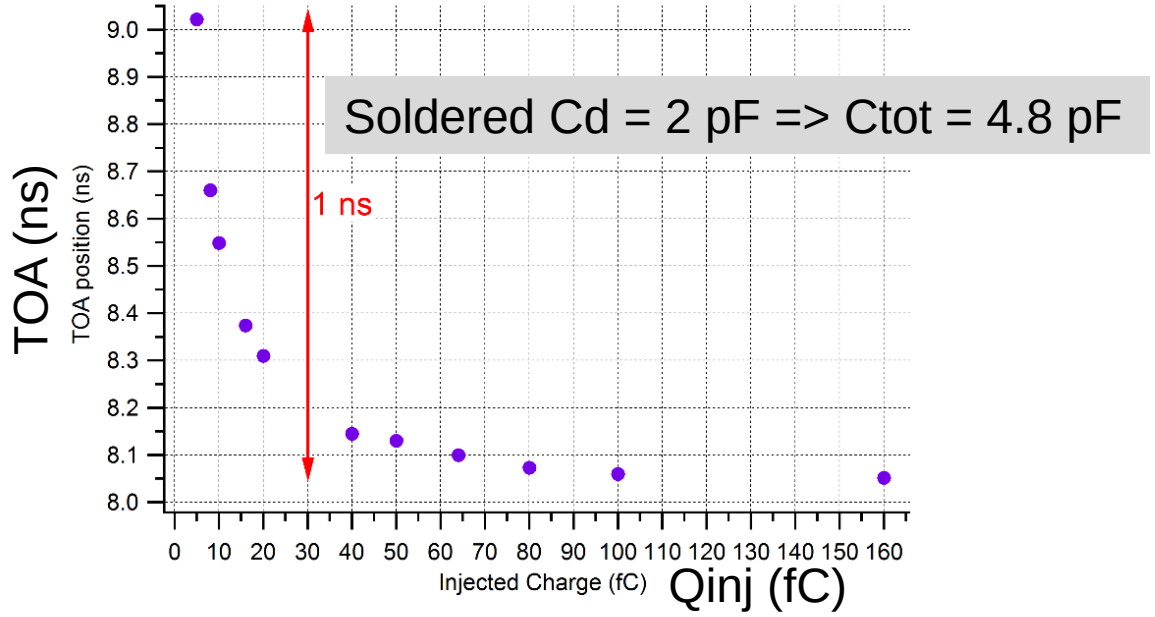




Test bench measurements







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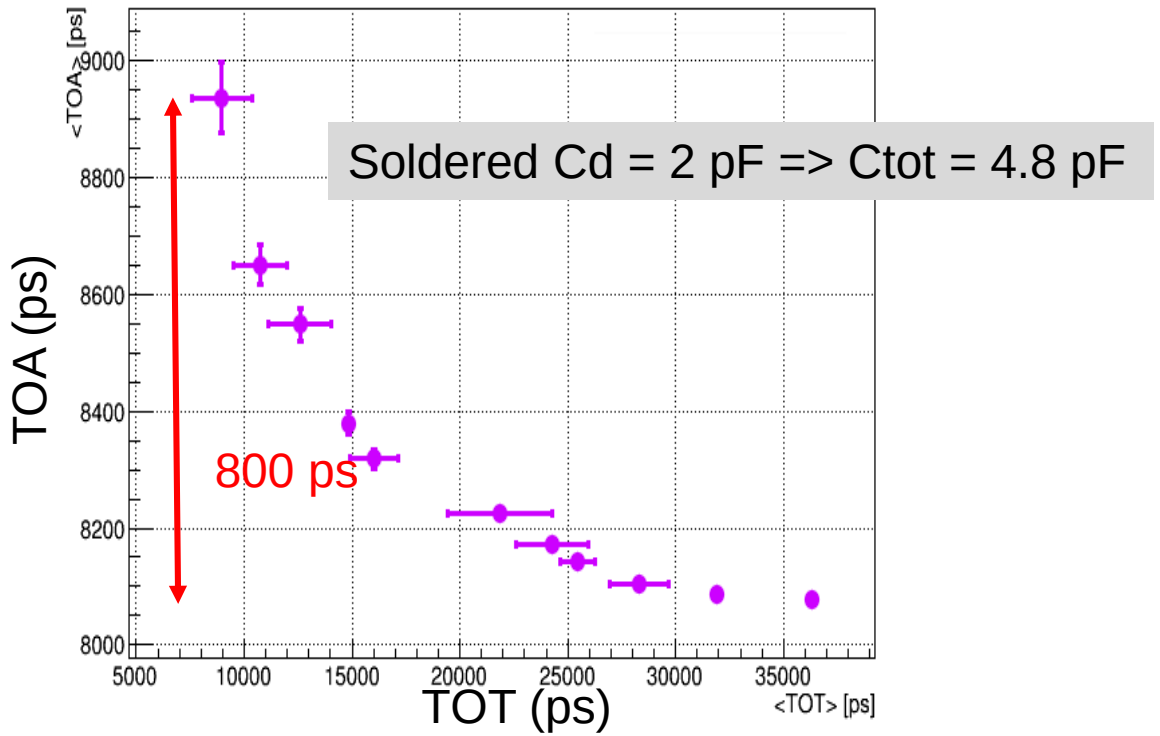
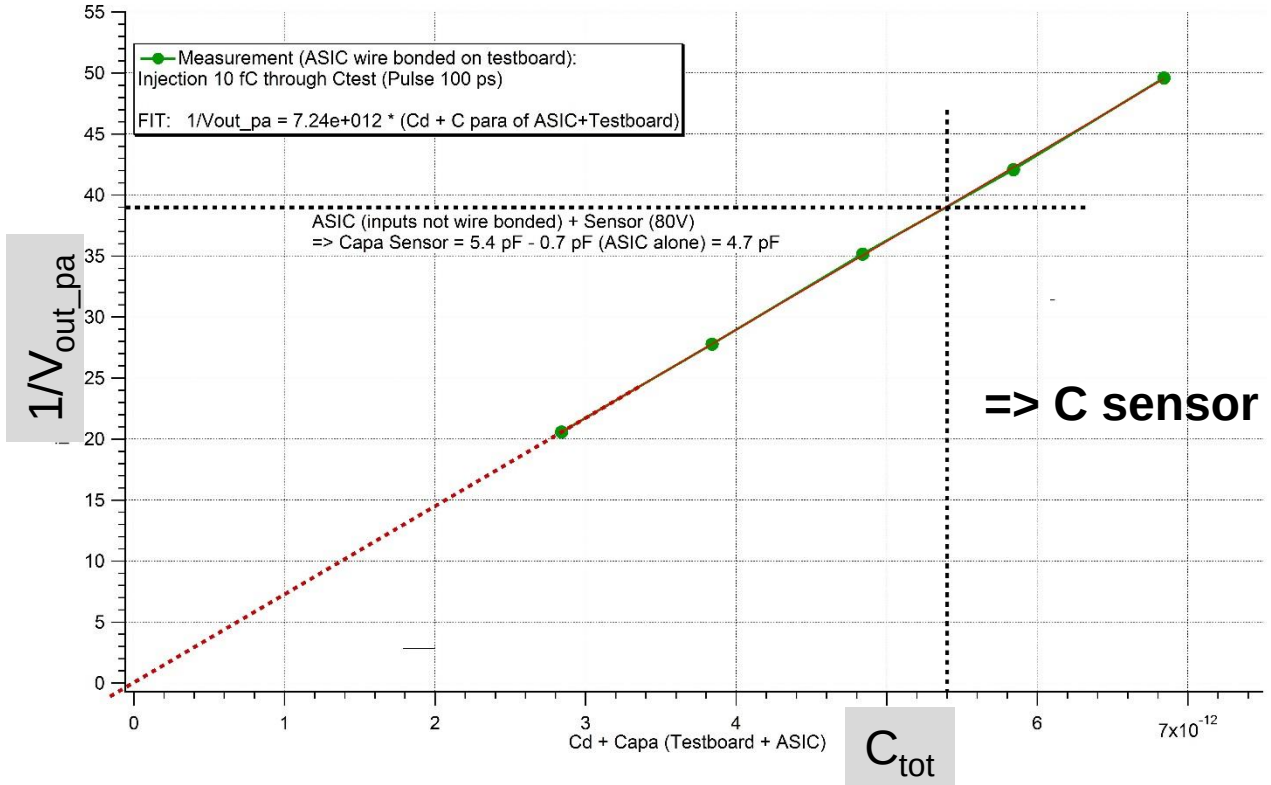
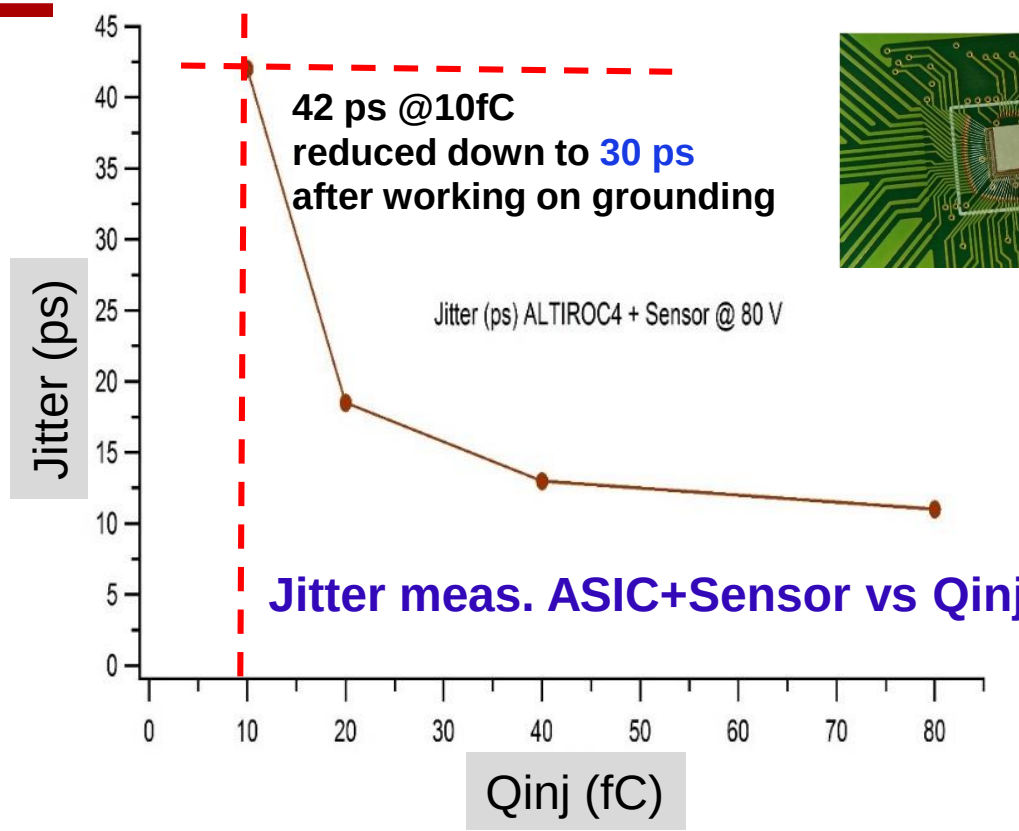


Test bench measurements with ASIC + sensor

- 1x1 mm² sensors fabricated by CNM/IFAE Barcelona, expected C sensor ~ 2.5 pF
- Bump-bonded to ALTIROC0 at Barcelona
- Sensor biased at - 80 V
- **Test pulse injection through internal Ctest=0.1 pF**

- After reworking on the grouding, ASIC+Sensor jitter measurement gives = 30 ps @ 10 fC and ~ 25 mV (for HV= 80 or 130V)





Jitter meas. ASIC+Sensor vs Qinj

=> C sensor = 5.4 pF – 0.7 pF = 4.7 pF

Testbeam with ASIC + sensor (Sept 2017)

- 1x1 mm² sensors fabricated by CNM/IFAE Barcelona
- Bump-bonded to ALTIROC0 at Barcelona
- Sensor biased at - 80 V
- **Testbeam** measurement **ASIC+Sensor (LGAD signal)**= **48 ps**

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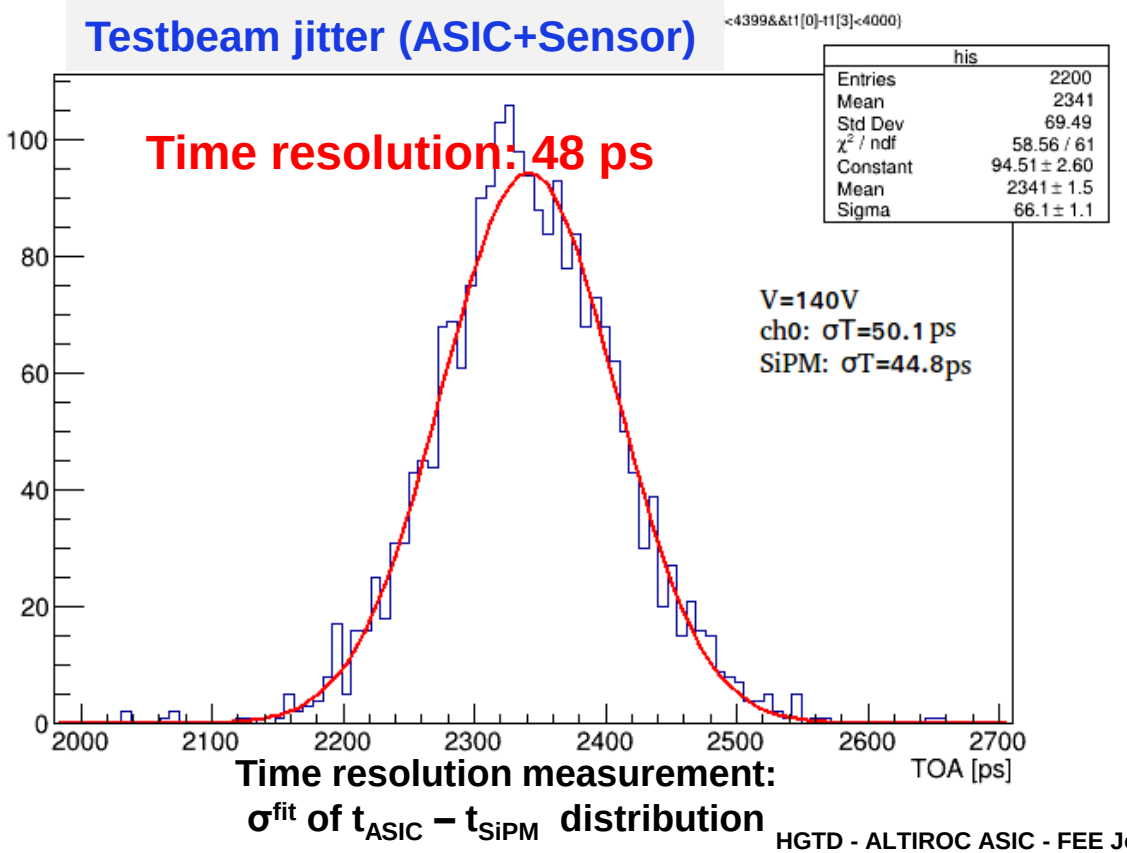
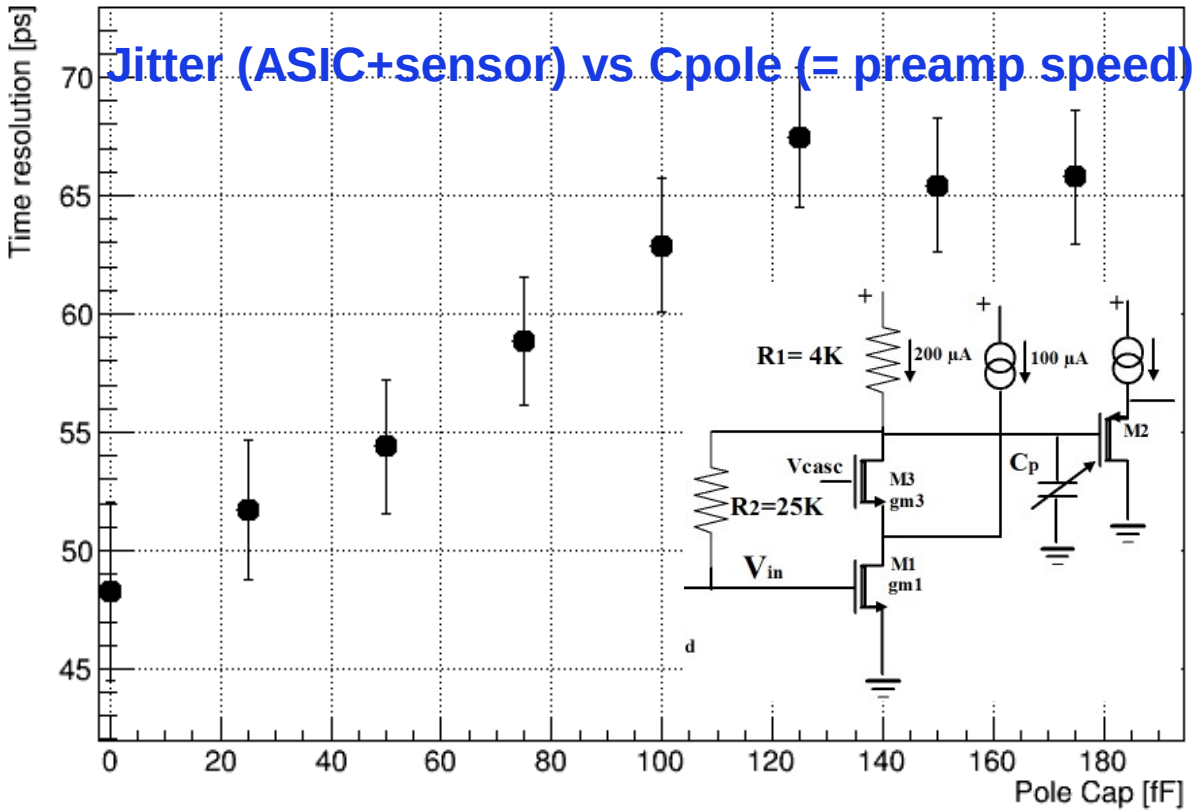
Testbeam jitter (ASIC+Sensor)



Time resolution measurement:
σ^{fit} of $t_{ASIC} - t_{SiPM}$ distribution

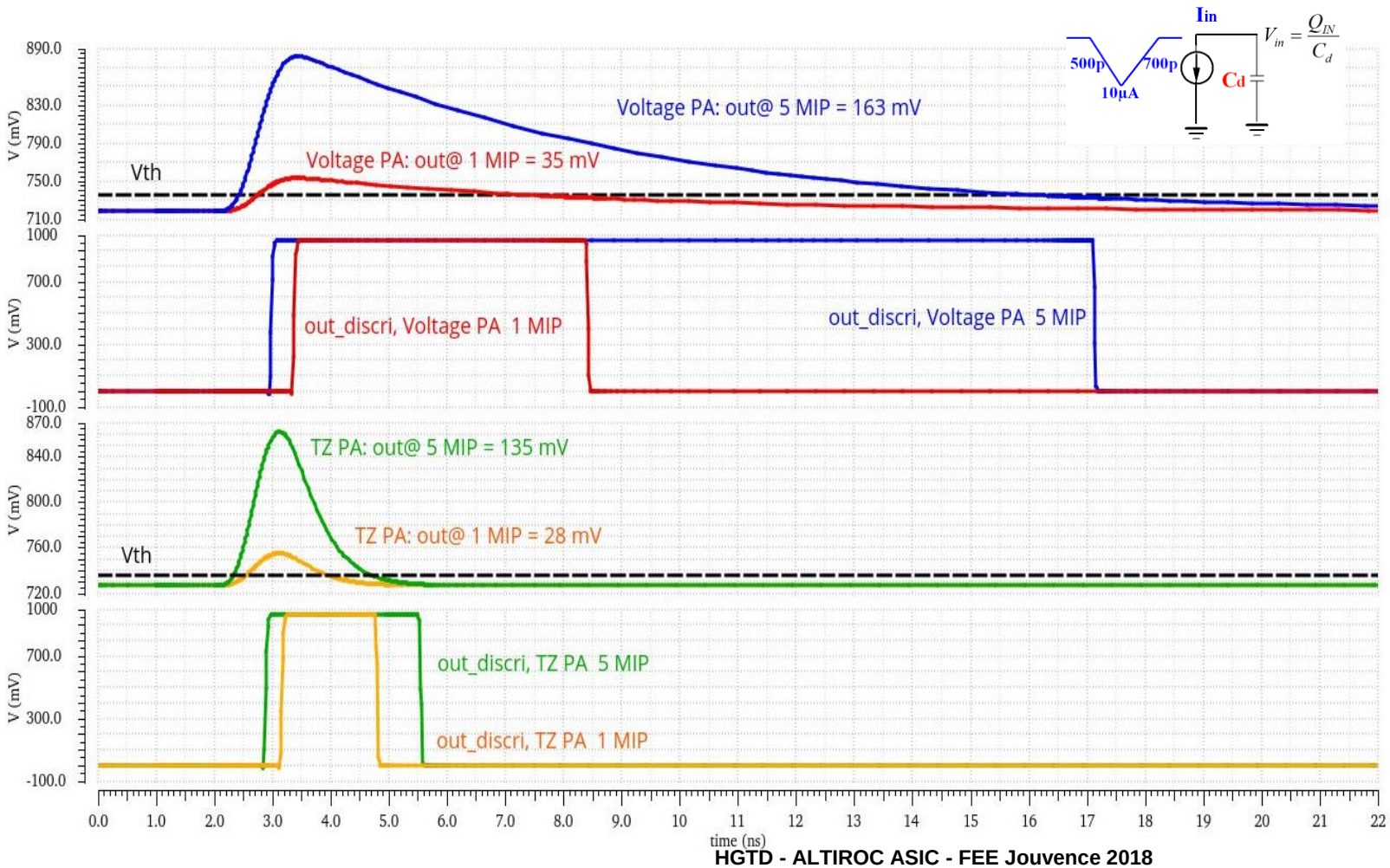


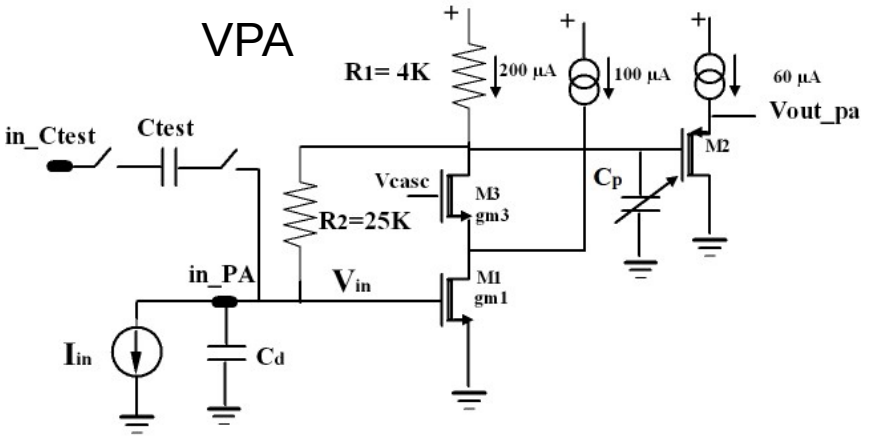
ALTIROC best input preamp: Voltage PA or TZ PA?

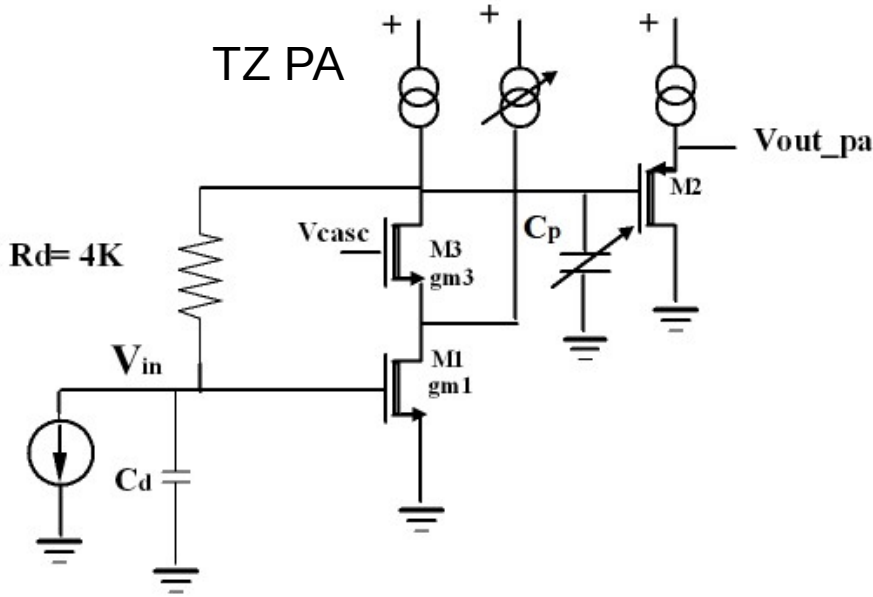
- Jitter: calculation gives the same result for VPA and TZ

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

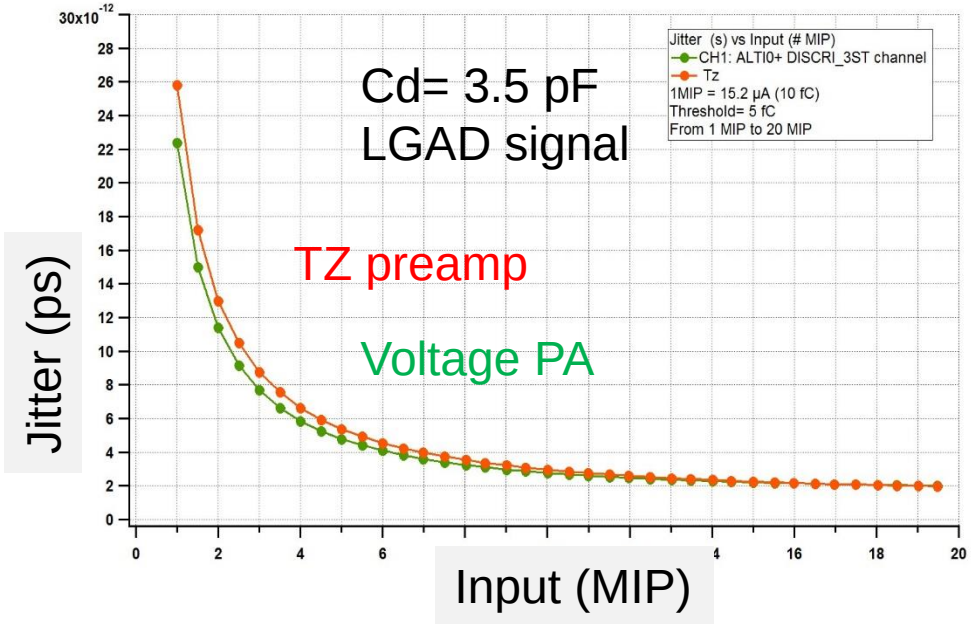
- Fall time given by 2.2* Rin_pa * Cd
Rin_TZ pa =150 Ω whereas Rin_Voltage PA ~ 1.5 KΩ
=> **TOT_TZ (few ns) very different from TOT_VPA**

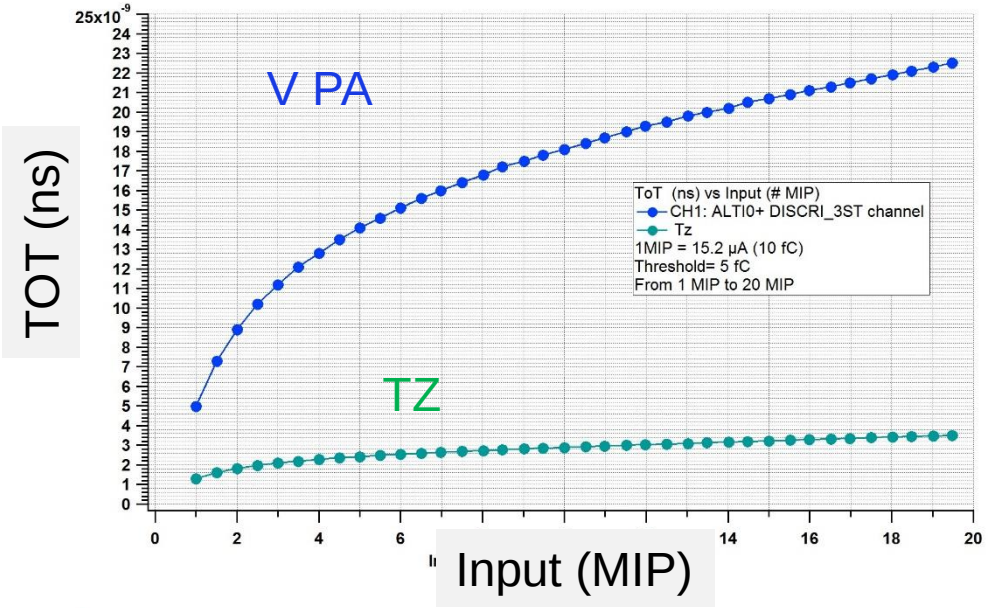




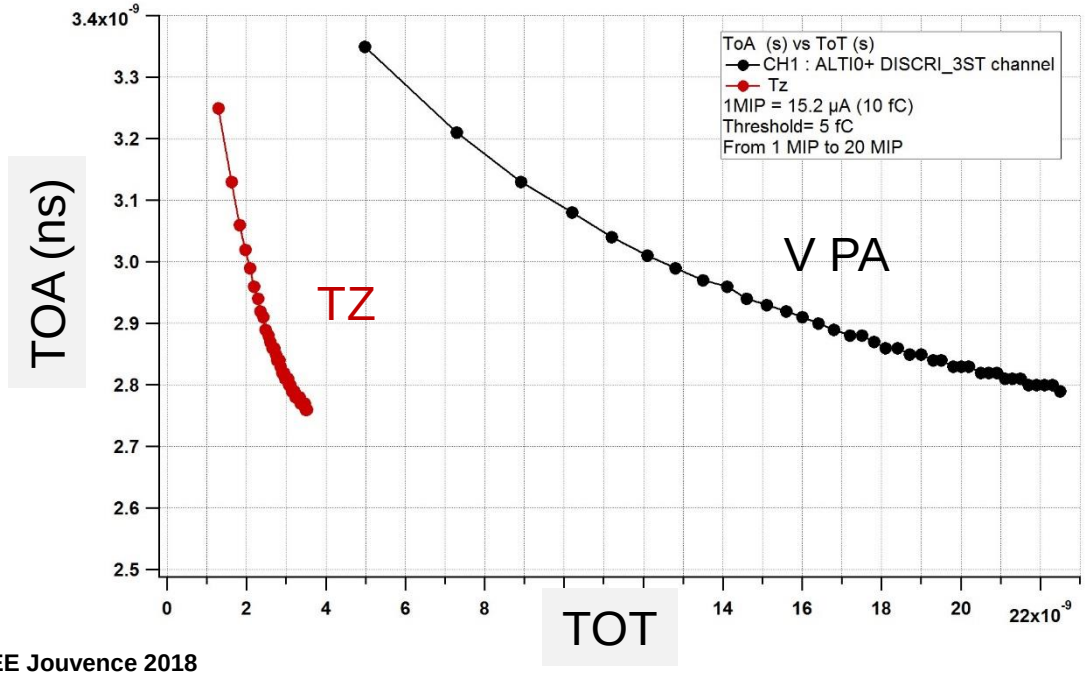


VPA, TZ PA and discriminator simulations





Jitter similar for TZ and VPA architectures but
TOA vs TOT sensitivity very different between these 2 architectures
=> TDC for TOT meas. different for VPA and TZ_PA

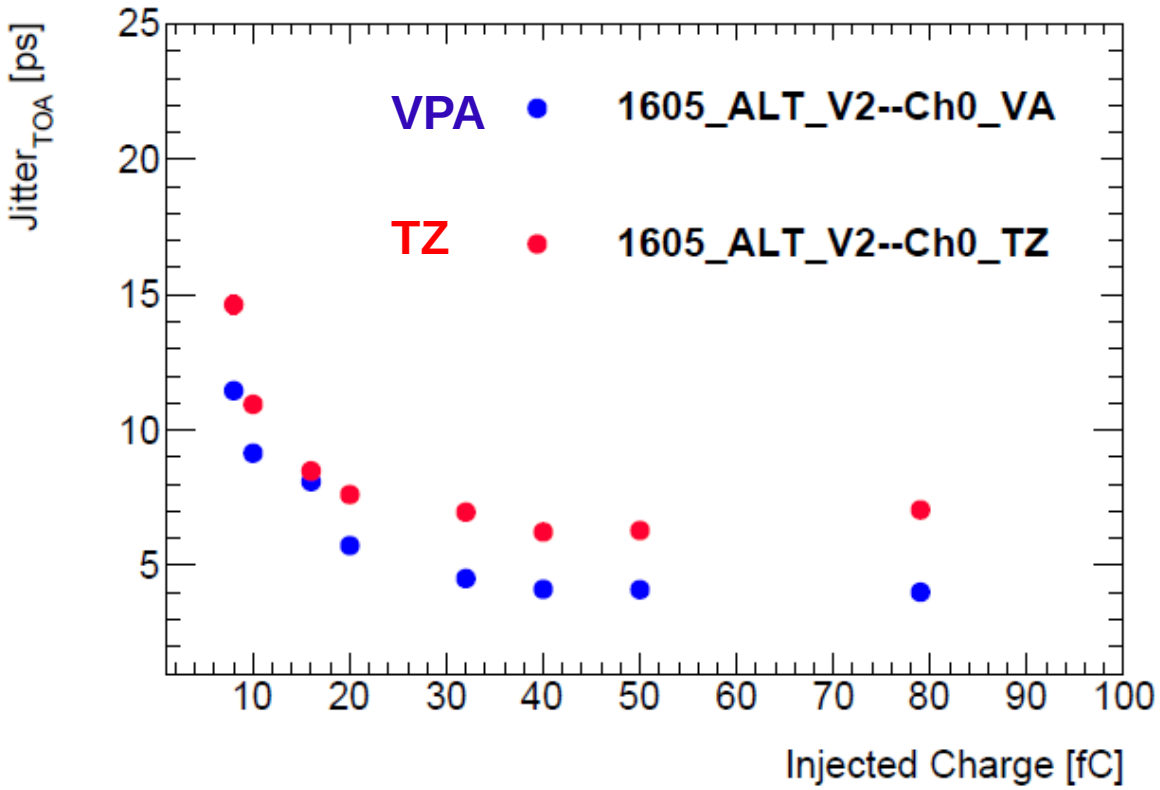


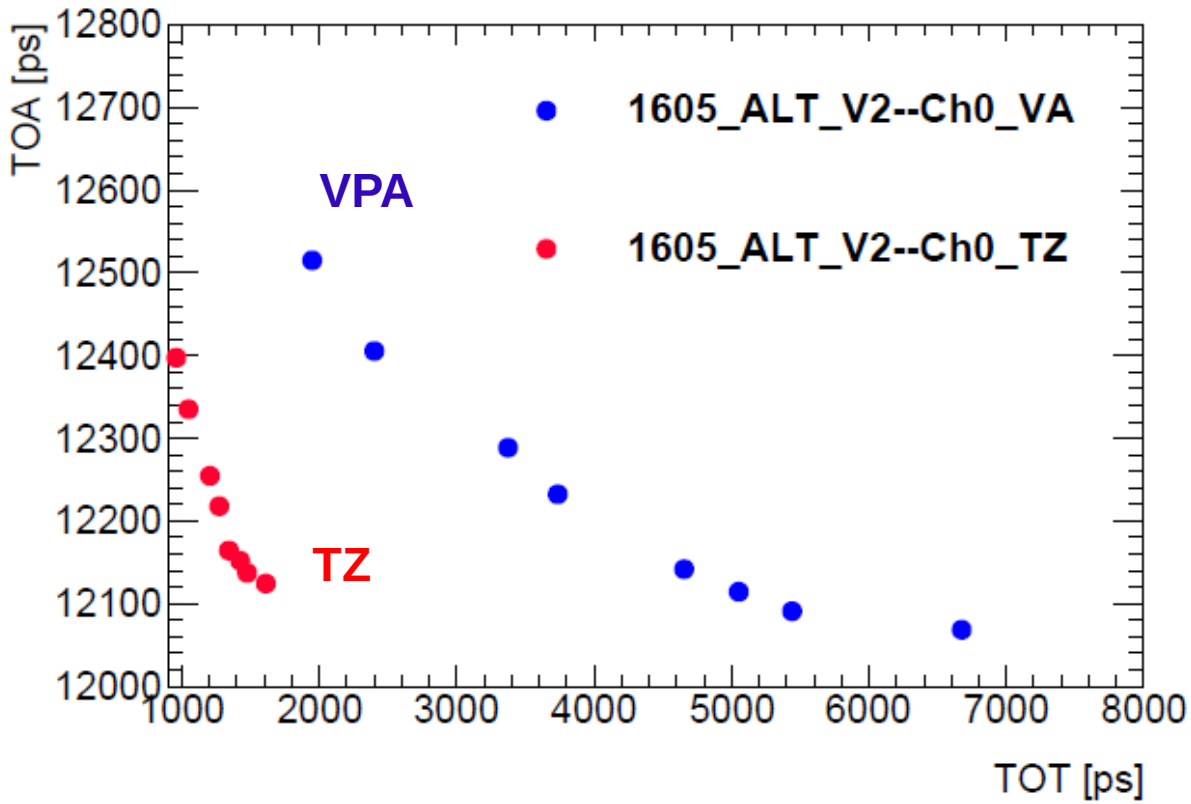
VPA
- Resolution: 40 ps
- Range: 18 ns
- 9 bits

TZ
- Resolution: 20 ps
- Range: 3 ns
- 8 bits

ALTIROC0_V2 measurements

- ALTIROC0_V2 (Submission December 2017) : same as ALTIROC0_V1 but faster VPA and the four 20pF- channels replaced by 4 TZ preamps



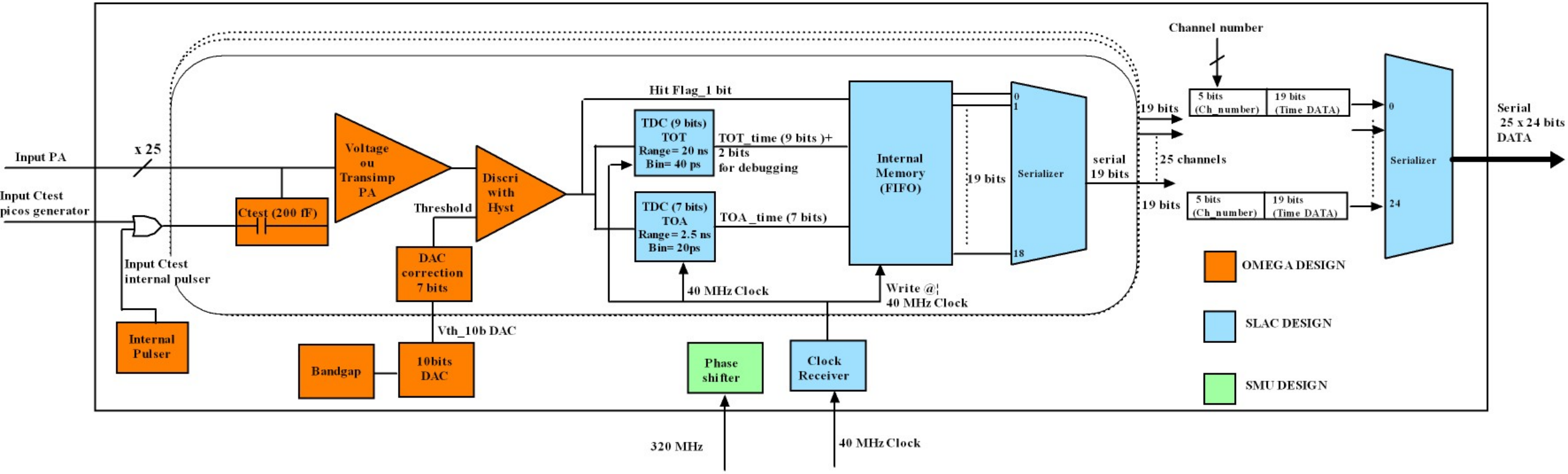


ALTIROC1 prototype (Mid June 2018 submission)

ALTIROC1 = Second ALTIROC ASIC prototype with 25 complete FE channels to readout 5 x 5 sensor cells of 1.3 mm x 1.3 mm (6.5 mm x 6.5 mm) + Phase shifter

3 Labs involved: **OMEGA (analog Part), SLAC (Digital part: TDC and FIFO), SMU (Phase shifter)**

ASIC size: 7,5 x 7 mm² taking into account the pads on the right side of the ASIC (7.5 mm) and also pads (for bias, probes ...) on the top side for debug (top pads only for this prototype version)



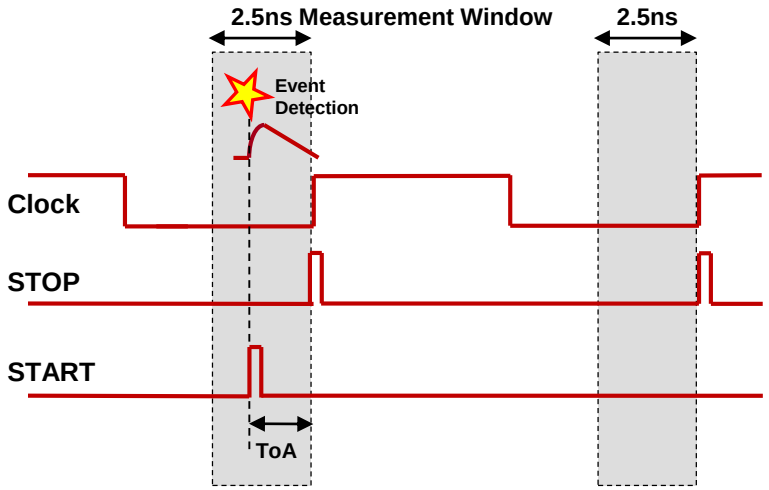
TOA TDC Architecture (Simplified): Vernier Delay Line

@ Bojan Markovic, SLAC

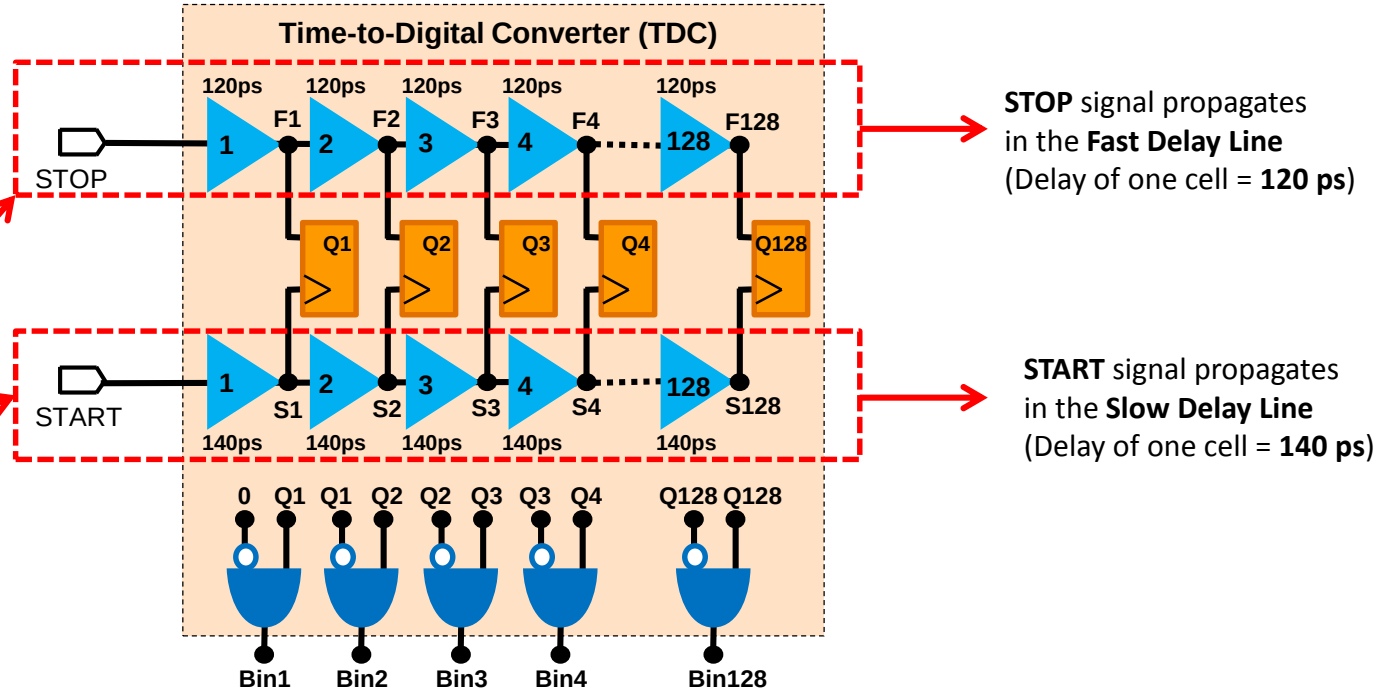
SLAC

TOA (VPA or TZ)

- **Resolution: 20 ps**
- **Range: 2.5 ns**
- **7 bits**



Simplified Block Diagram:



Differential shunt capacitor voltage-controlled delay cells

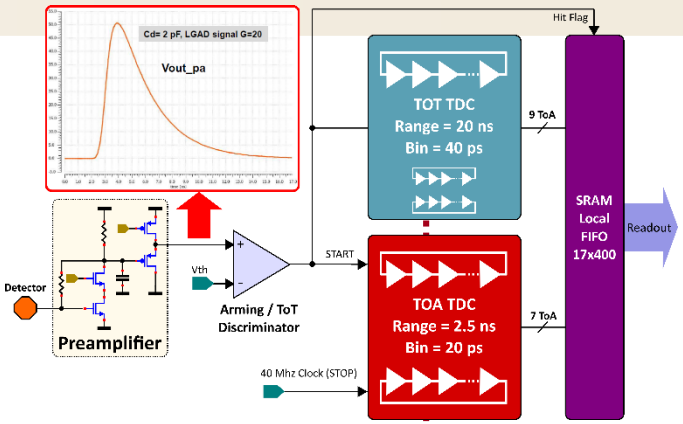
- The **START** pulse comes first and initializes the TDC operation.
- The **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized.
- At each tap of the Delay Line the **STOP** signal catches up to the **START** signal by the deference of the propagation delays of cells in Slow and Fast branches of the delay line: i.e. **140ps – 120ps = 20ps** that represents the **LSB** of time measurement.
- The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion.
- TDC range is equal to **128*20ps = 2.56ns**

TDC for TOT measurement

@ Bojan Markovic, SLAC

TOA (VPA or TZ)

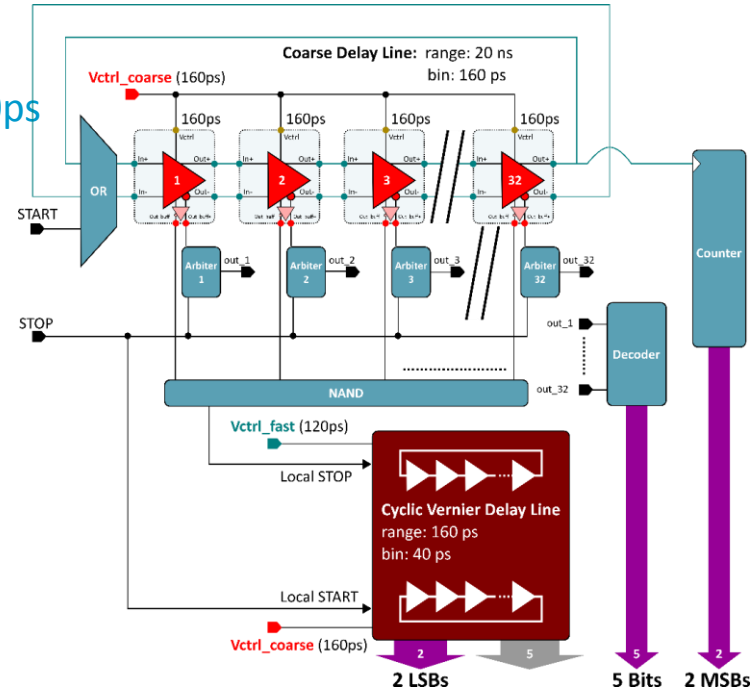
- Resolution: 20ps
- Range: 2.5 ns
- 7 bits



TOT: coarse delay line + TOA TDC

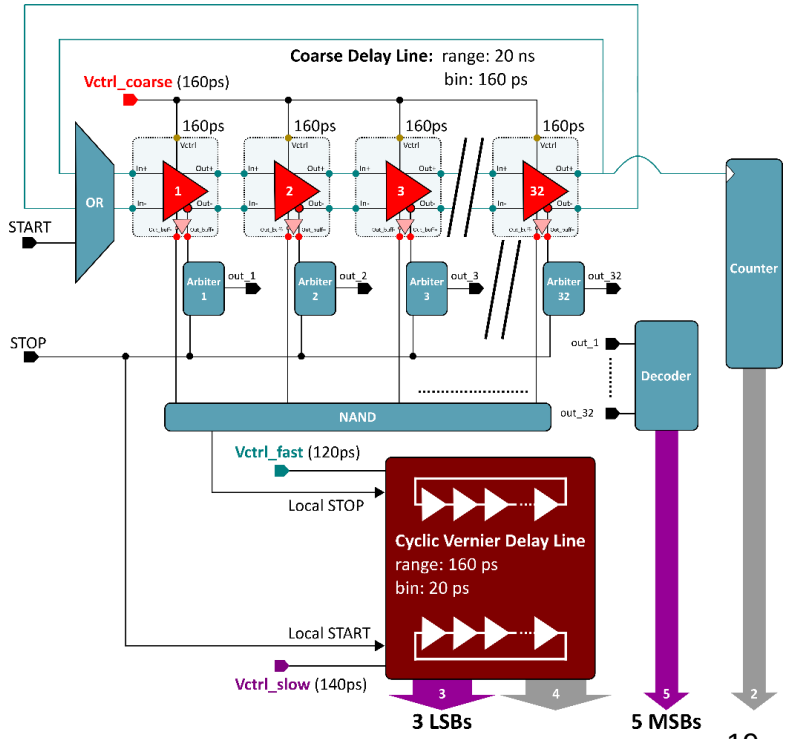
TOT VPA

- Resolution: 40ps
- Range: 18ns
- 9 bits



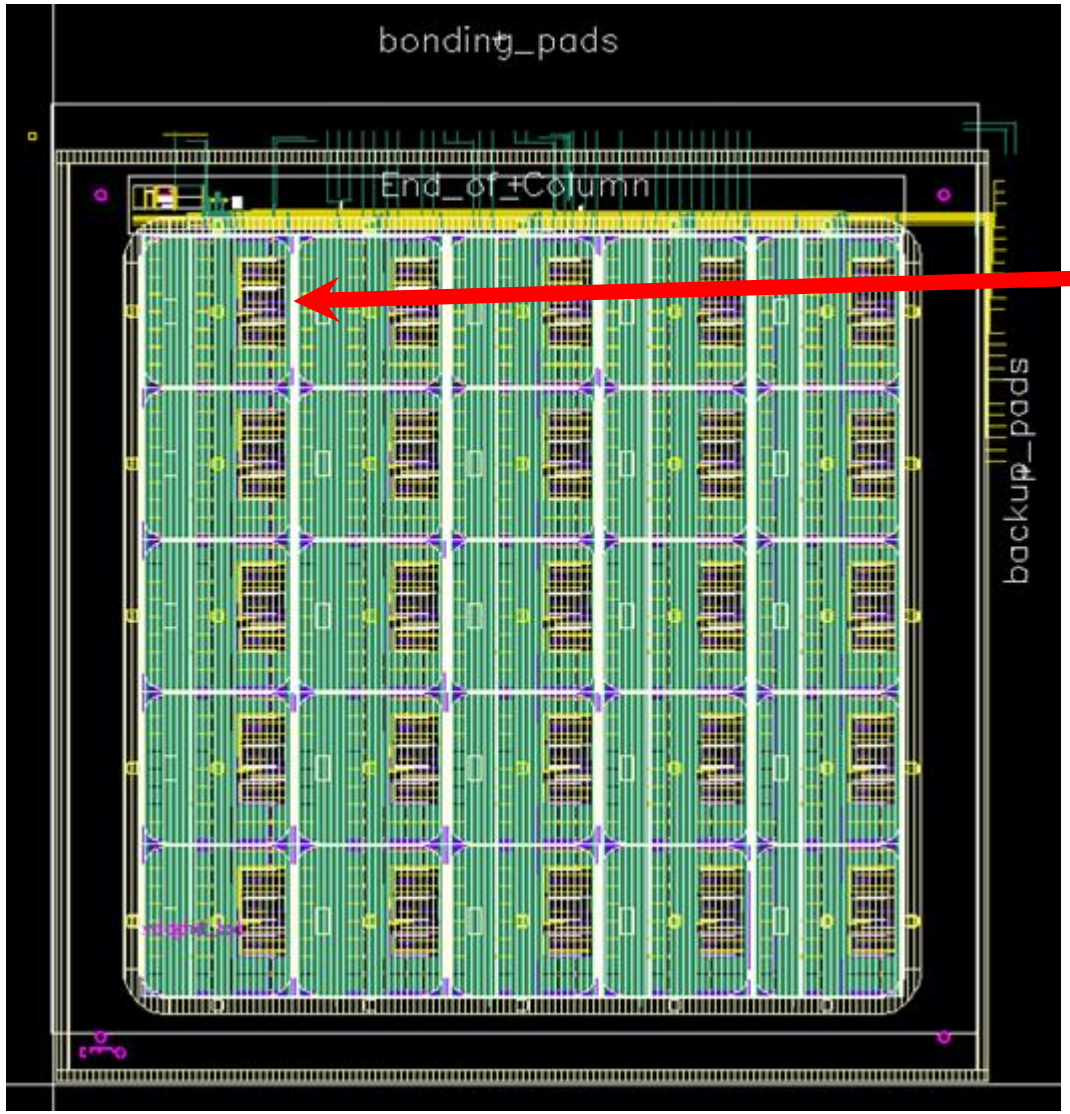
TOT TZ

- Resolution: 20ps
- Range: 3ns
- 8 bits

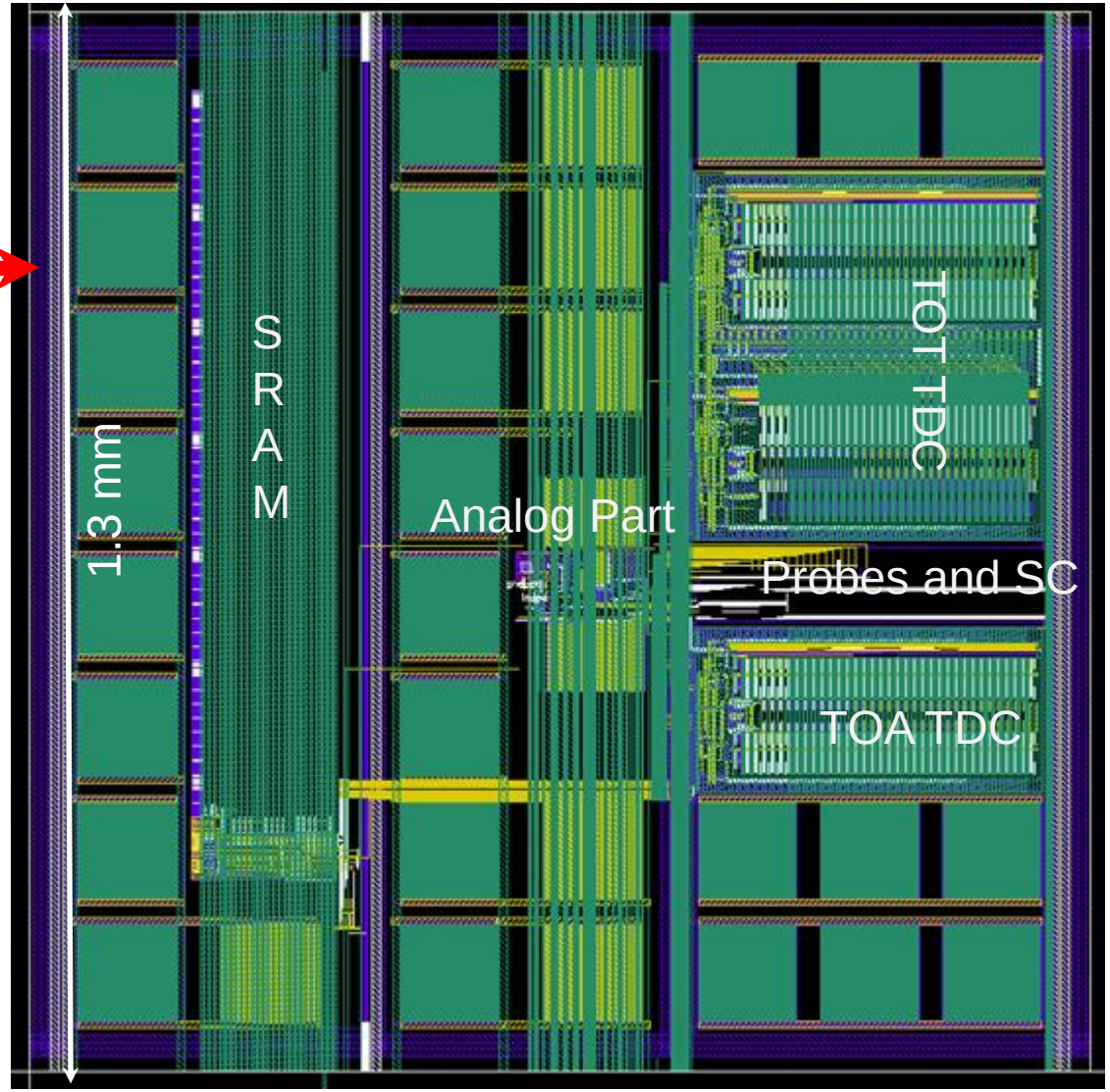


Altiroc1 layout ~ 7 mm

~ 8 mm



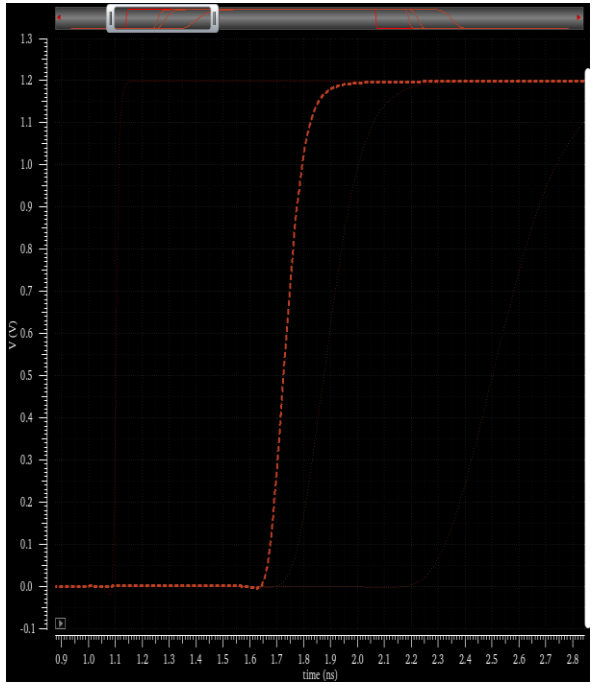
One pixel layout 1.3 mm

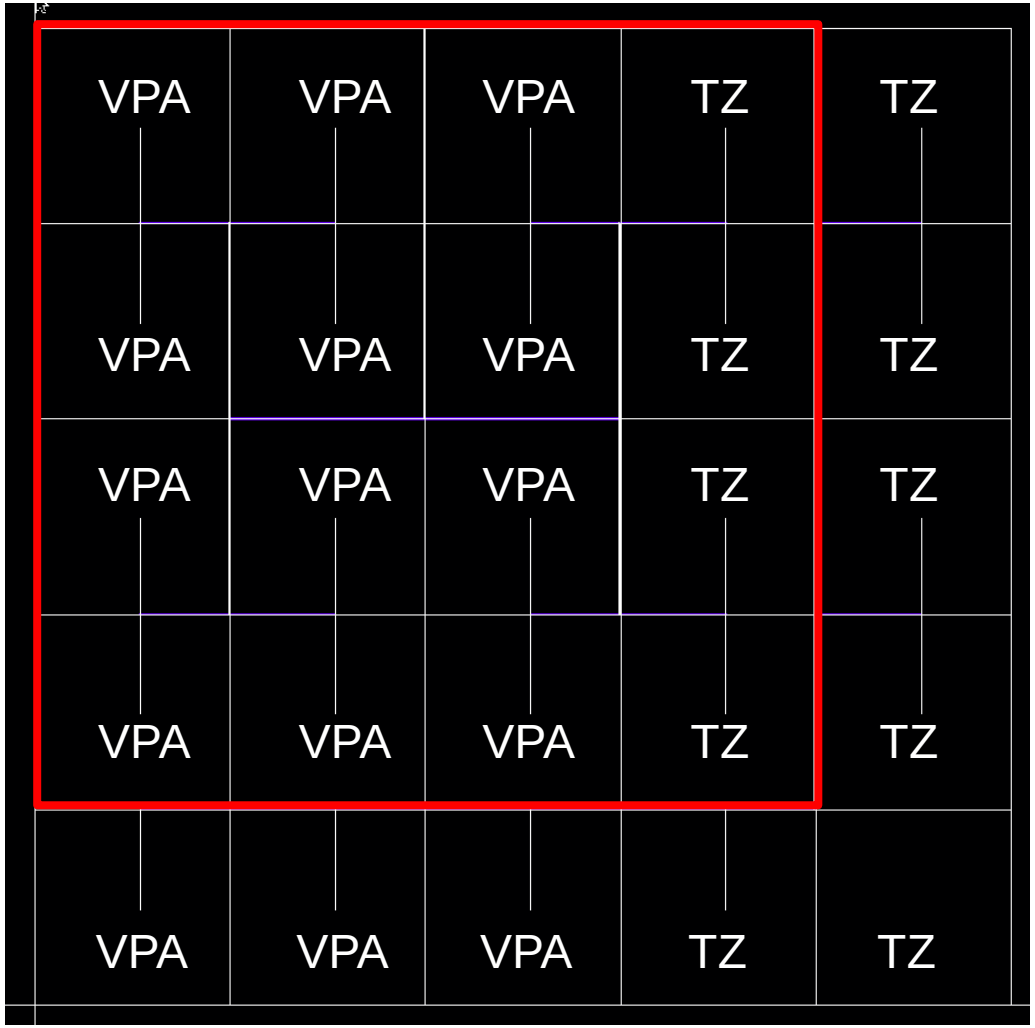


Clock tree

- Clock tree (pulser command , clocks): 4x4 channels
- Delay : 700 ps
- $tr_{10\text{-}90}$ = 130 ps

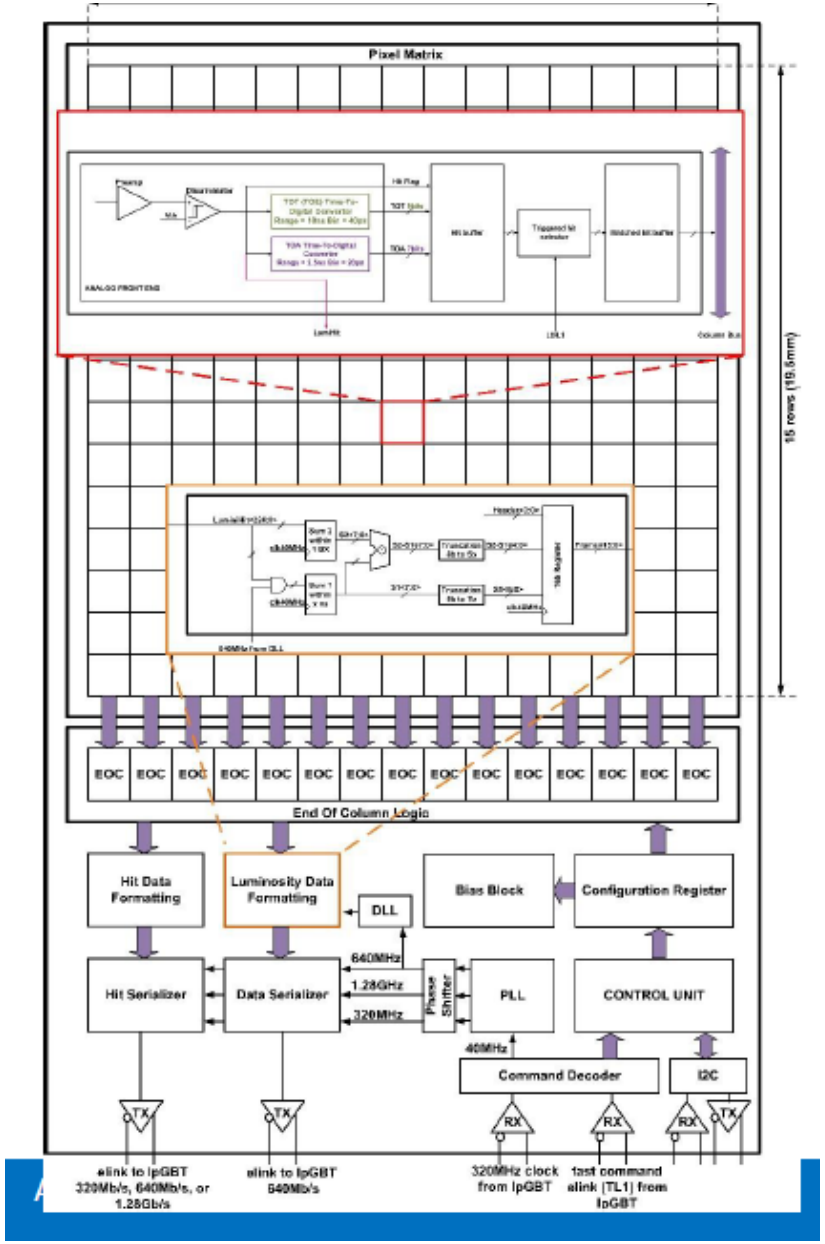
VPA: Voltage preamp
TZ: Transimpedance preamp





SUMMARY

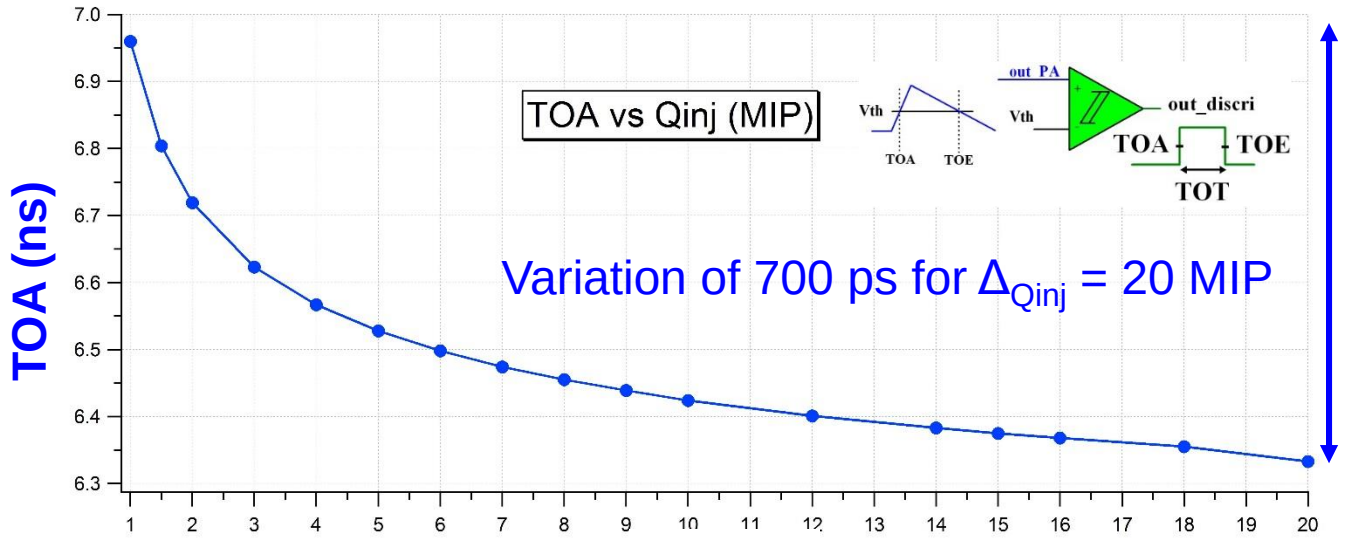
- Performance quite good on testbench but discrepancy between measurements and simulations to be understood
  - ~ 25 ps jitter obtained on test bench at Q = 10 fC with test pulse and Ctot = 2 pF + 2.8 pF
- ASIC+sensor: Testbench and testbeam measurements give a larger detector capacitance than expected
  - 30 ps jitter obtained on test bench at Qinj = 10 fC with testpulse and sensor connected
  - 48 ps in testbeam
- ALTIROC1: 25 channels (PA+discri+TDC+FIFO)
  - Submission mid June 2018
  - Radiation tests in 2018 -2019
- Final ASIC: 225 channels with all the readout part



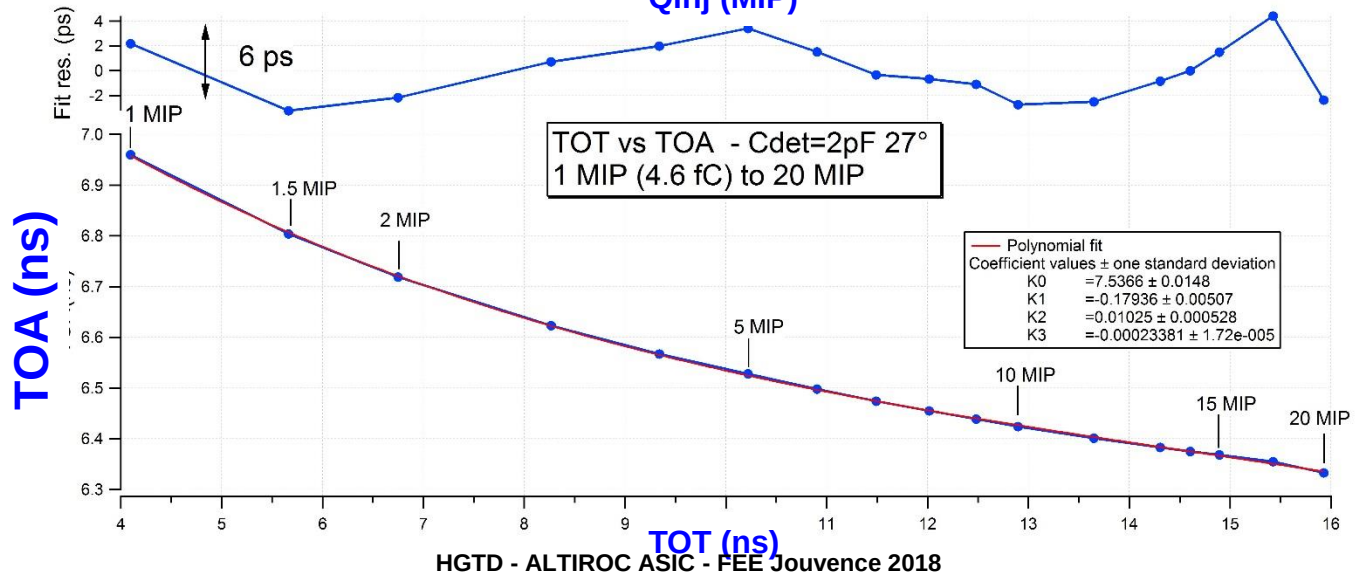
BACKUP

Time Walk correction

- Can be corrected using Time Over Threshold technique
- TOA position vs TOT value: polynomial fit , 700 ps variation corrected to better than 10 ps



$$\sigma_t^{TW} = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$



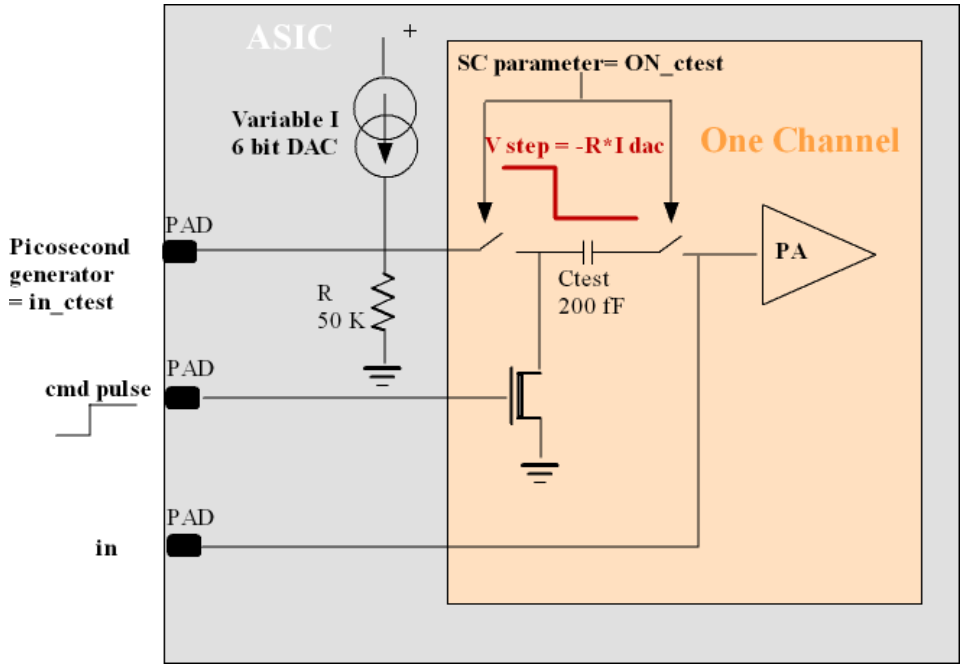
Internal pulser

- **To calibrate t0 and TOT**

External clocks needed by the TDC must exhibit a good phase stability (Phase jitter and drift between clocks between different ASIC must be < 5 ps)

Calibration of the absolute value of the phase:

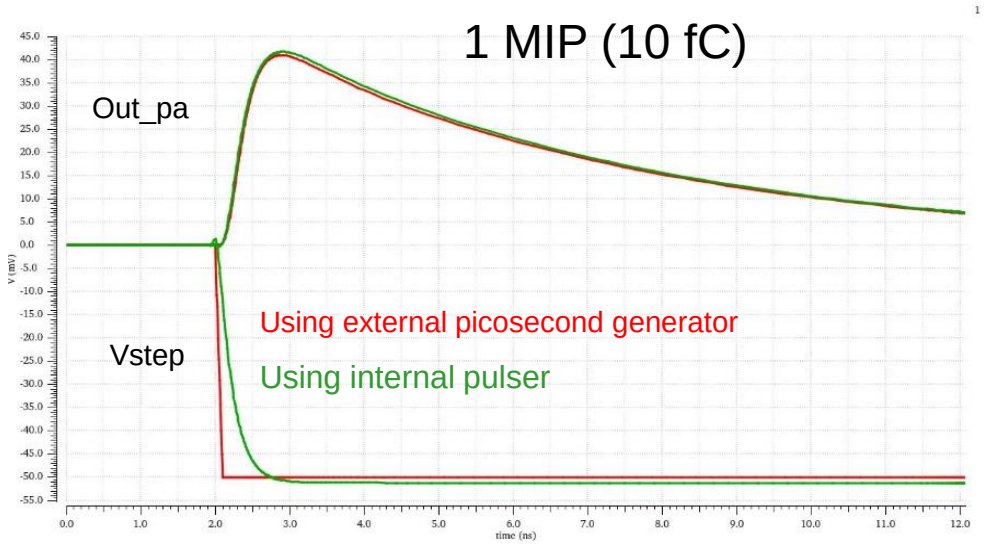
Measurement of t0 of each ASIC and channel thanks to an internal pulser



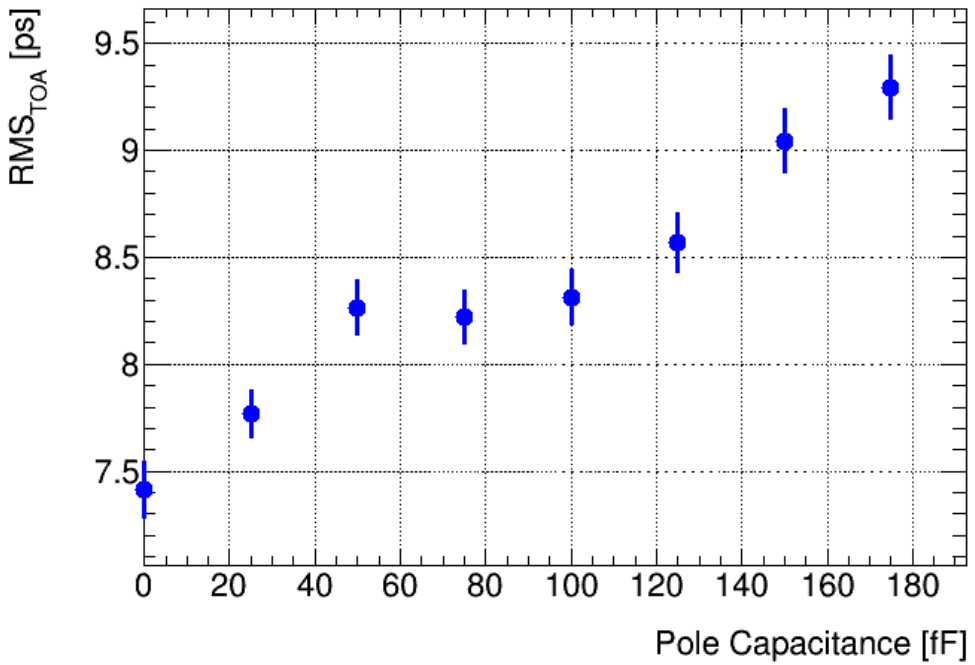
- **Principle:**

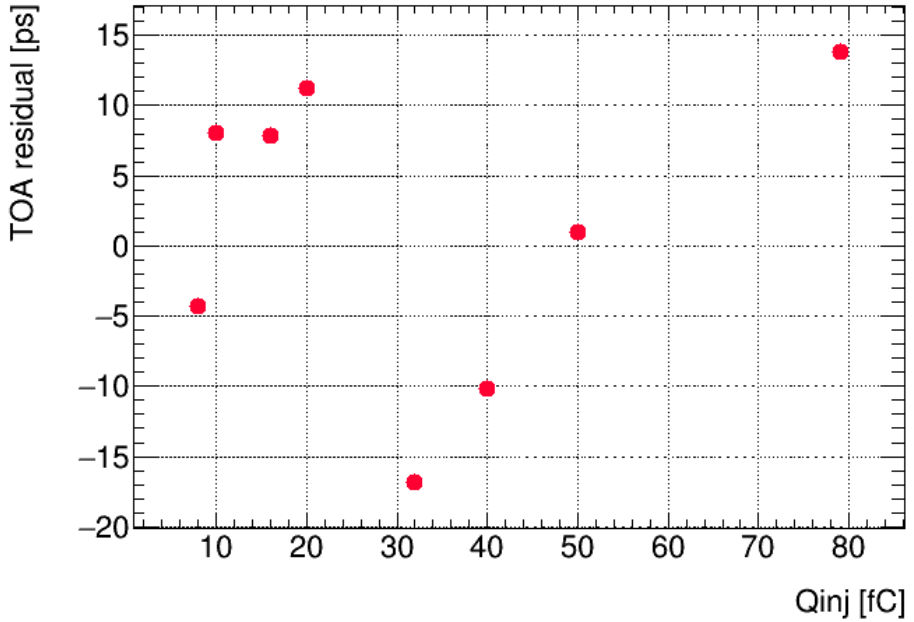
Programmable current (DAC 6 bits) that flows in a resistor R and that is interrupted by an external cmd pulse => Voltage step (=-R*I_{DAC} that is sent to the internal Ctest capacitor of each channel)

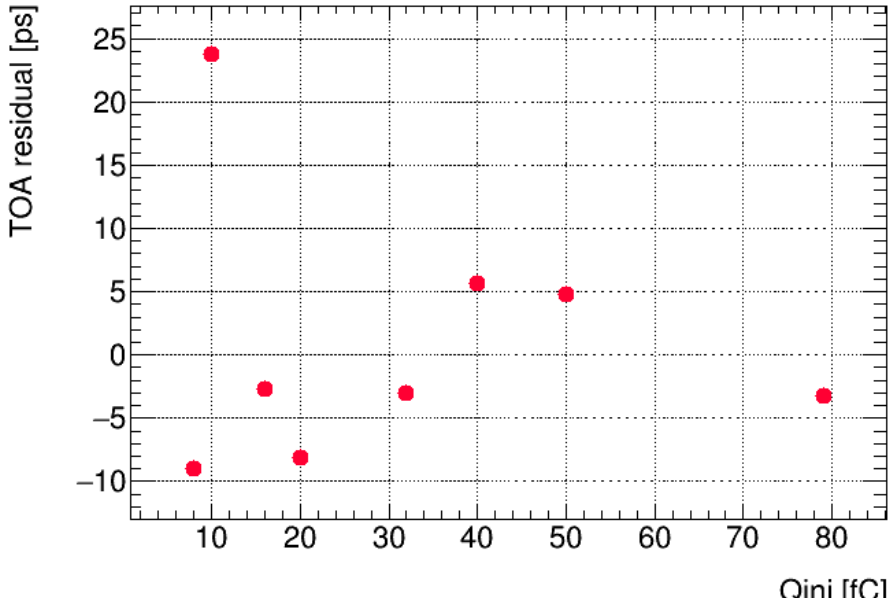
Dynamic range: 7,7 mV (LSB) to 500 mV or 1,5 fC up to 100 fC



ALTIROC0_V2 measurements







Power Consumption Summary

Time-to-Digital Converters			
TOA TDC (10% occupancy)		TOT TDC (10% occupancy)	
Vernier DL TDC	Coarse + Vernier DL TDC	Coarse + Vernier DL TDC TZ PA	Coarse + Vernier DL TDC Voltage PA
405 µW	**350 µW**	**360 µW**	**500 µW**
SRAM 19x400			
Read simultaneous with Write operation		Read disables the Write operation	
Write @ 40MHz (10% occupancy)	Write & Read @ 40MHz (10% occupancy)	Write @ 40MHz (10% occupancy)	Read @ 40MHz
125 µW	**460 µW**	**125 µW**	**180 µW**