CMOS sensors in 110 nm with full depletion of 200 um and above

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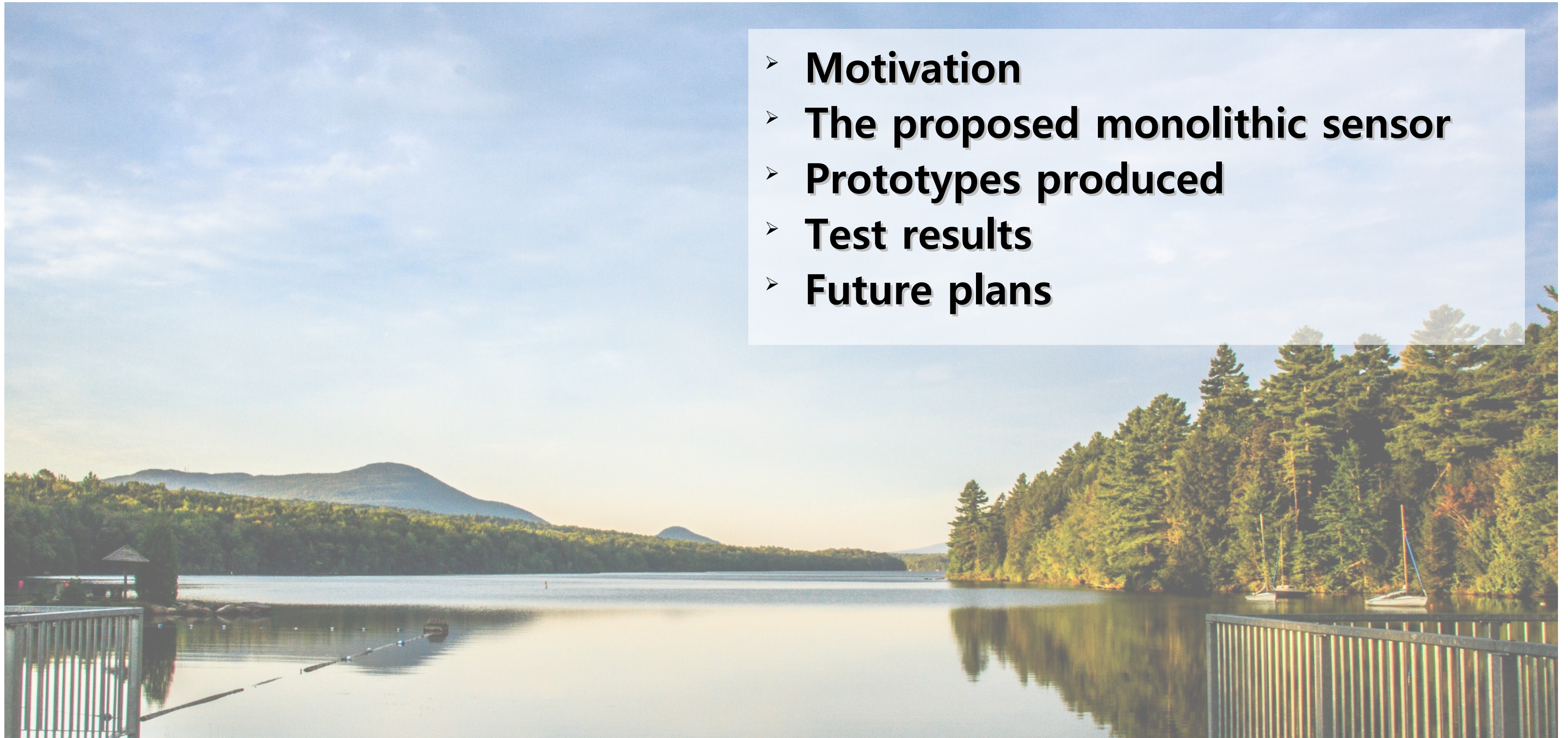
Jouvence
May 23th 2018

Jonhatan Olave
On behalf of the SEED collaboration

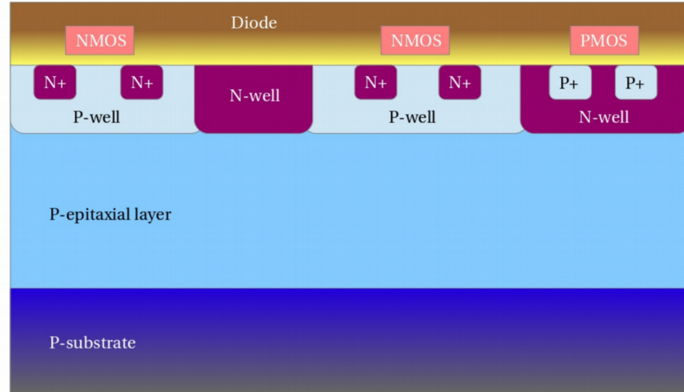
INFN TORINO

Outline



- Motivation
- The proposed monolithic sensor
- Prototypes produced
- Test results
- Future plans

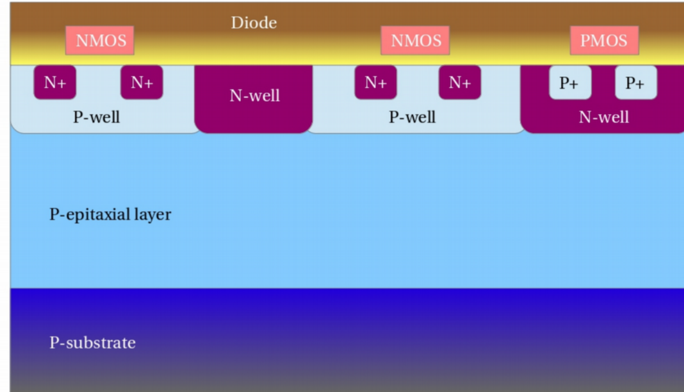
Monolithic sensors



Monolithic technology

- Sensor and readout electronics are built in the same silicon wafer
- Low material budget
- Low cost because only one fabrication process is needed

Monolithic sensors



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Partially depleted

- The sensing region extends for few tens of um
- The charge collection is performed mainly by **diffusion**
- Collection time > 10 ns
- Competitive charge collection → **low efficiency**
- Maximum radiation tolerance ~10^{13} neq/cm^2
- Low SNR

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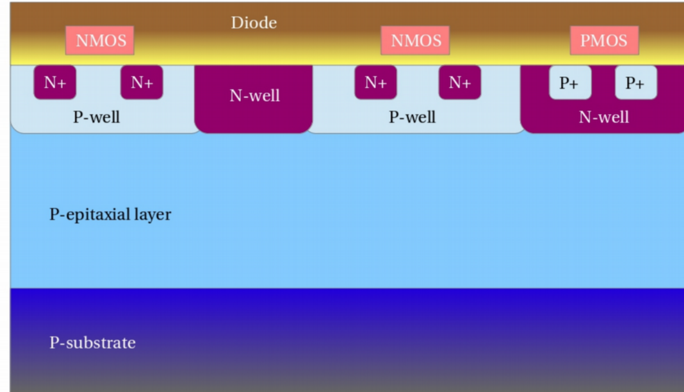
Monolithic sensors



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Fully depleted

- The charge collection is performed mainly by **drift**
- **Fast charge collection** (<10 ns)
- CMOS circuitry can be implemented
- **Competitive charge collection is avoided → good efficiency**
- High radiation tolerance
- Good SNR

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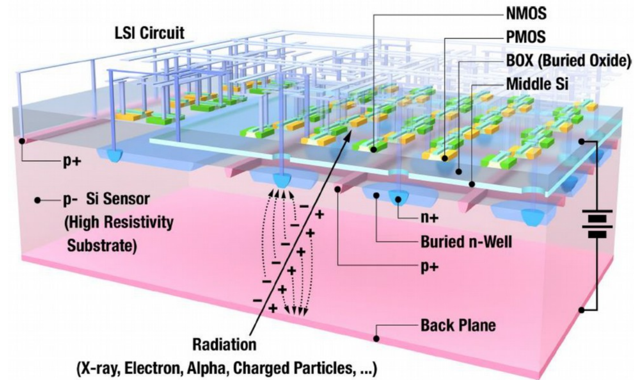
Large depletion: approaches adopted



Y. Arai, IEEE IEDM 2017

FD SOI

- Buried oxide used to separate the sensor from the electronics
- High resistivity substrate
- Buried oxide →gate effect →2 buried oxide layers used
- Radiation tolerance up to 10Mrad

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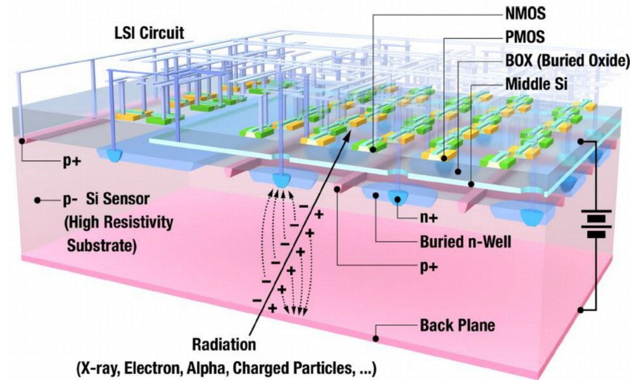

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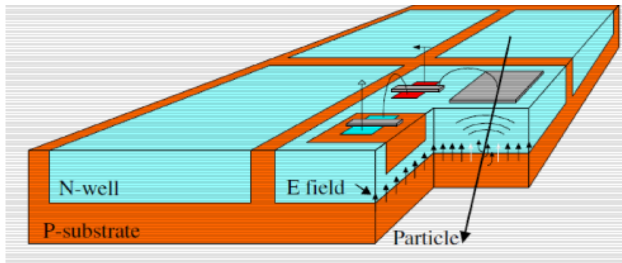
HV-CMOS

- High resistivity p-substrate (>2kΩ cm)
- The collector node is a deep nwell
- High voltages can be applied
- Fast charge collection
- High efficiency
- CMOS electronics built in the sensing node → high sensor capacitance → high noise



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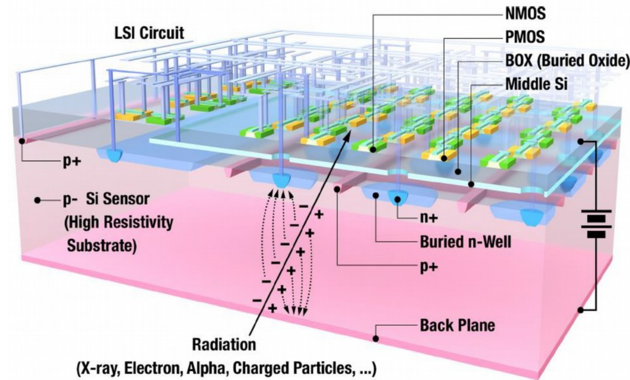

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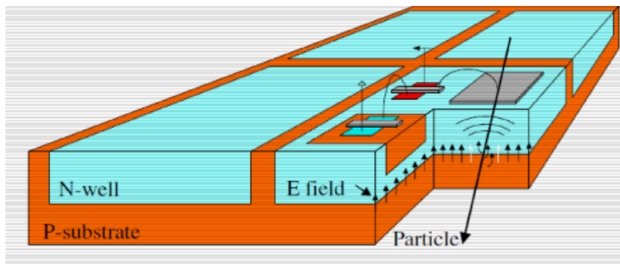
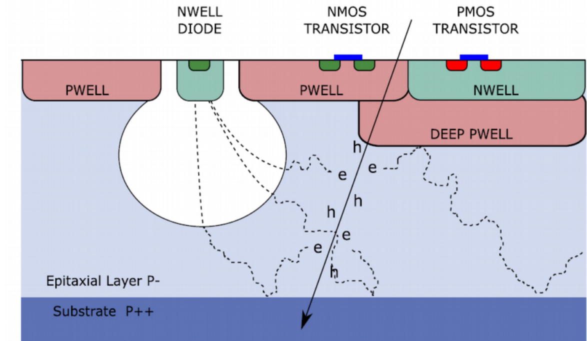


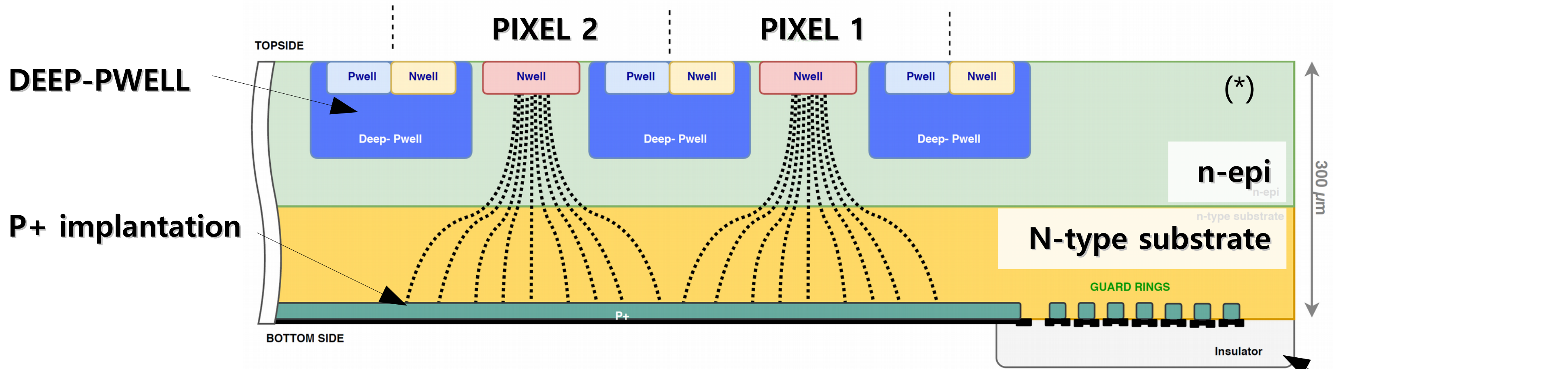


J.P. Crooks, et al., IEEE TNS 2007

ALPIDE

- High resistivity p-substrate (> 1kΩ cm) + epitaxial layer
- Partial depletion
- Sensing node shielded by a deep pwell
- Small sensor capacitance
- Radiation tolerance (TID) up to 700 krad

The proposed monolithic sensor



- **Goal**: full depletion in 100-500 um. The present prototype is 300 um.
- Technology: **110 nm CMOS** technology
- Sensor built on a **high resistivity** substrate
- **Custom backside process** developed in collaboration with an industrial partner
- The **depletion starts from the backside**
- At the backside, the **main diode is surrounded by a guard-ring**
- **Both NMOS and PMOS** transistors
- The **pixel capacitance is kept low** ~ 20 fF

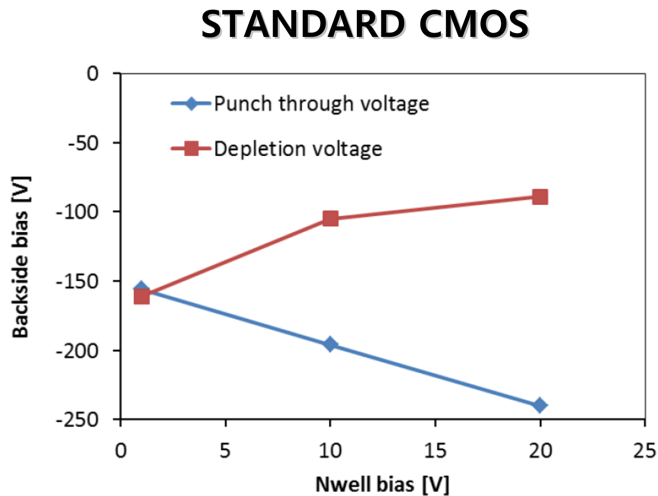
Multiple guard rings protection

(*) not to scale

Standard fabrication vs custom fabrication

Ingredients for reliability

- The bias voltage high enough to reach the **full depletion** avoiding an early **punch through**
- The difference between the punch through voltage and the full depletion voltage must be maximized. This allows to increase the electrical field and thus to get a much faster charge collection.



- The **maximum n-well** voltage allowed: 1.2 V

Standard fabrication vs custom fabrication

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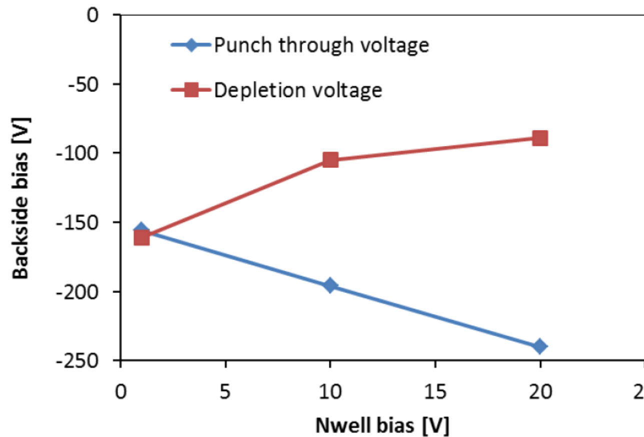

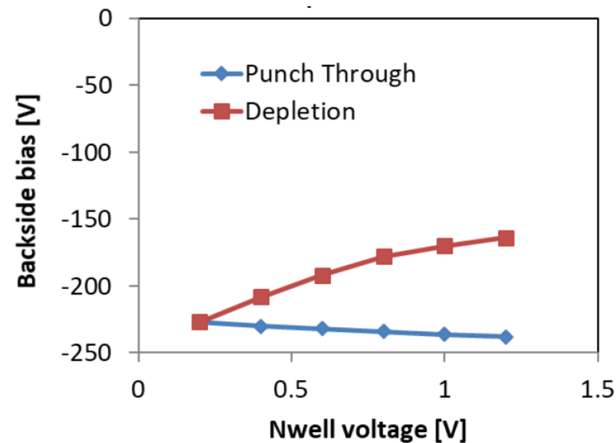

- The **maximum n-well** voltage allowed: 1.2 V
- The use of a **n-epi layer allows to increase the punch though voltage** allowing the full depletion also with low voltage CMOS process.

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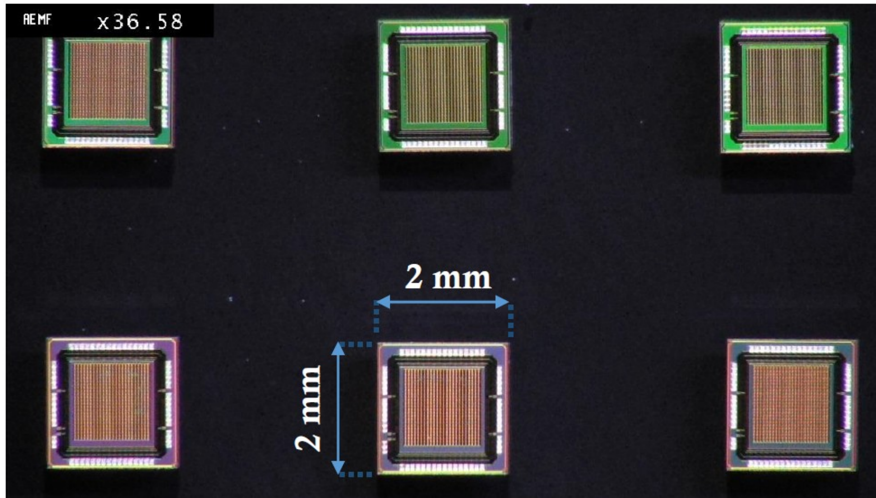
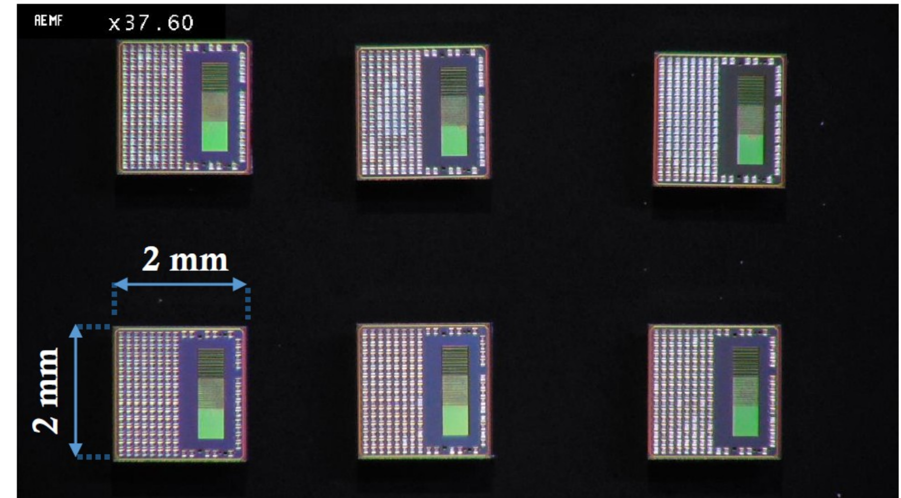
Set of prototypes

Complete monolithic sensor



Test chip

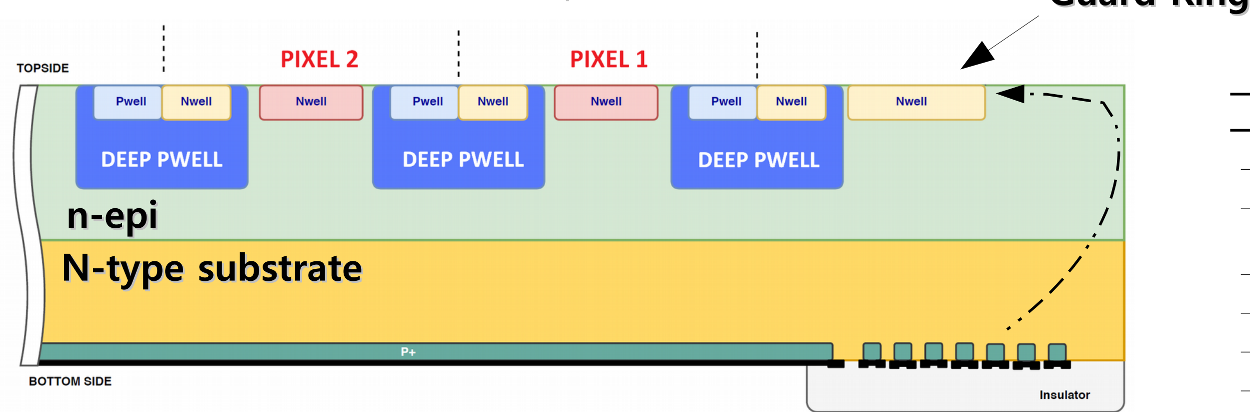


Technology	110 nm double side CMOS technology
Metal layers	6
Size	2 X 2 mm^2

- Wafers with small different epitaxial layer thickness have been used for the production

The MATISSE prototype

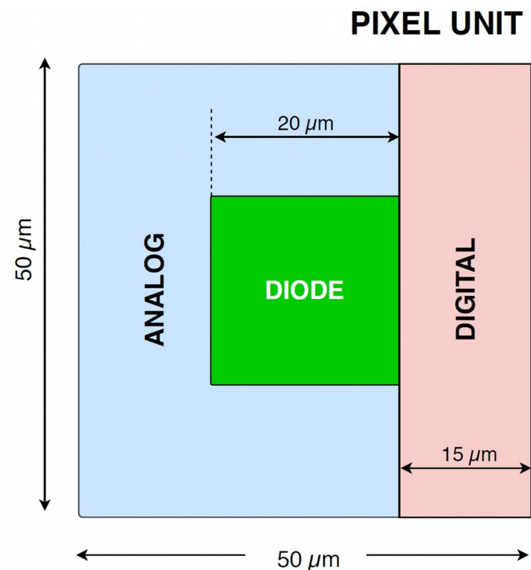
MATISSE = **M**onolithic **A**c**TI**v**E** pixel **S**en**S**or **E**lectronics

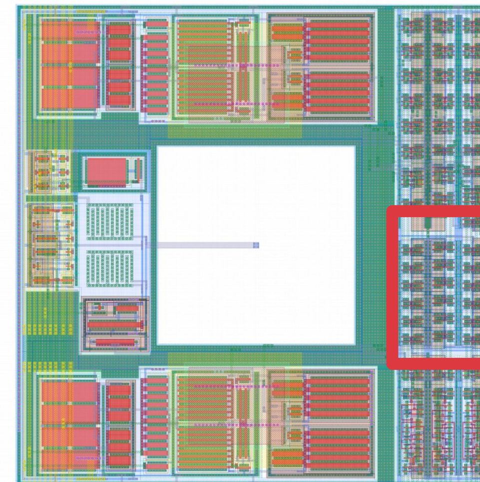


MAIN REQUIREMENTS OF MATISSE	
Technology	CMOS BSI 0.11 μm
Voltage supply	1.2 V
Measurements	Hit position Energy Loss
Number of channels	24×24
Input dynamic range	up to 24 ke$^-$
Sensor capacitance	$\sim$ 40 fF
CSA input common mode voltage	> 600 mV
Local memories	2 ($\sim$70 fF each)
Noise	< 100 e$^-$
Shutter type	Snapshot shutter
Readout type	Correlated Double Sampling Double Sampling
Readout speed	up to 5 MHz
Other features	Internal test pulse Mask mode Baseline regulation

- **MATISSE is a full monolithic sensor** with embedded electronics on board.
- The electronics built on the top side is compatible with a standard CMOS process fabrication flow
- On the top a **matrix array of 24 x 24** pixels is built
- Each pixel implements an analog readout in **global shutter**

Pixel architecture





Large digital buffer

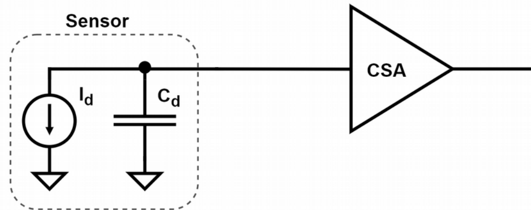
ANALOG

- Amplification stage
- Two memories
- Two buffers to drive the transmission bus
- Test pulse injection system
- Baseline regulation system

DIGITAL

- Logic for masking
- Registers for local programming
- Large digital buffer to test the digital noise injection from digital circuits

The analog in-pixel electronics



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The analog in-pixel electronics

- Analog gain defined as $1/C_f$

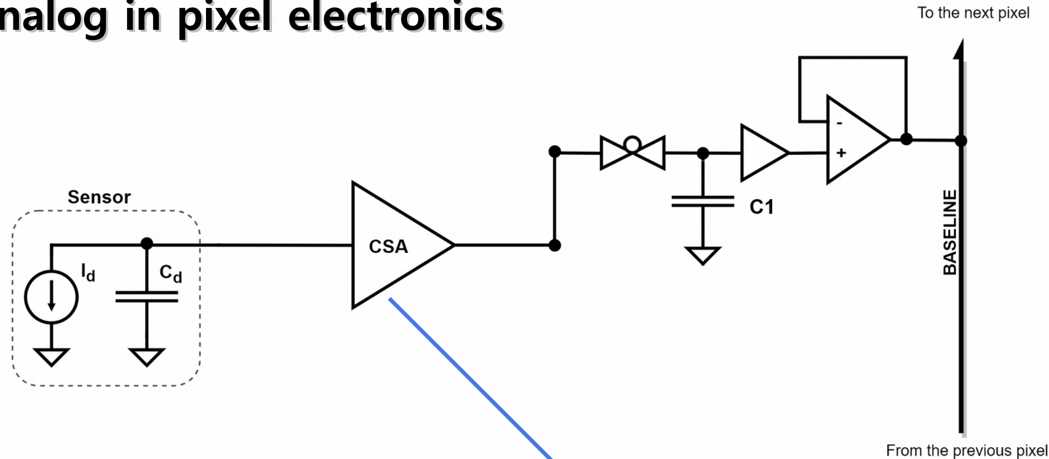
Sensor
I_d
C_d
CSA

CSA

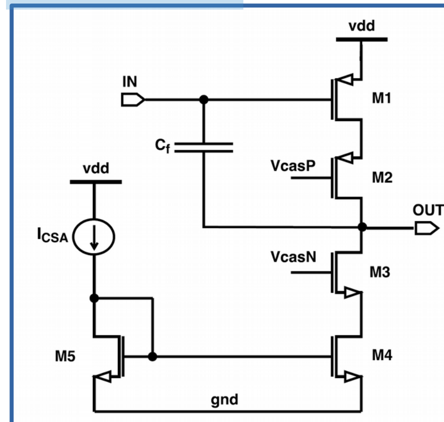
vdd
IN
M1
C_f
vdd
VcasP
M2
OUT
I_{CSA}
VcasN
M3
M5
M4
gnd

The MATISSE prototype

Analog in pixel electronics



CSA



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The MATISSE prototype

Analog in pixel electronics

- Analog gain defined as $1/C_f$
- Analog buffer based on a switched op-amp amplifier → high dynamic range

To the next pixel

Sensor

I_d C_d

CSA

C1

C2

BASELINE

SIGNAL

From the previous pixel

CSA

vdd

IN

M1

C_f

vdd

VcasP

M2

OUT

I_{CSA}

VcasN

M3

M5

M4

gnd

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The MATISSE prototype

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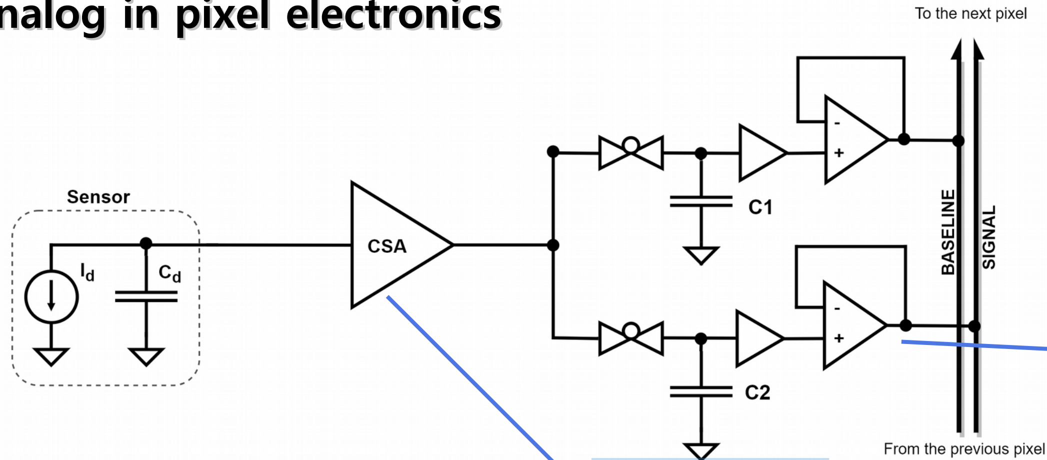

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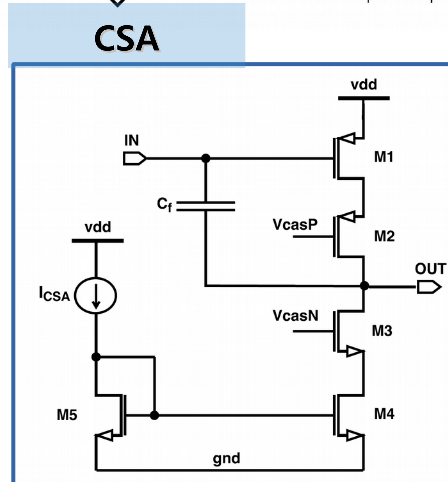
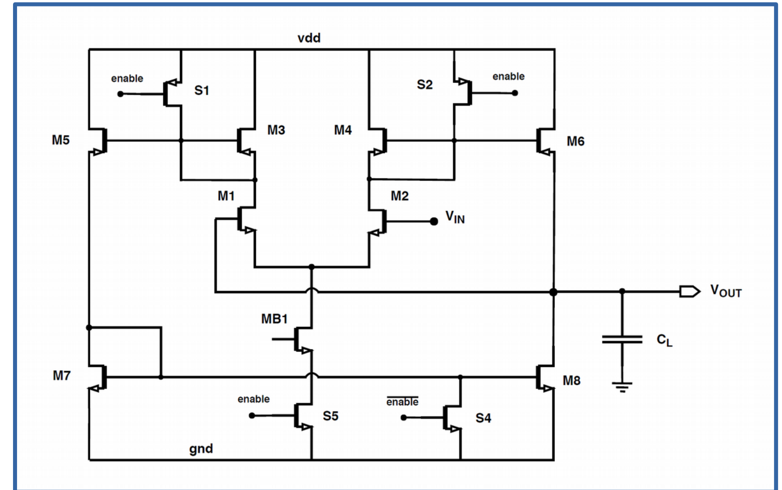


Analog Buffer



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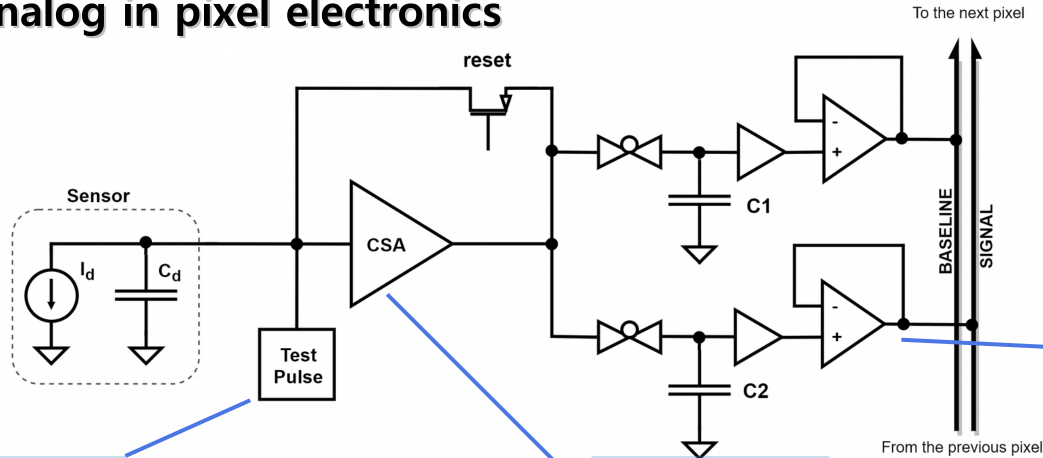

- Analog gain defined as $1/C_f$
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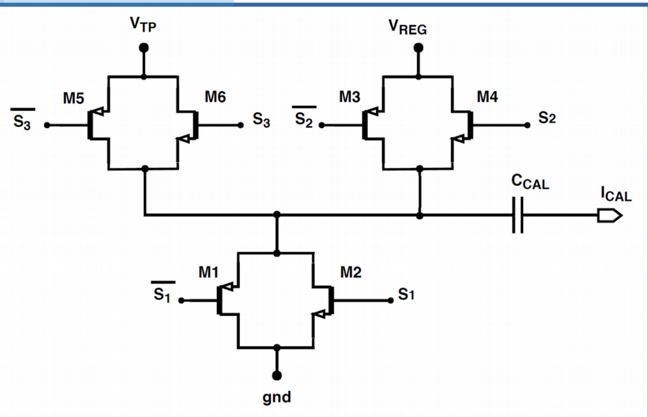
- The calibration system: test pulse injection and baseline regulation

Calibration



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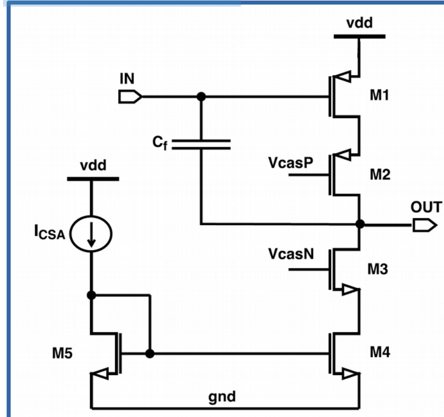

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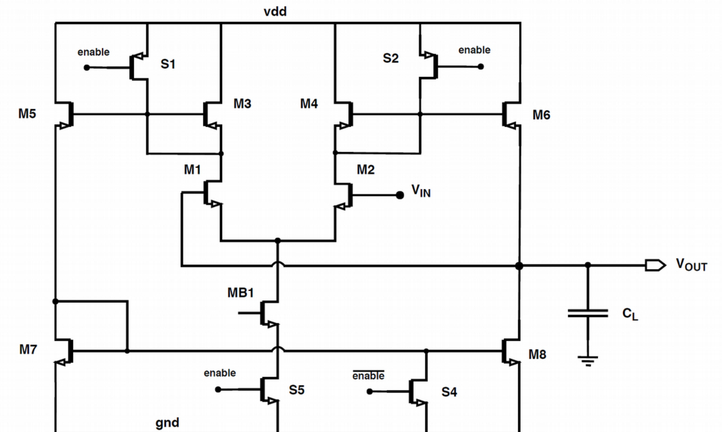

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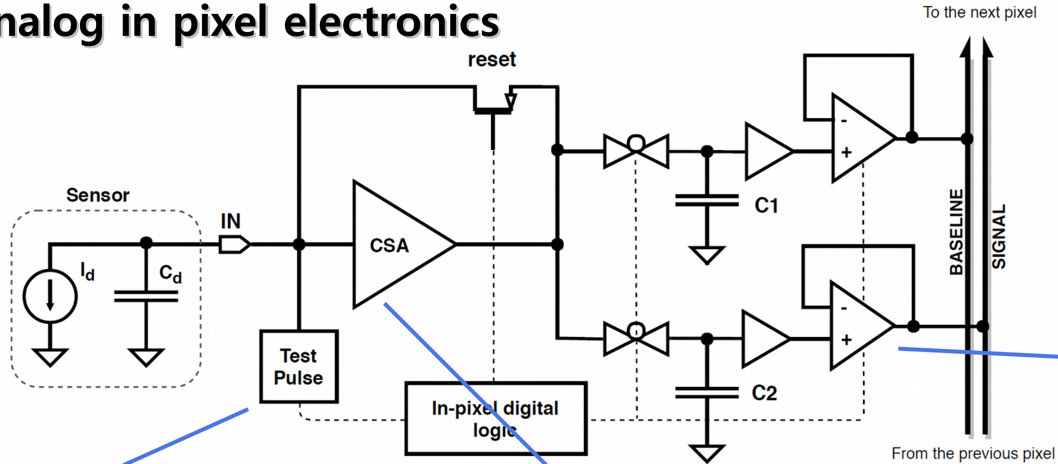

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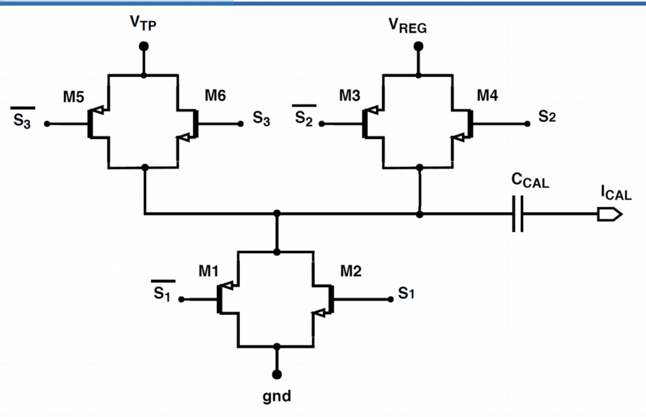

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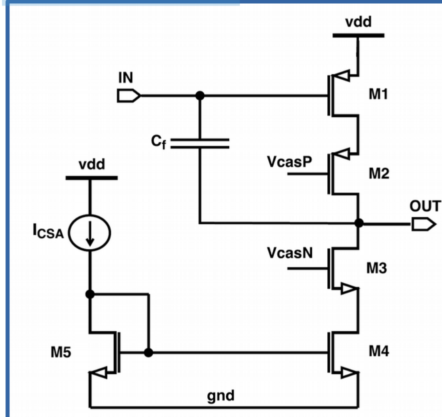

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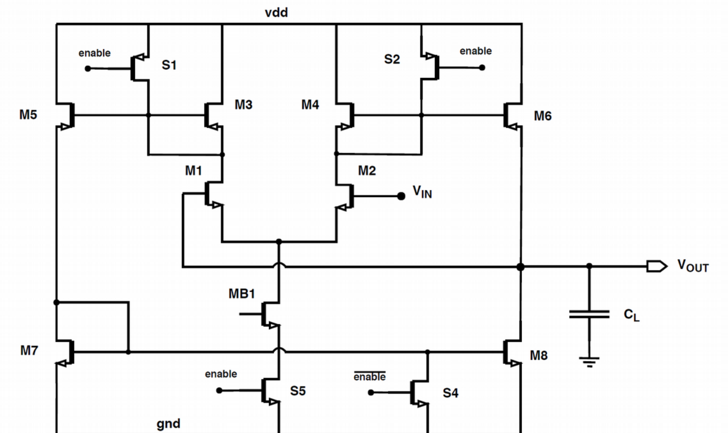

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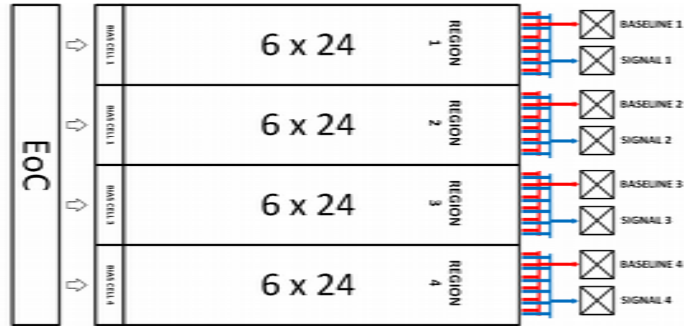
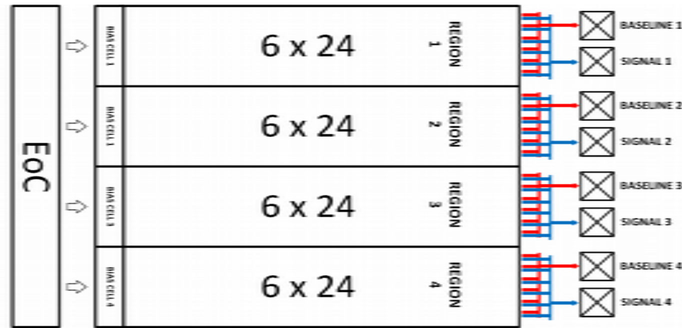
Readout scheme



- Matrix arranged in **four sectors** each made by 6 x 24 pixels
- Readout managed by a **End of Column** logic
- Each sector has **two analog outputs** sent off-chip

The readout logic



- Matrix arranged in **four sectors** each made by 6 x 24 pixels
- Readout managed by a **End of Column** logic
- Each sector has **two analog outputs** sent off-chip
- Column and row selection performed by means of **two clock signals**
- The logic based on rolling shutter
- The four sectors can be readout in parallel

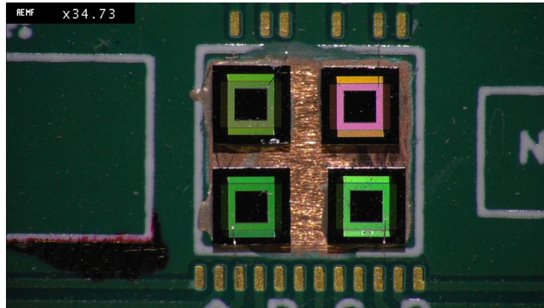
SECTOR

v_read_clk

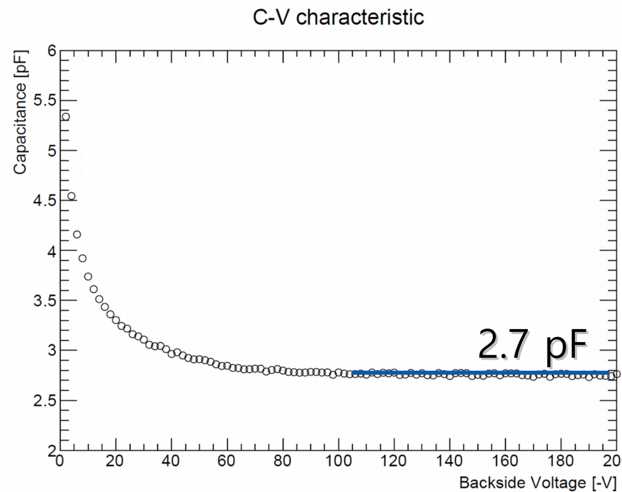
h_read_clk

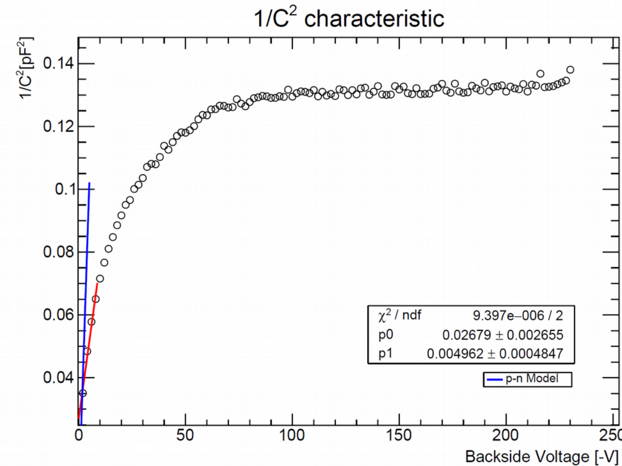
EoC Sector

Depletion studies



- In full depletion the capacitance is 2.7 fF in agreement with what have been measured in test structures
- The $1/C^2$ follows the expected trend of an asymmetric p-n junctions with doping concentration of the substrate only at low voltages





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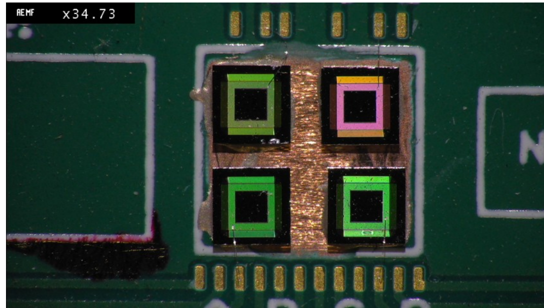
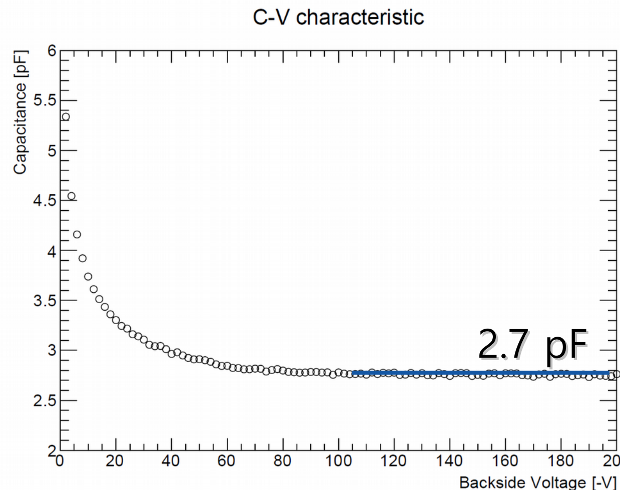
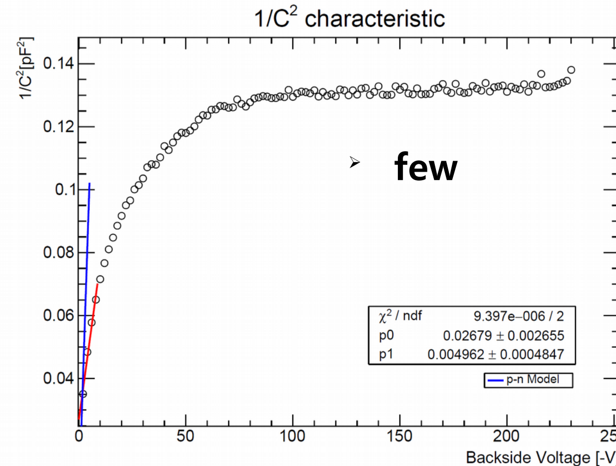
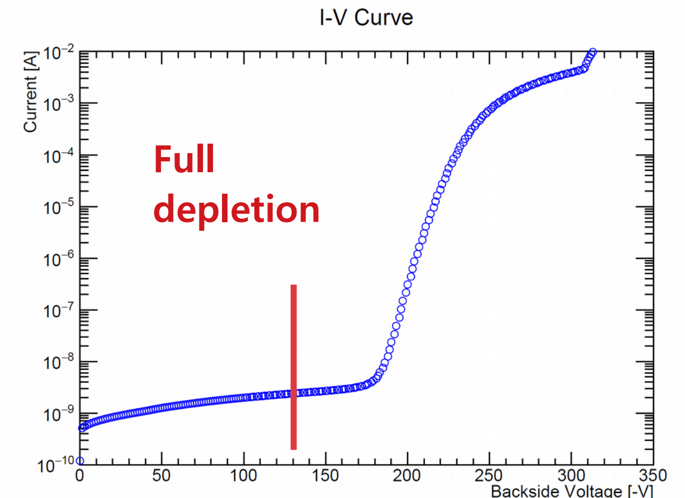


- In full depletion the capacitance is 2.7 fF in agreement with what have been measured in test structures
- The $1/C^2$ follows the expected trend of an asymmetric pn junctions with doping concentration in the order of $10^{12}cm^{-3}$ only at low voltages
- I-V shows leakage currents of **few nA** up to 180 V
- **Maximum voltage** before breakdown is **240 V**







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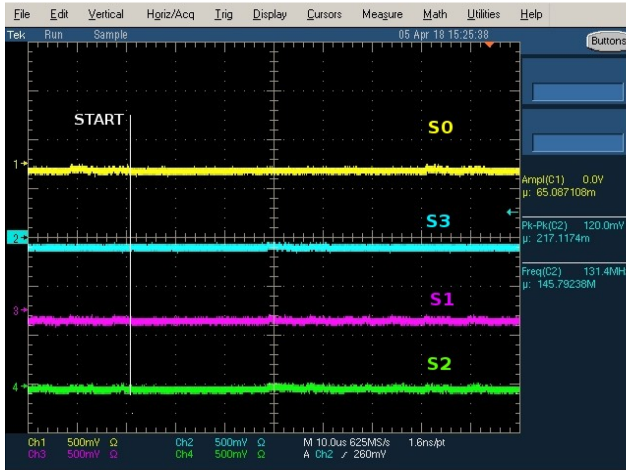

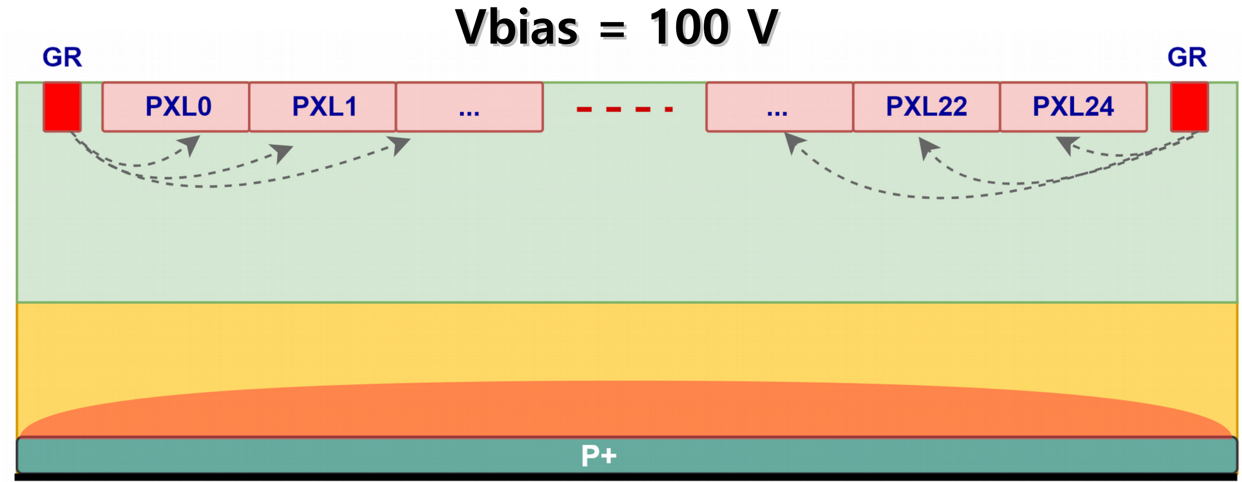

- At 100 V the leakage current injected to all the channels generates the saturation of the whole matrix

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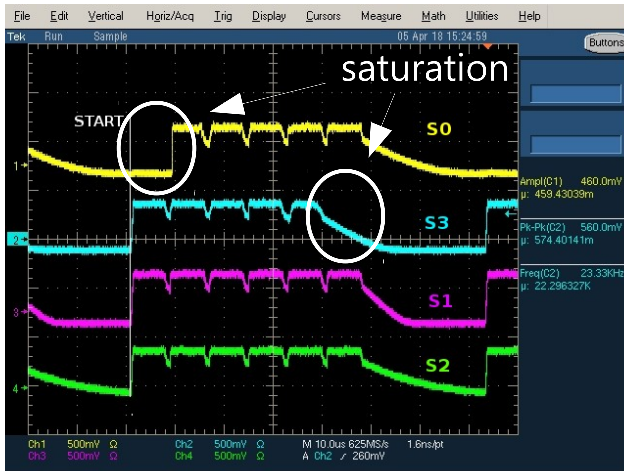

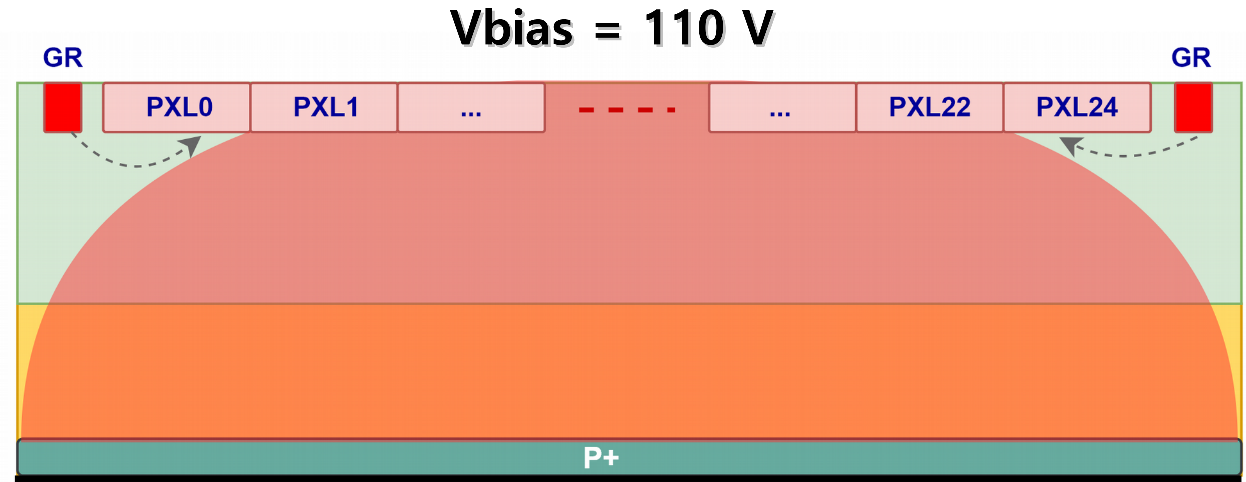

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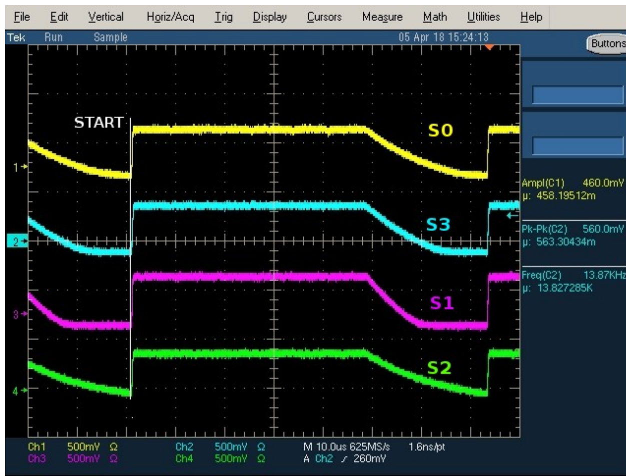
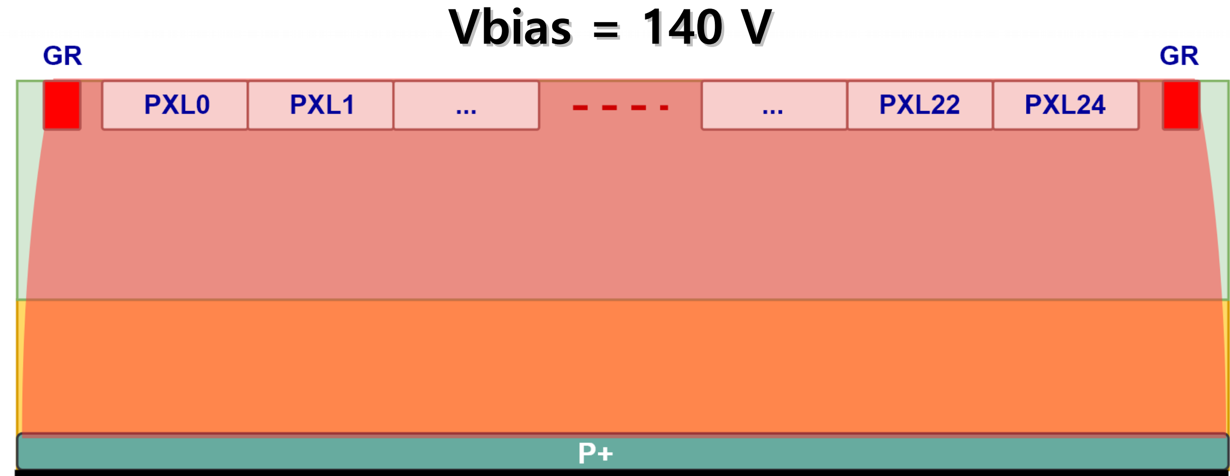
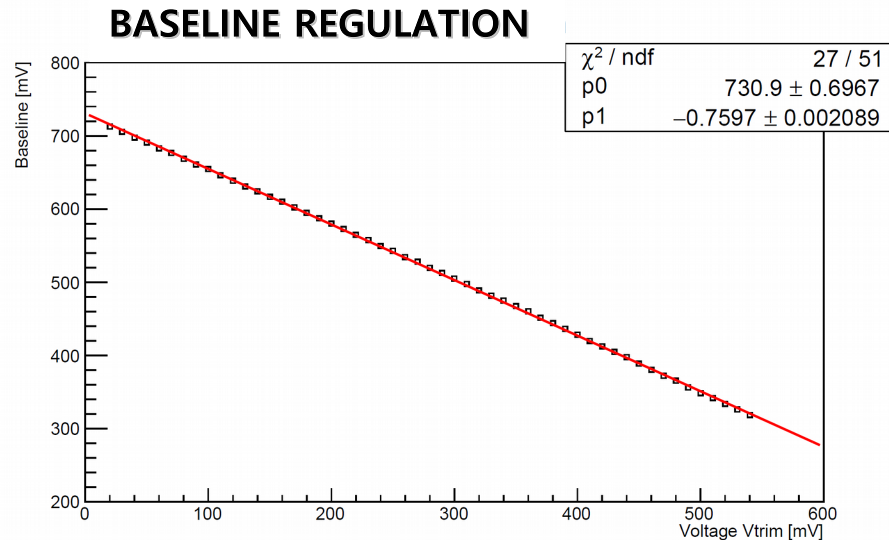




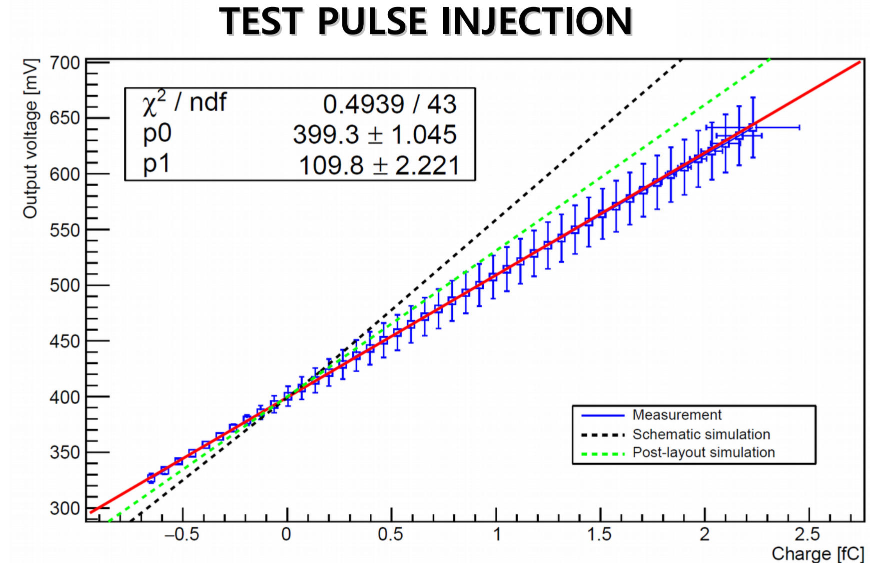
- At 100 V the leakage current injected to all the channels generates the saturation of the whole matrix
- At 110 V the depletion region reaches the topside. First, the pixels in the middle sees the effect of depletion. External pixels still receive a high leakage current
- For voltages higher than 140 V, the channels do not see any leakage current at the input transistor
- Parasitic currents along the chip edge has been observed. They are collected by the guard ring built around the matrix array

Electrical test (I)

BASELINE REGULATION

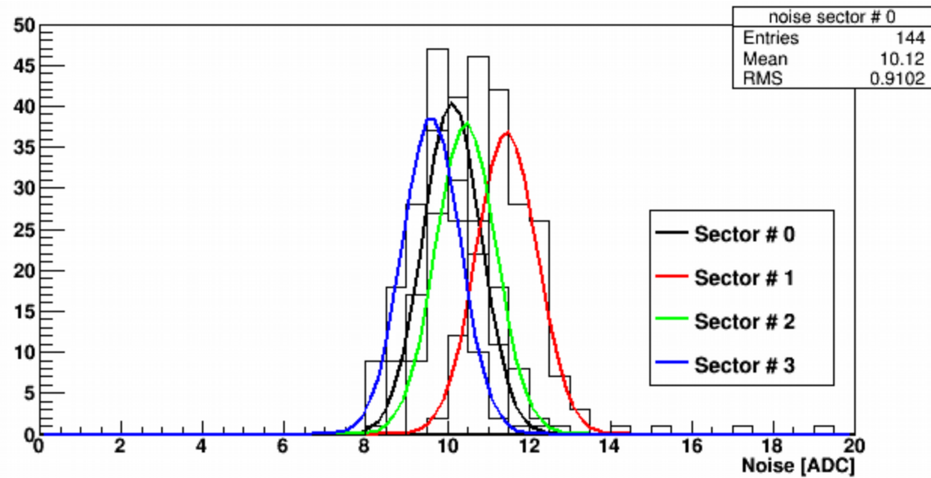


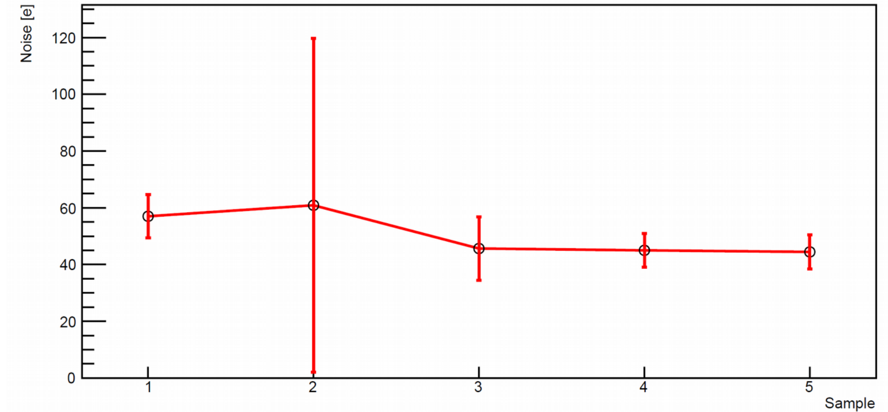
TEST PULSE INJECTION



- The baseline regulation system allows a regulation between 400 mV – 700 mV
- Linearity has been explored with test pulse injections: excellent linearity observed in the full range.
- Thanks to the versatile test pulse injection system also **negative pulses** can be used to explore the region below the baseline
- The comparison with schematic and post layout simulations shows a slightly smaller gain. Parasitics increases the effective feedback capacitance → analog gain is slightly smaller than simulations

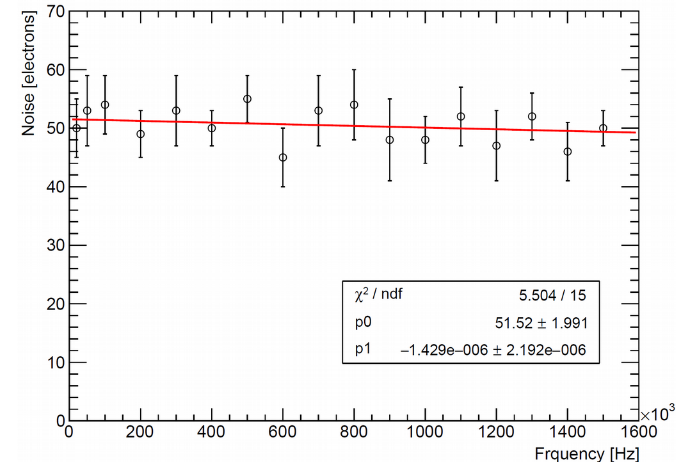
Electrical test (II): noise





- Noise is measured as the standard deviation of the baseline distribution.
- All the sectors have similar noise performances
- Noise is 420 ADC counts 50 electrons of noise
- **Digital noise with frequencies up to 1.6 Mhz does not give any effect on the analog noise**

The analog circuitry is well isolated by the digital circuitry built on the pixel cell



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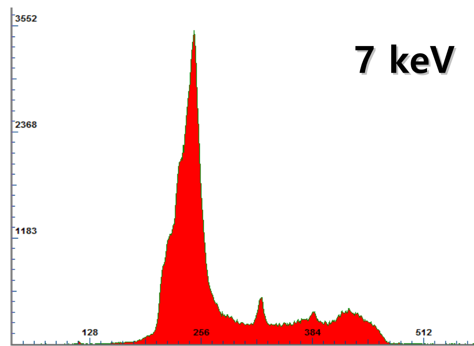
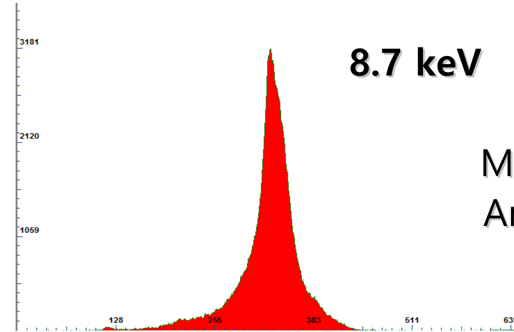
Xray measurements

- Calibration made by means of the facility for total dose RP-149 Semiconductor Irradiation System.
- A monochromator has been used to get a monochrome spectrum.
- Two different energies selected: 7 KeV and 8.7 KeV.

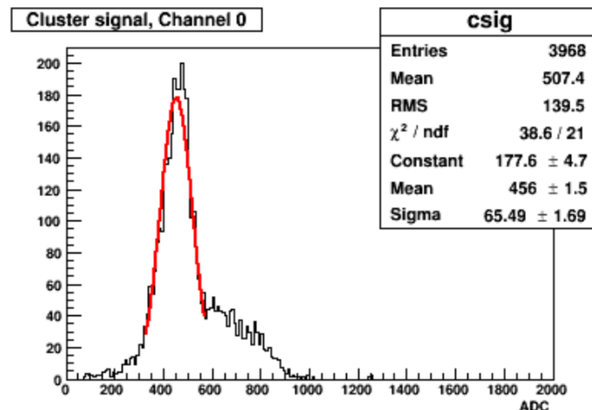


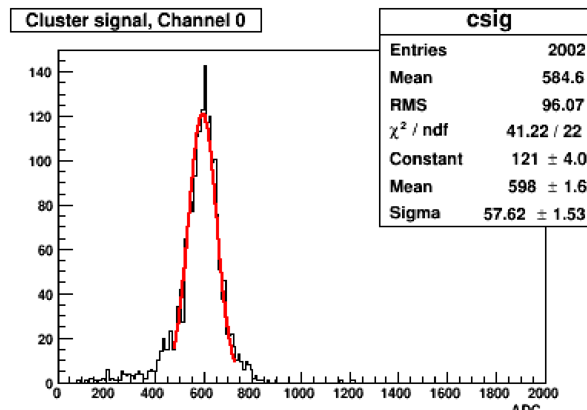
7 keV



8.7 keV

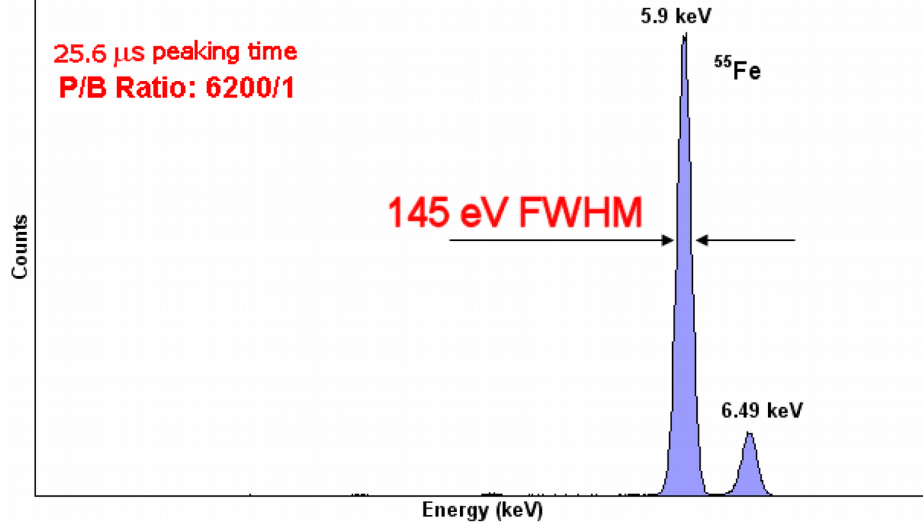
Measured with the Amptek XR-100CR

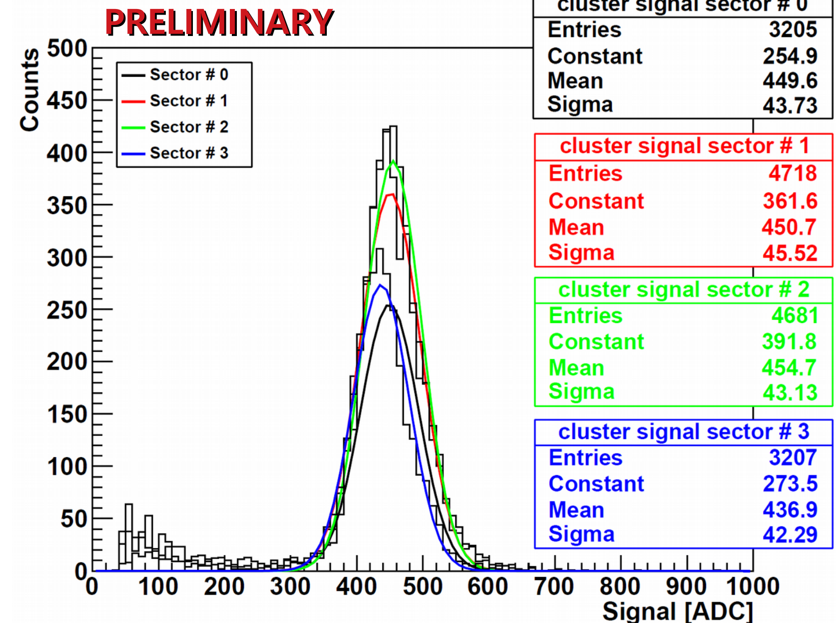




Measured with MATISSE

Measurement with 55Fe



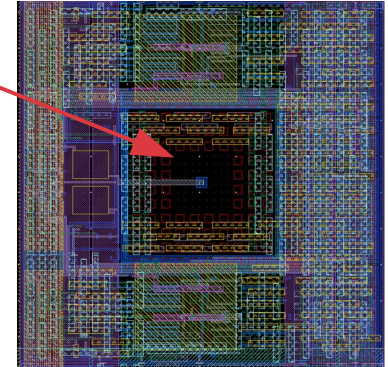


- The four sectors exhibit very similar analog gain
- The measurement has been used to calibrate the analog gain to 116 mV/fC
- FWHM is 1300 eV which is not enough to see the secondary peak → more statistic is required

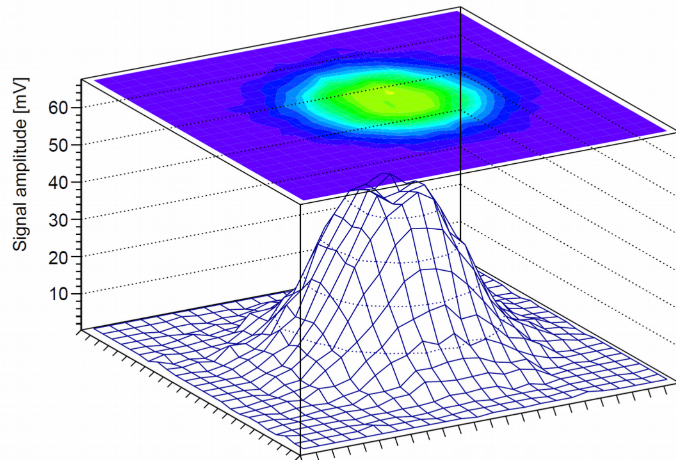
Laser measurements

- The metal fillers of the channel has been designed so that left free the pixel centre for optical measurements.
- A laser of with a **wavelength 1060 nm** has been used for the measurements
- The laser spot has been focused up to reach a diameter 8 um
- Laser sent to 16 pixels in the matrix

Low metal density

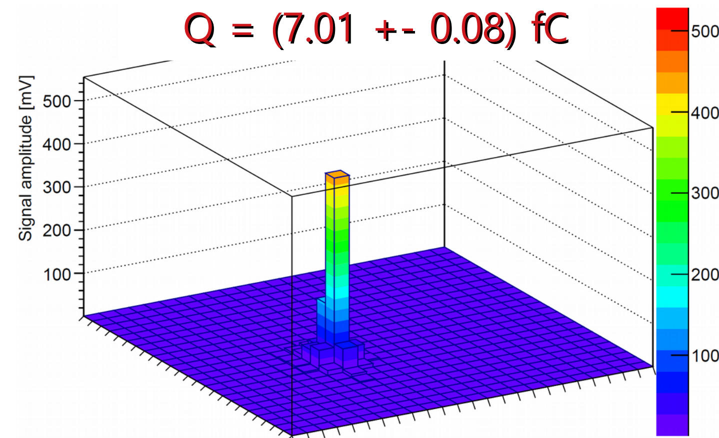


Non focused pulse



Focused pulse

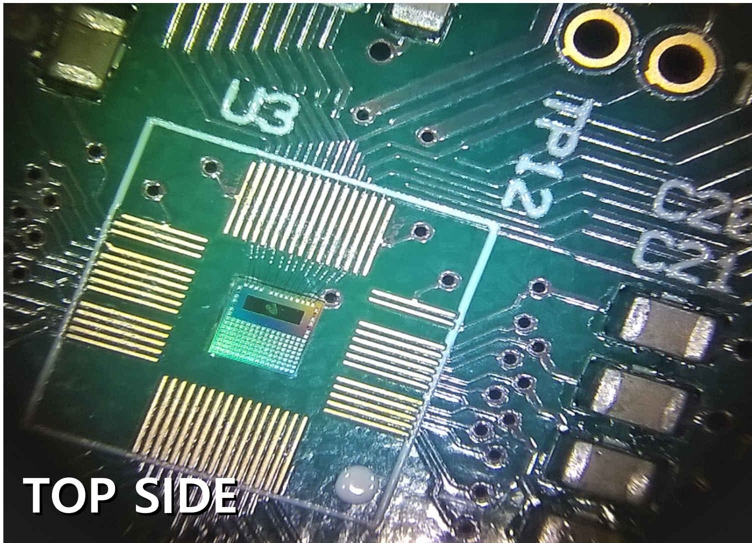
Q = (7.01 +- 0.08) fC

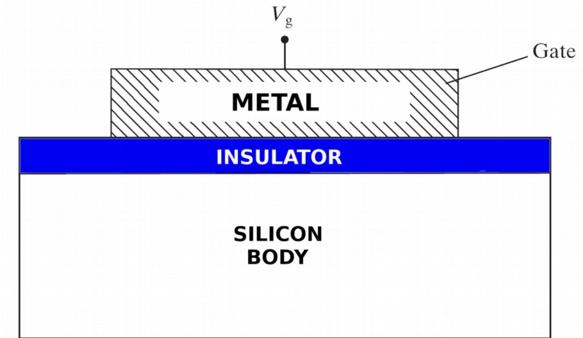


FRONT END ELECTRONICS 2018

Test chip description

Technology	BSI CMOS technology
Metal layers	6
Substrate	High resistivity (n-type)
Size	2 X 2 mm^2
Test structures	Test diodes Test matrices Test capacitor (MOS)

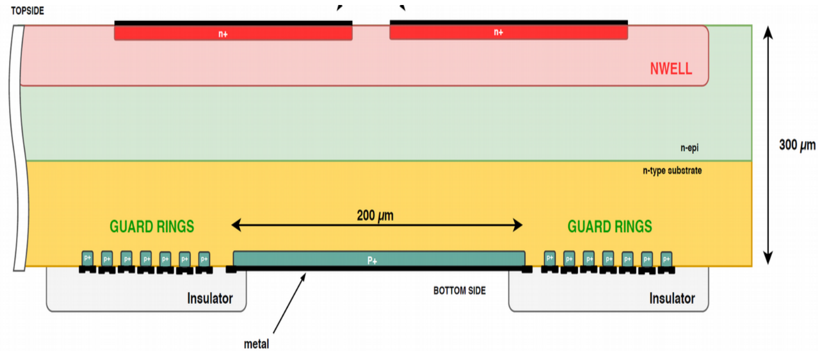




MOS capacitor

- The MOS capacitor is built for quality verification purposes of the BSI layers.
- The insulator is the same one used to build the guard-rings of the diodes and matrices
- **Area**: 300 µm X 300 µm
- Used to study parameters like the thickness oxide, the trapped charge concentration.

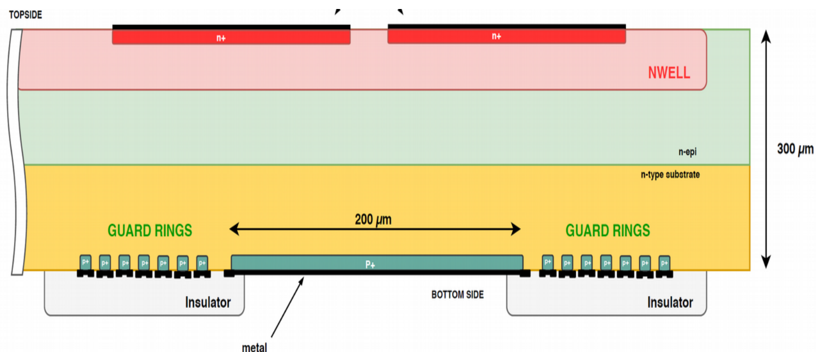
Test diodes



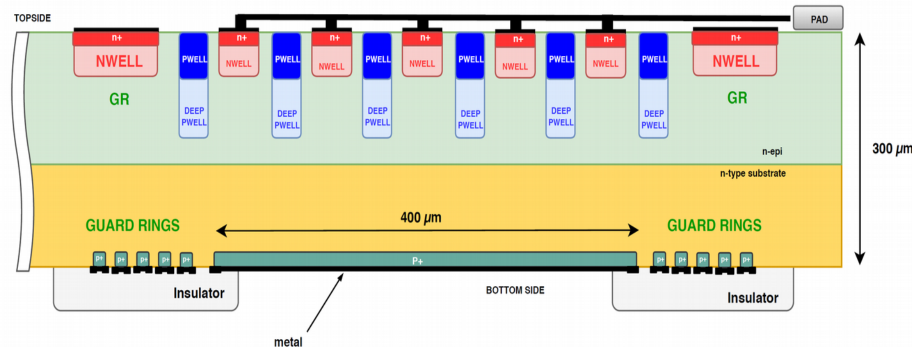
- **Area**: 200 µm X 200 µm
- **8 different diodes** implemented to determine the optimal GR structure
- Diodes differs by the **number of rings** and **pitch** used to build the guard-ring.

- **Two** groups:
  - Pitch 6 µm: 5, 20 and 30 rings
  - 10 rings: pitch of 5, 6 ,7 and 8 µm

Test diodes



Pseudo-matrices

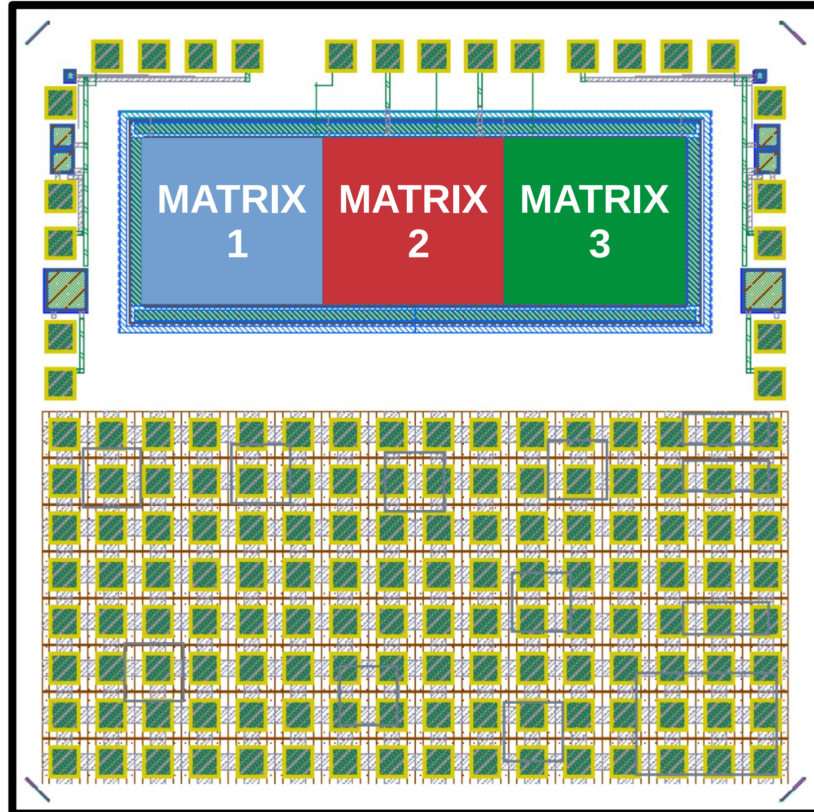


- **Area**: 200 μm X 200 μm
- **8 different diodes** implemented to determine the optimal GR structure
- Diodes differs by the **number of rings** and **pitch** used to build the guard-ring.
- **Two** groups:
  - Pitch 6 μm: 5, 20 and 30 rings
  - 10 rings: pitch of 5, 6 ,7 and 8 μm

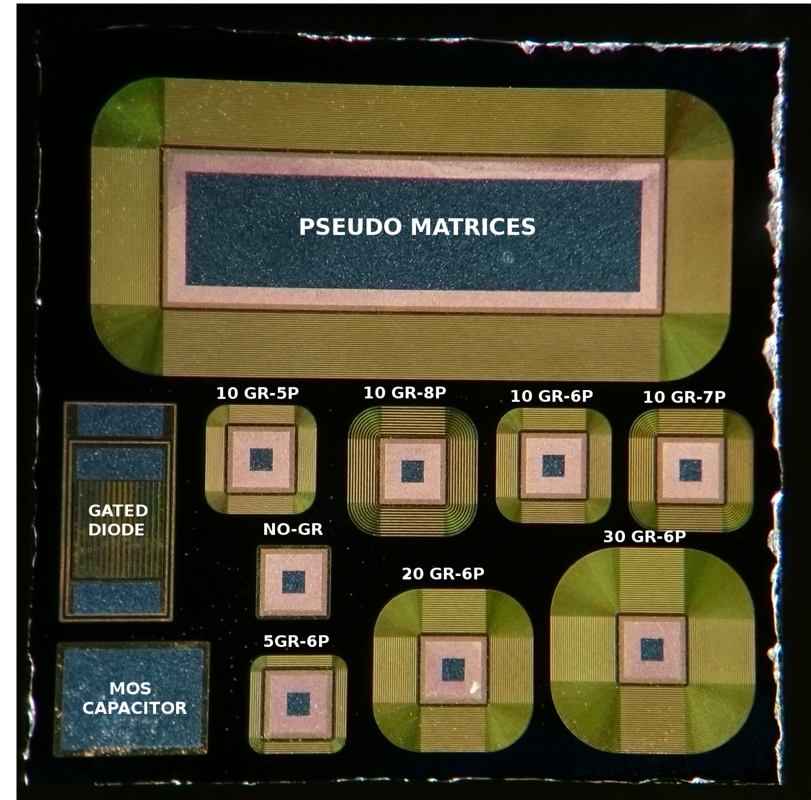
- **Three** matrices with different pixel sizes has been developed: 10 μm (8 x 9), 25 μm (16 x 18) and 50 μm (40 x 45)
- On the top side is built the deep-pwell required to implement the CMOS electronics
- No electronics is built on the pseudo matrices
- Each pixels has a collector node (nwell) in the middle
- All the collector nodes of a matrix are shorted and connected to a PAD

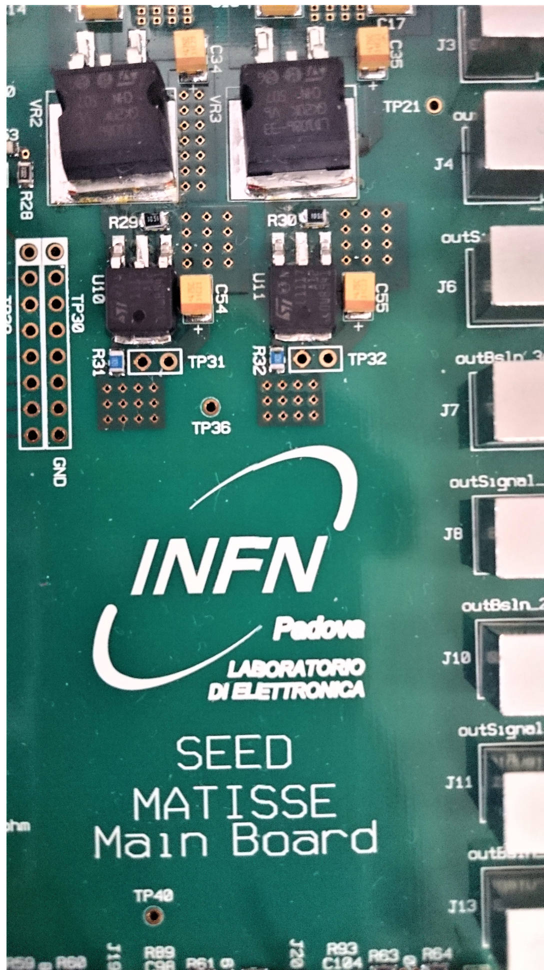
Test chip

TOP

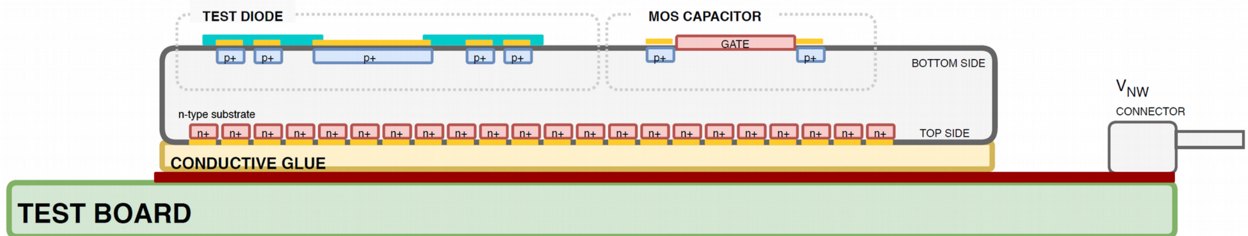


BOTTOM

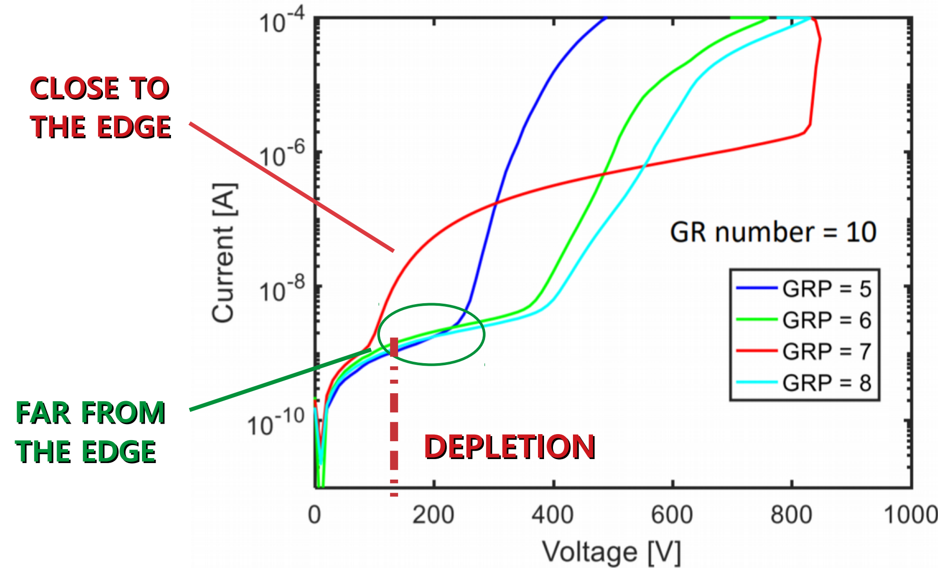


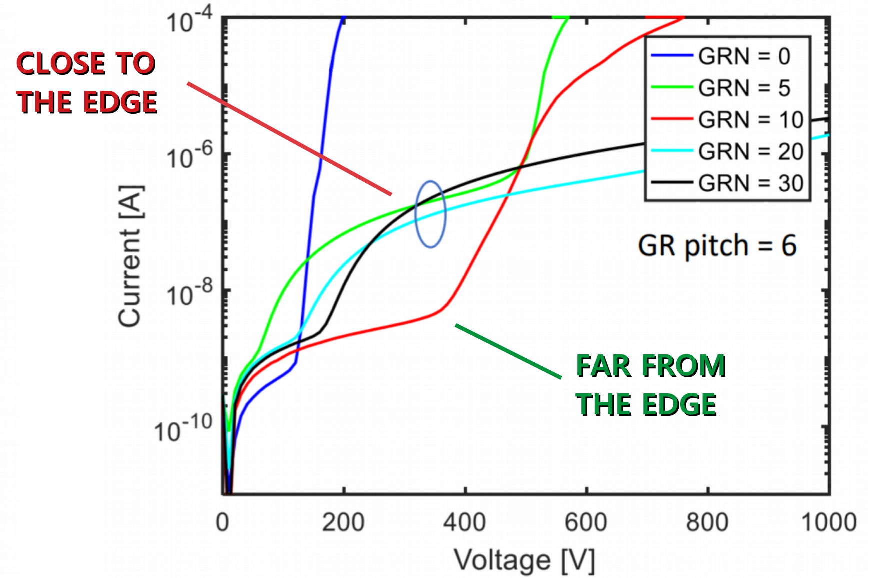


Test results



Test diodes: IV curves





- The breakdown voltage for all the samples is higher than 400 V. Only for the diode without GR the current suddenly increases around 180 V.
- Diodes placed far from the chip edge have in general low leakage current. Good results are obtaining with the guard-ring made by 10 rings with pitch of 6 um. In this case leakage is kept below 3 nA up to 400 V.

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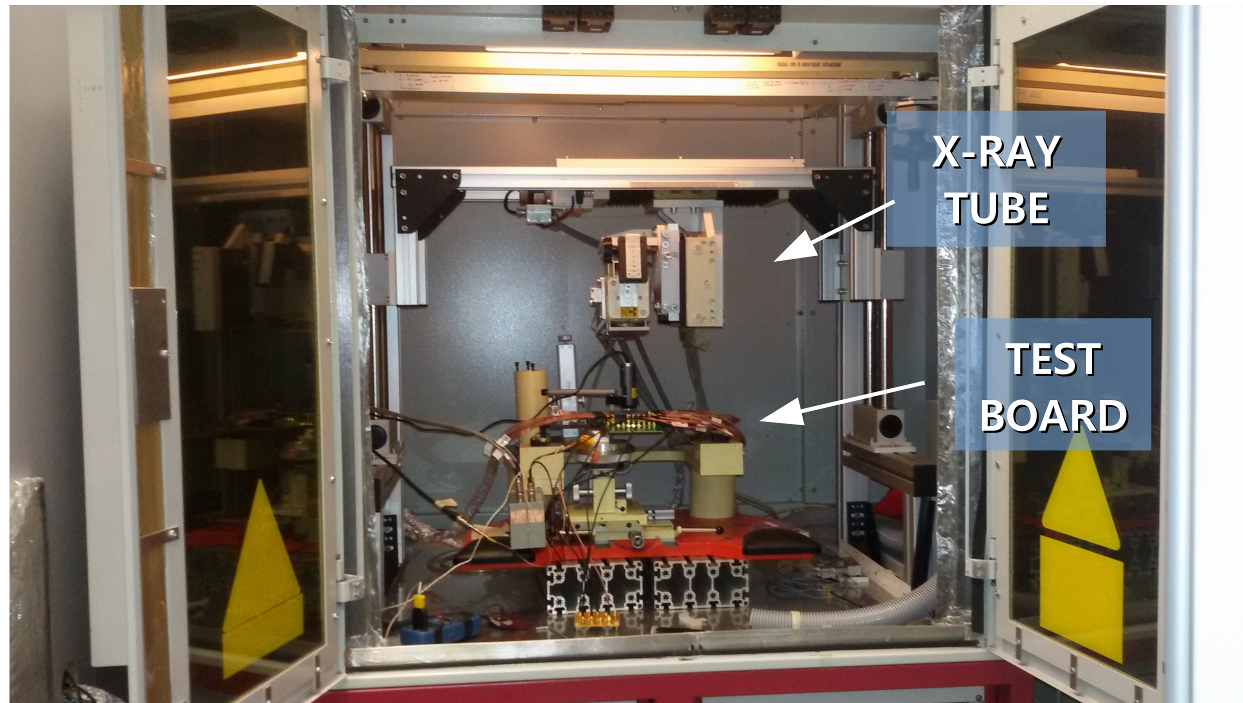
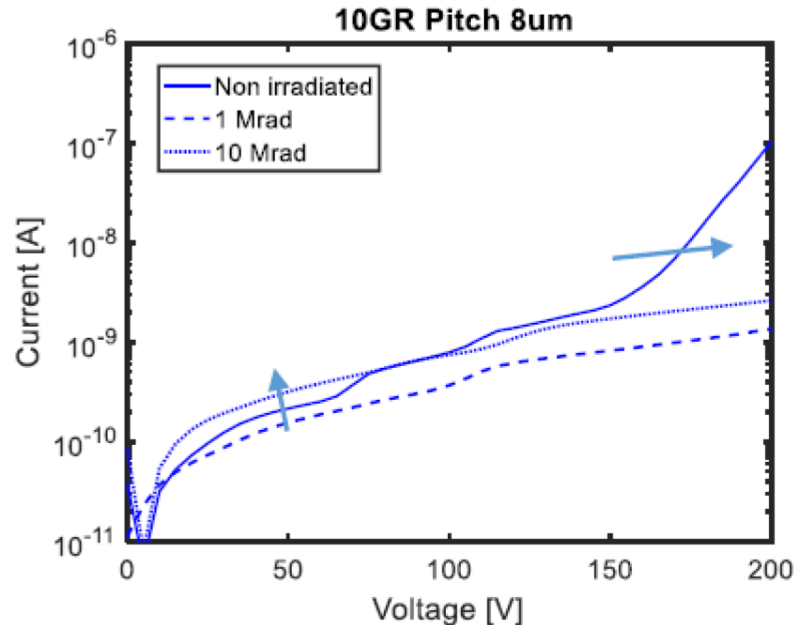
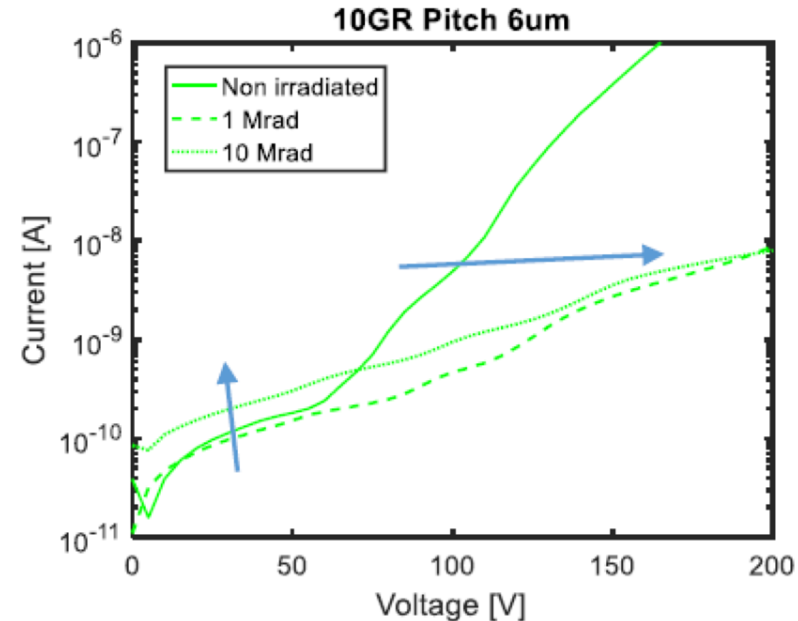
Test diodes: Irradiation tests

The irradiation tests have been carried out at the INFN of Padova. The facility is the RP-149 Semiconductor Irradiation System from Seifert equipped with a X-ray tube based on a tungsten anode.



Test diodes: IV curves before and after irradiation





- The test diodes have been irradiated up to 1 Mrad and 10 Mrad
- All diodes behave in similar way: the effects of irradiation contrast the trapped charge in the oxide allowing to recover the guard-rings. Two effects are observed: the breakdown moves towards high voltages and the leakage slightly increases as expected but it is still below 1 nA

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Summary

- First production: **300 um thick monolithic sensor** developed and tested with excellent results
- The full depletion has been proved by means of leakage measurements
- Test structures has been developed to prove the possibility to increase the maximum sensor bias voltage up to 1000 V
- The embedded electronics has been tested with good results. Test on the digital part guarantee the optimal isolation between the analog and digital domain

Future work

Measurements to complete the sensor characterization:

- Dedicated laser measurements to **study the charge collection**
- Measurement of the **collection time** with a laser an external amplifier
- **Studies of radiation damage** with neutrons (IEL and NIEL)
- **Beam test** is planned at the end of 2018

New run with different substrate thickness:

- 100 – 150 um
- 500 um

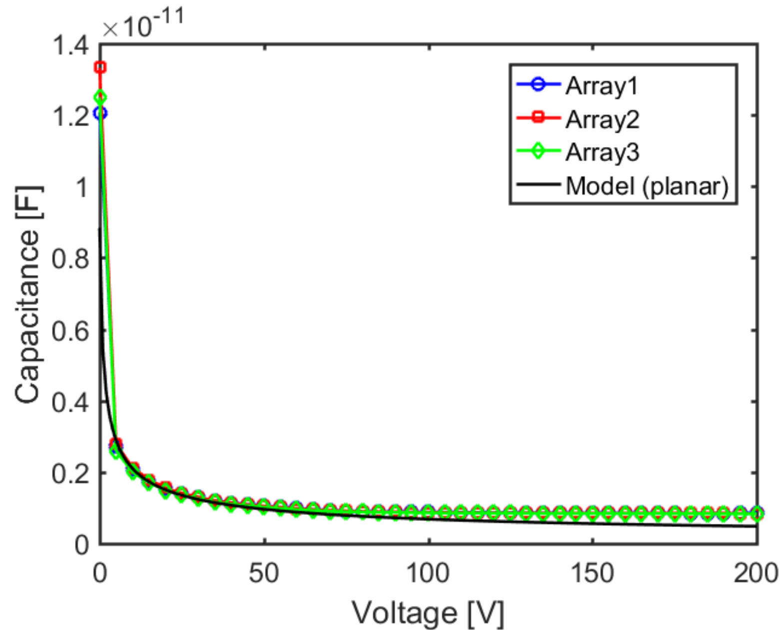
We kindly acknowledge the SEED collaboration (INFN sections of Torino, Padova, Perugia, Frascati) for the support and the following funding agencie:

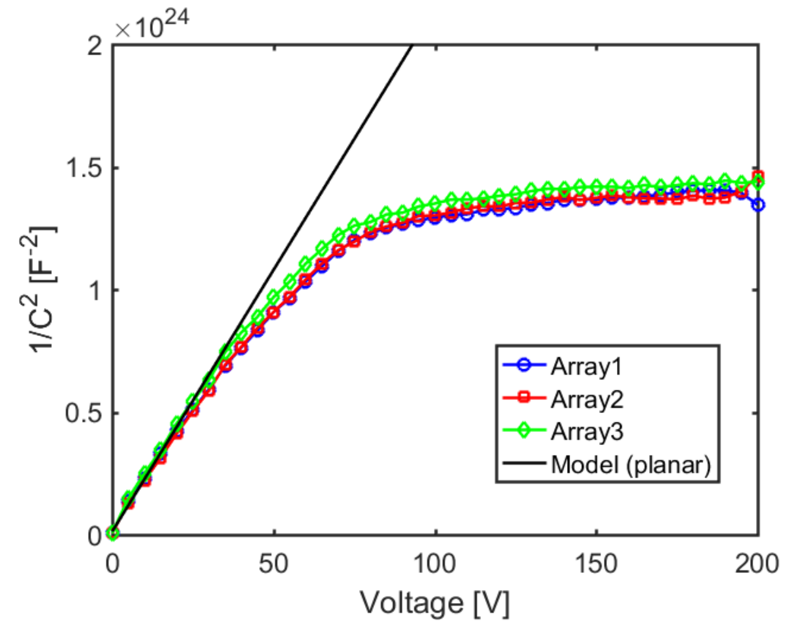
- INFN – R&D committee 5

Thank you for your attention

Backup slides

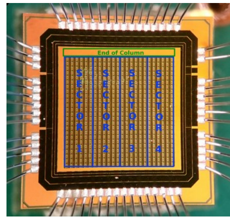
Test matrices: CV curves



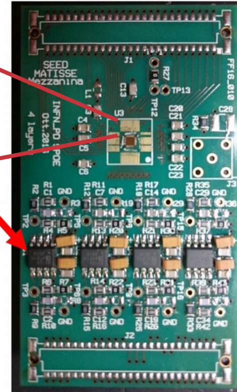


- The C-V characteristic guarantees the full depletion for voltages around 150 V but the trend does not highlight the voltage value when this happens due to the effect of the guard rings at low voltages.

The DAQ system



Buffers (x8)

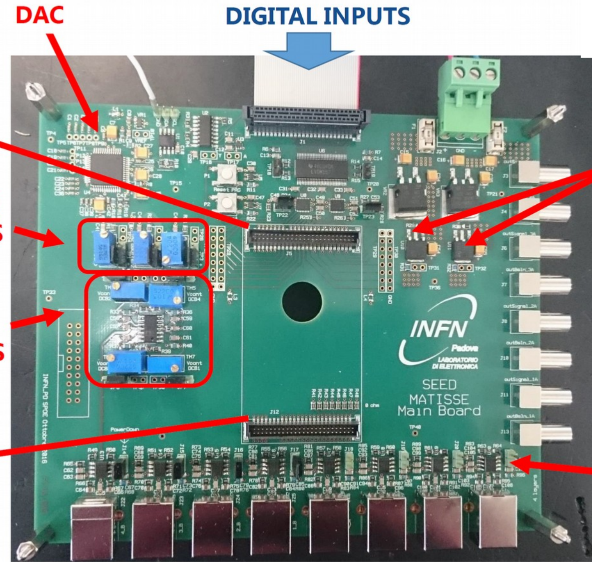


DAC

DIGITAL INPUTS

TRIMMER FOR I BIAS

TRIMMER FOR V BIAS



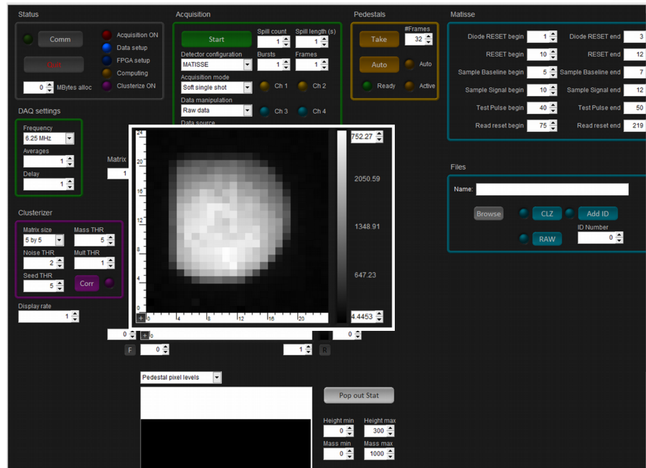
LDOs 1.2V

SINGLE ENDED ANALOG OUTPUTS

Differential buffers (x8)

DIFFERENTIAL OUTPUTS

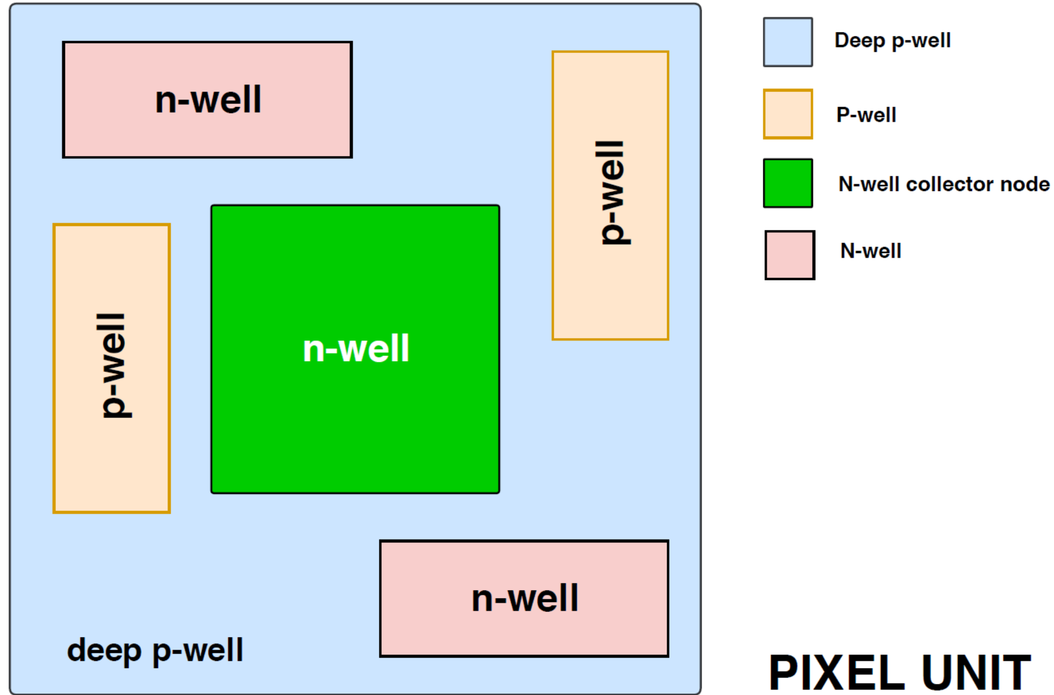
Software



DAQ box

The **DAQ box** box is based on a commercial FPGA and a custom analog board with 5 independent channels each with a 100 MS/s 14 bit Analog to Digital Converter (ADC).

The pixel cell



PIXEL UNIT

Power consumption

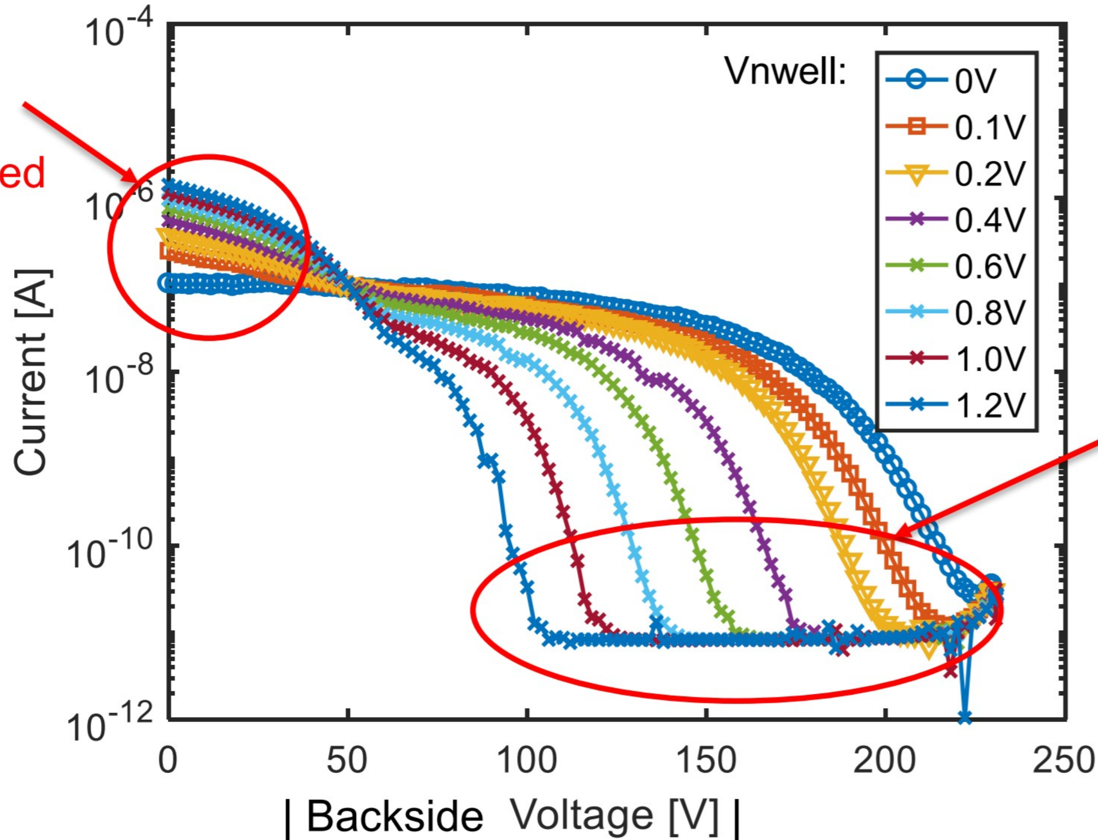
INFN TORINO

SYSTEM	SUPPLY [V]	MEASURED [mW]
motherboard	± 5	2000
motherboard	1.2	0.54
ASIC (static)	1.2	3.84
ASIC (transmission)	1.2	13.2
Channel (static)	1.2	6×10^{-3}

Leakage

INFN TORINO

Current between guard ring and pixels in undepleted sensor



Depleted sensor: pixels isolated from guard ring