# Development of MAPs frontend for the ILC tracking detectors

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**IPHC-IN2P3-CNRS /Université de Strasbourg**

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***FRONT-END ELECTRONICS***
***FOR PARTICLE PHYSICS, PHOTON SCIENCE AND RELATED APPLICATIONS***

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# Contents

- Requirements, motivations
- Amplifier schematics and simulations
- Tests and results
- Summary and future plans

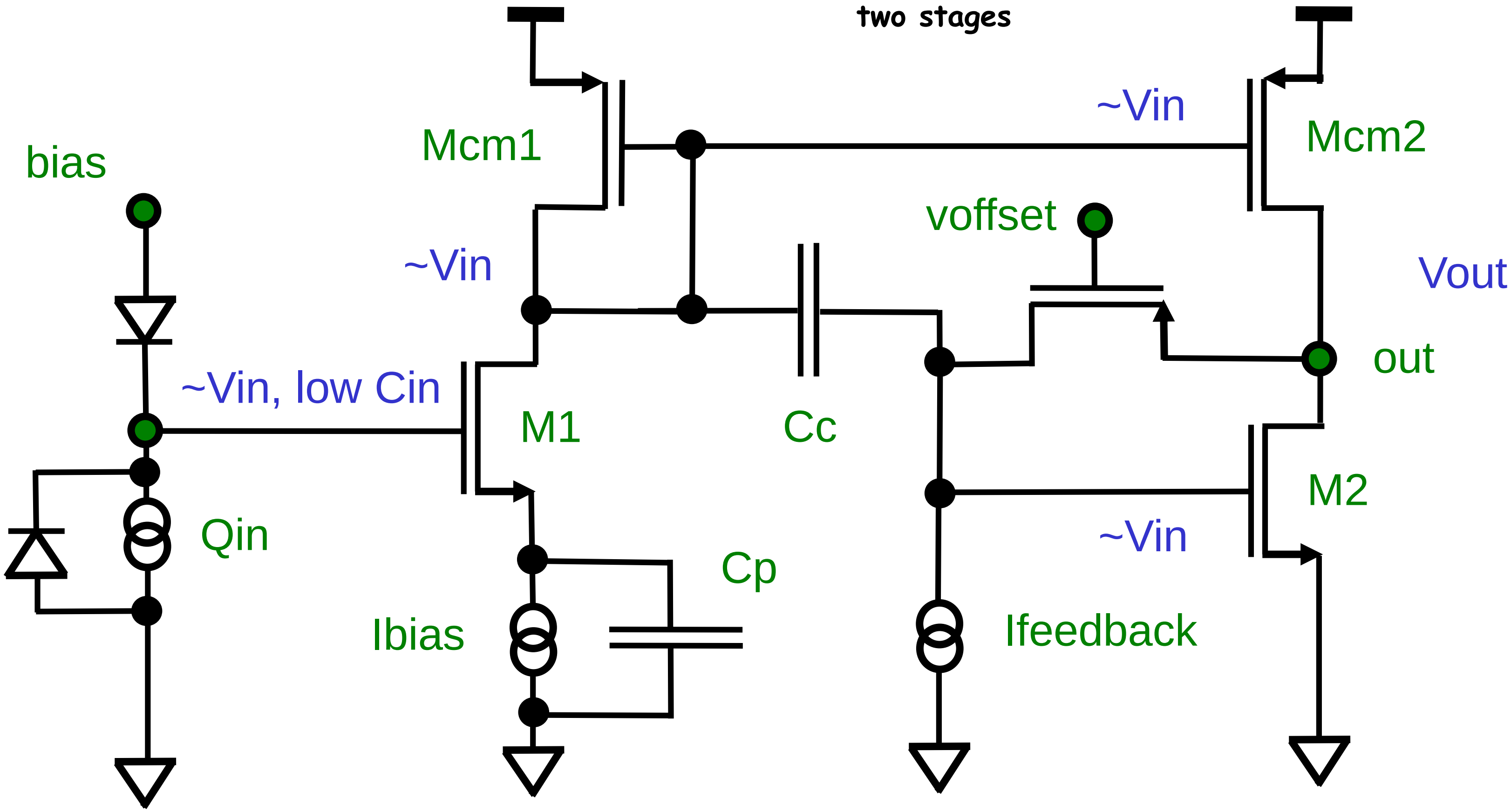
# Requirements for ILC vertex detector and analogue front-end circuit requirements

1. $\sigma_{sp}$< ~3 μm --> 22 $\mu m^2$ pixel
   - digital part is a fraction >0.5 of this area, less room for the analogue part
2. < 1-2-4 μs readout time (depending on layer)
   - particle response pulse duration less than then the readout time
   - time walk at least < 500 ns (bunch crossing time) or ideally <50ns for the full range
3. ~ 100 $mW/cm^2$ = 1 $nW/\mu m^2$ (< 500 nW/pixel )
   - only small fraction < 100 nW/pixel of is dedicated to analogue front end

**Motivations for R&D: small power consumption (<100nW) and small pulse duration (<3us) is possible to reach with amplifier used in Alice and currently implemented in MIMOSIS chip for CBM, however can we still reduce power and response time by few times (not by optimisation by design parameters)?**

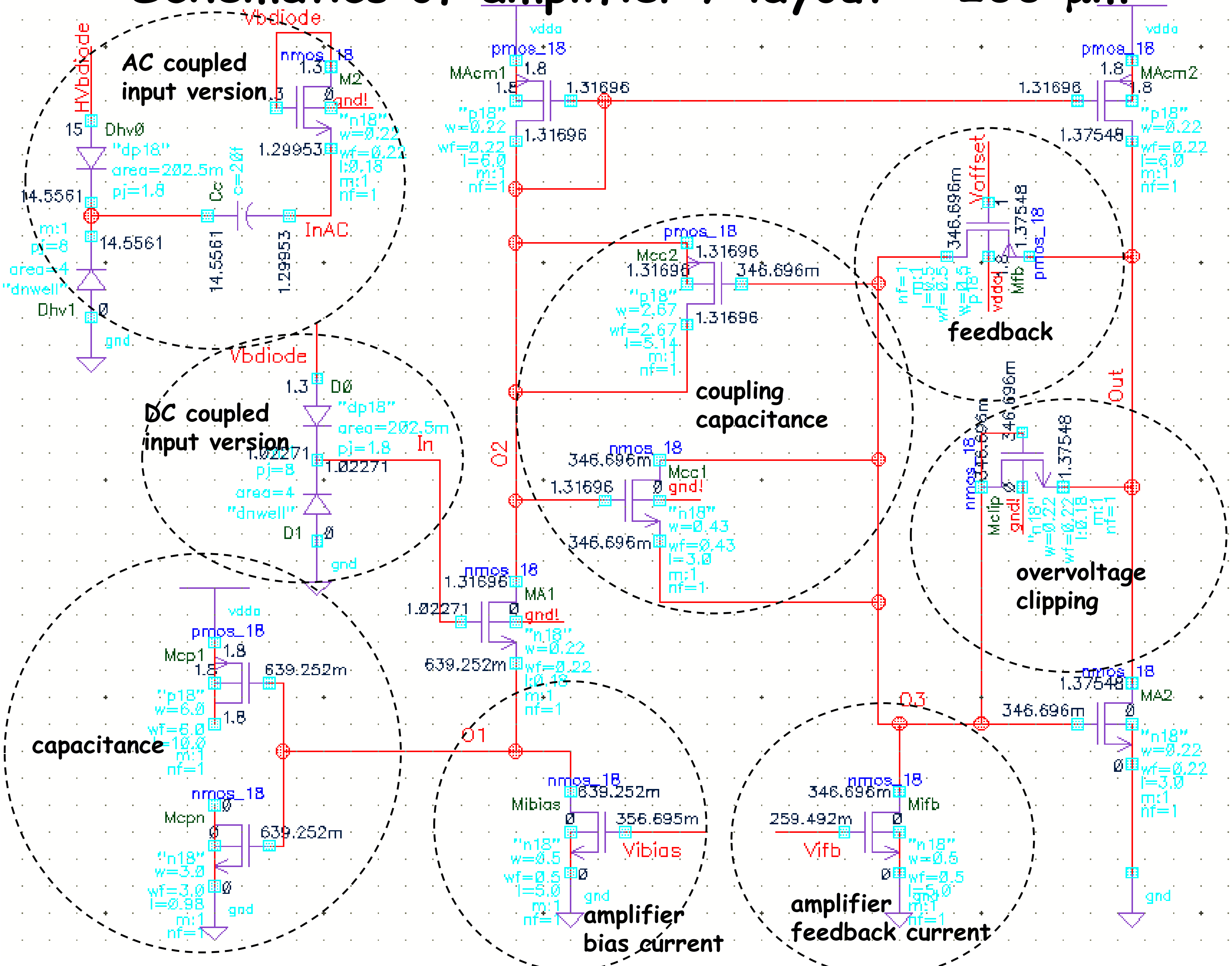
# Schematics of amplifier

two stages



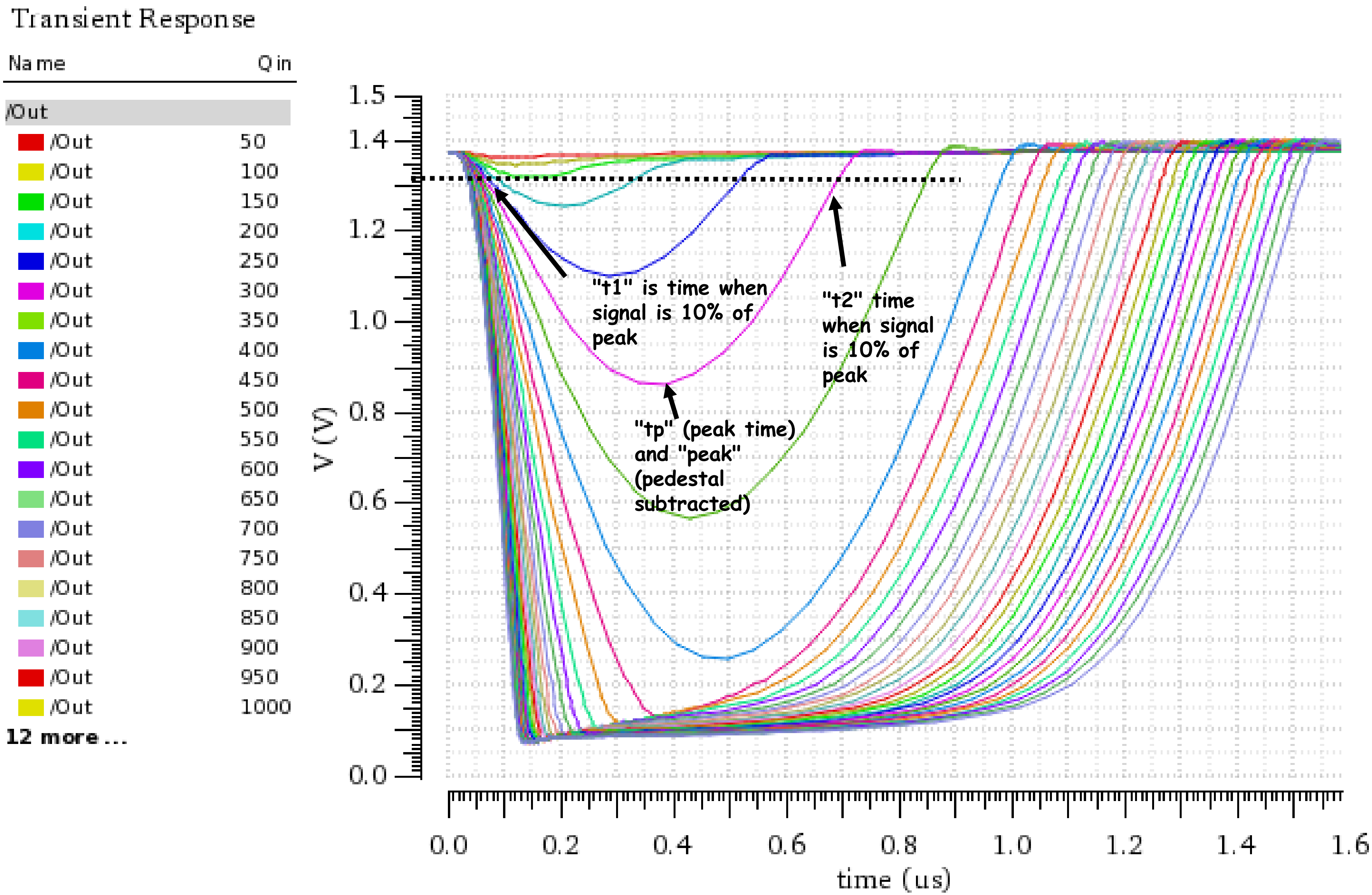

second stage similar feedback principle as in Alpide amplifier, but larger voltage swing and output offset control range

# Schematics of amplifier / layout ~ 200 μm²



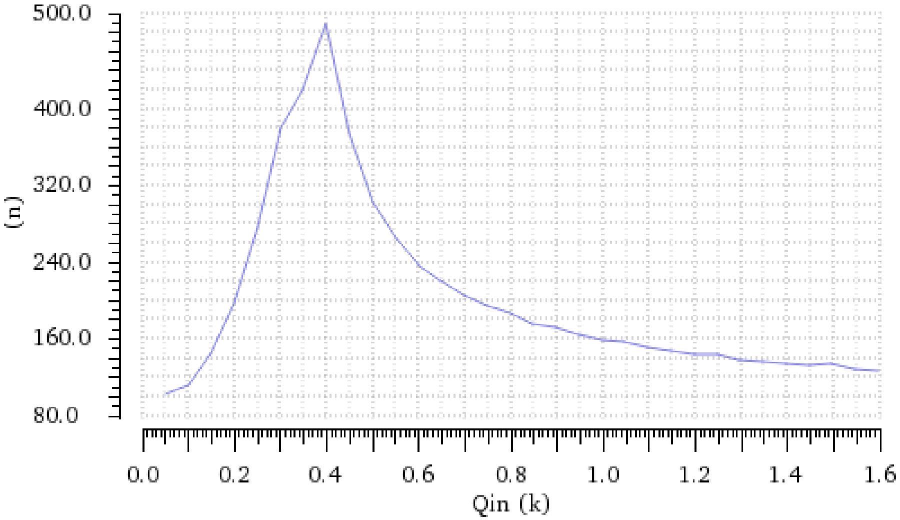
# Simulations

**output waveform for 50 to 1600 electrons input charge with step of 50e**
**total bias current 48 nA, feedback current 2.25 nA**

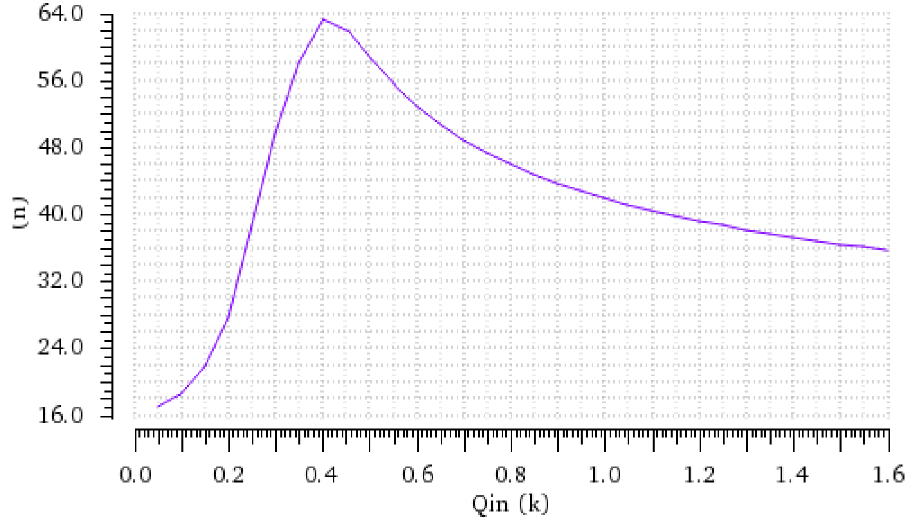


# Simulations

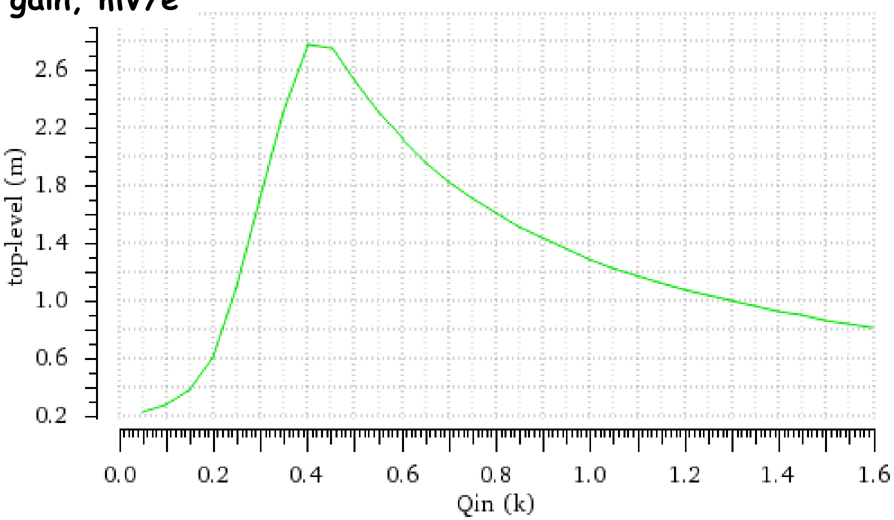
t peak , ns



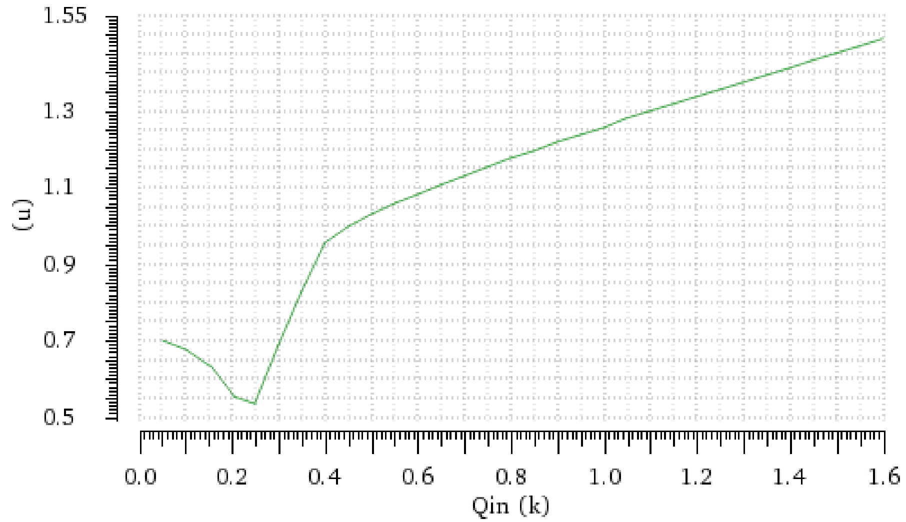

t1, ns




gain, mV/e

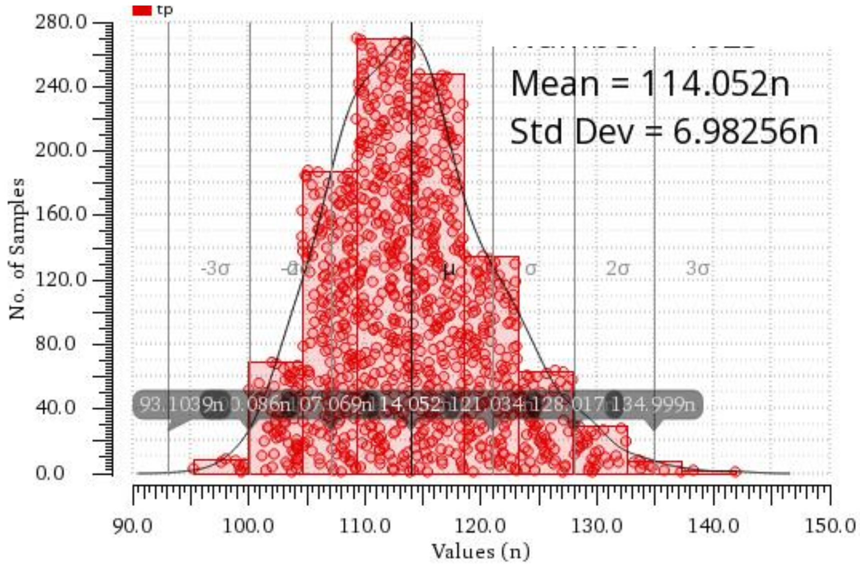



t2, ns

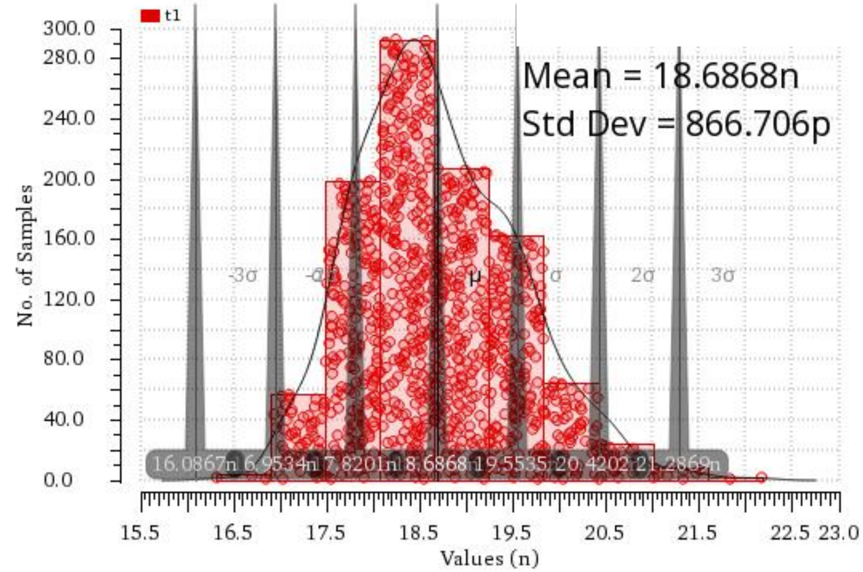


# Simulations mismatch parameters, Q=100e

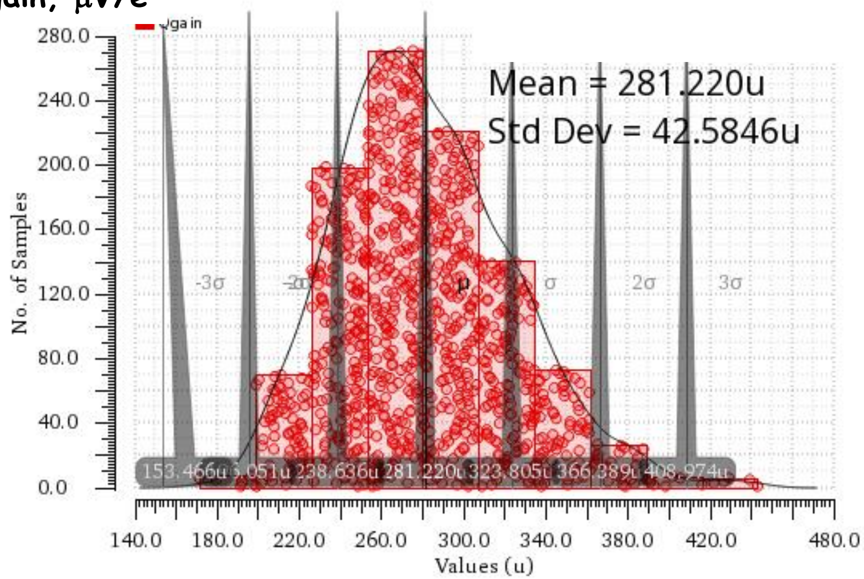
**t peak, ns**



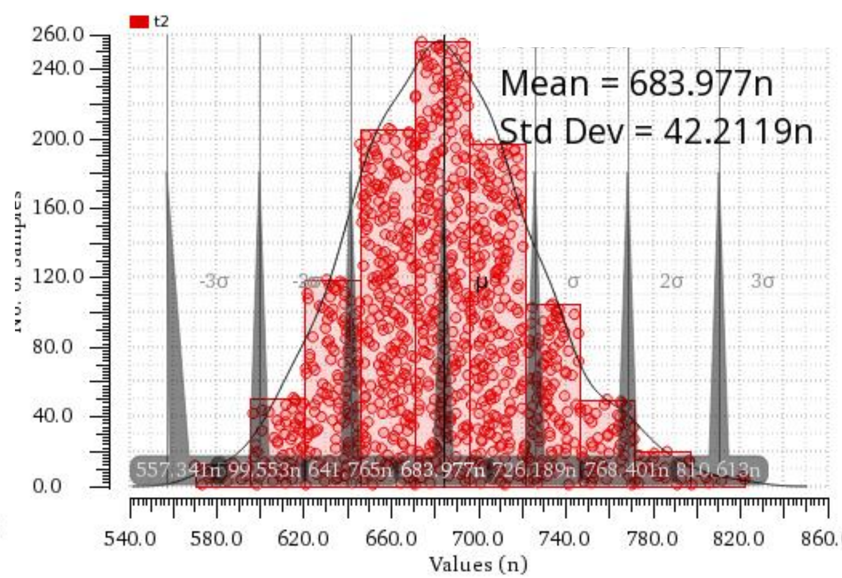

**t1, ns**




**gain, μV/e**

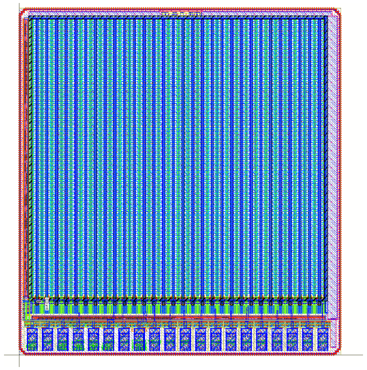



**t2, ns**



# Test chip and measurements

• matrix of amplifies has been implemented in a small size 2x2 mm chip in 0.18 μ technology (EPI HR 18 μm), amplifier area < 200 $\mu m^2$

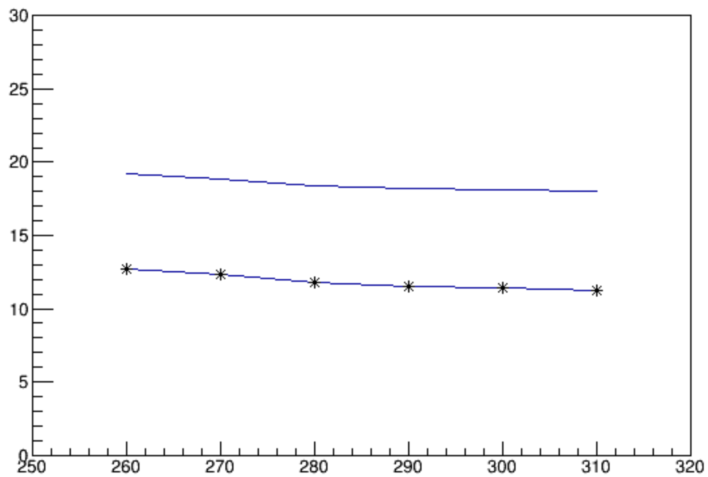


• multiplex buffered (source follower) output of each amplifier to one analog output and record waveforms from injected charge

• there are two versions with same amplifier and different charge sensing diode connections: DC coupled and AC coupled, the AC coupled allows for a bias voltage up to 40 V

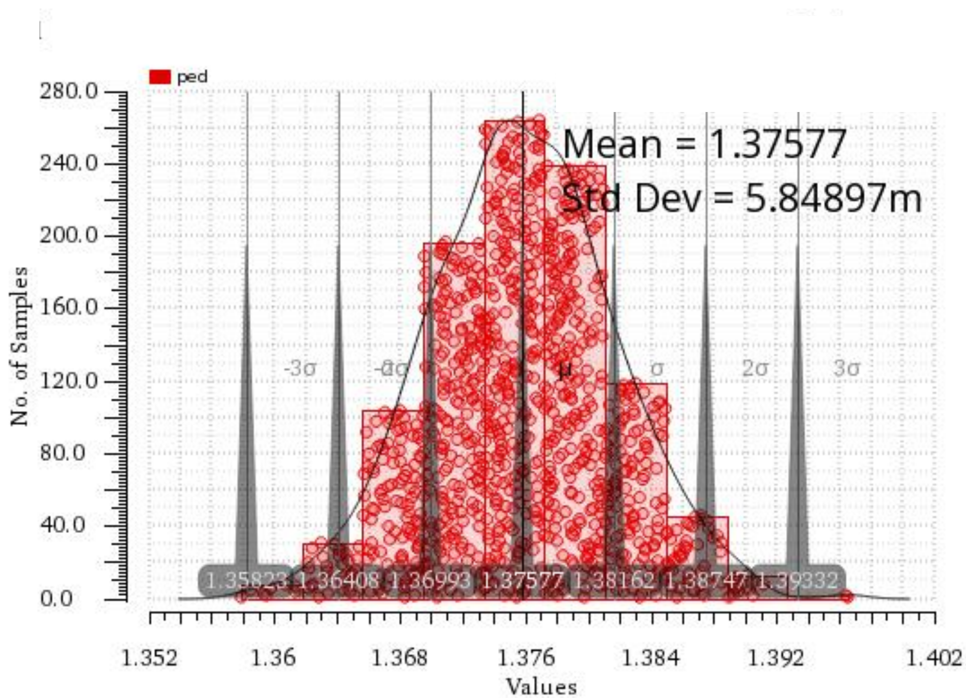
# Measurements

Pedestal dispersion (mV) for 48nA bias current as a function of feedback voltage, before and after correction (*) spread of source followers removed



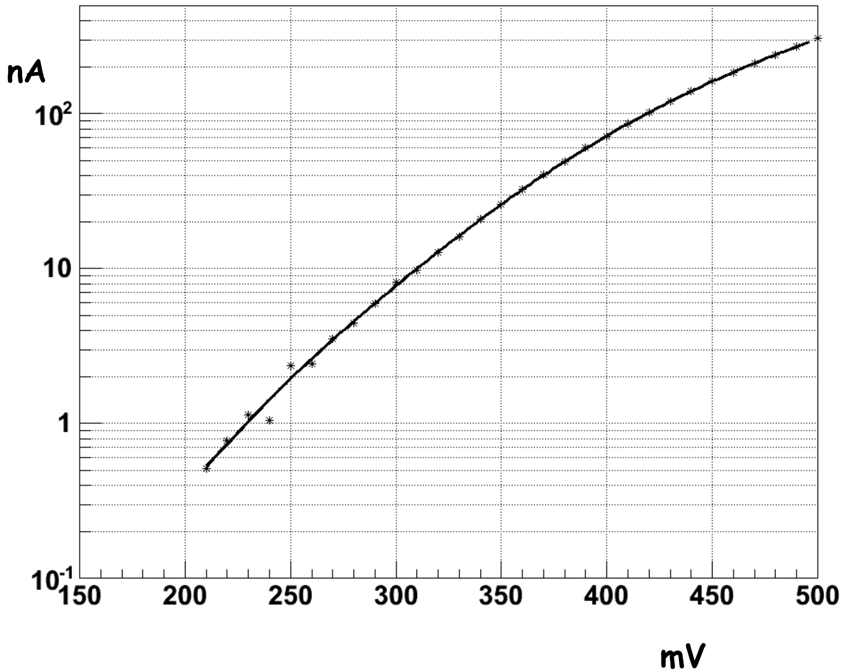

pedestal dispersion two times larger than in simulation, but still OK

Simulations mismatch



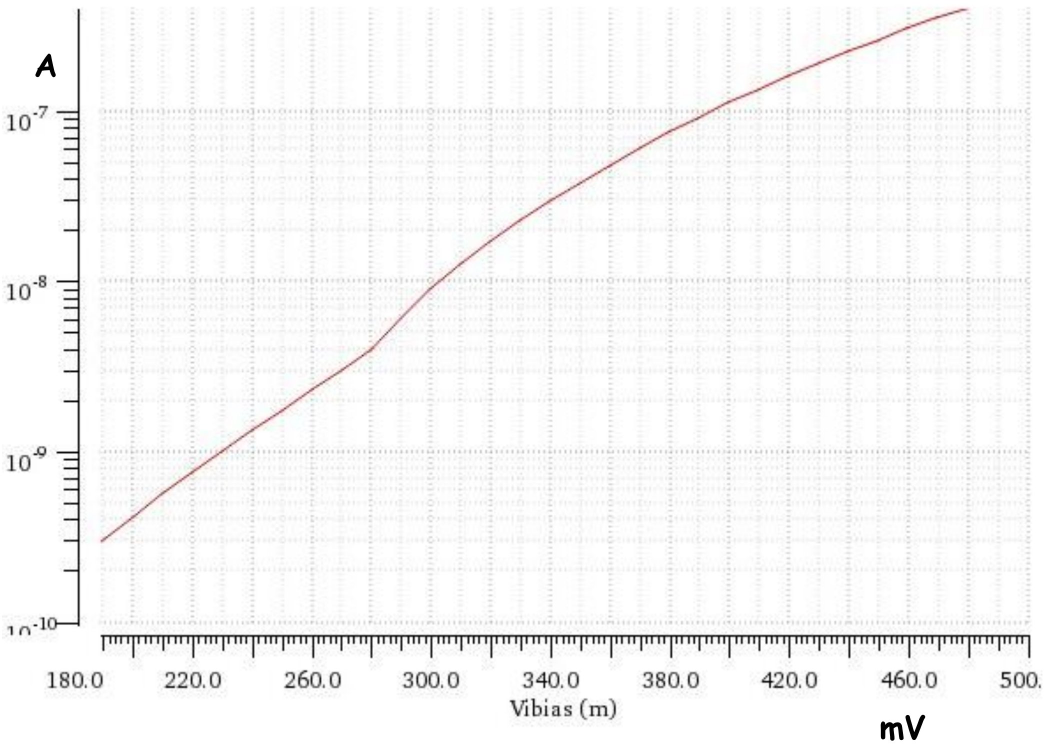
# Measurements

Bias current (total) as a function of bias voltage




good agreement with simulations (<50% discrepancy)

Simulations of total bias current





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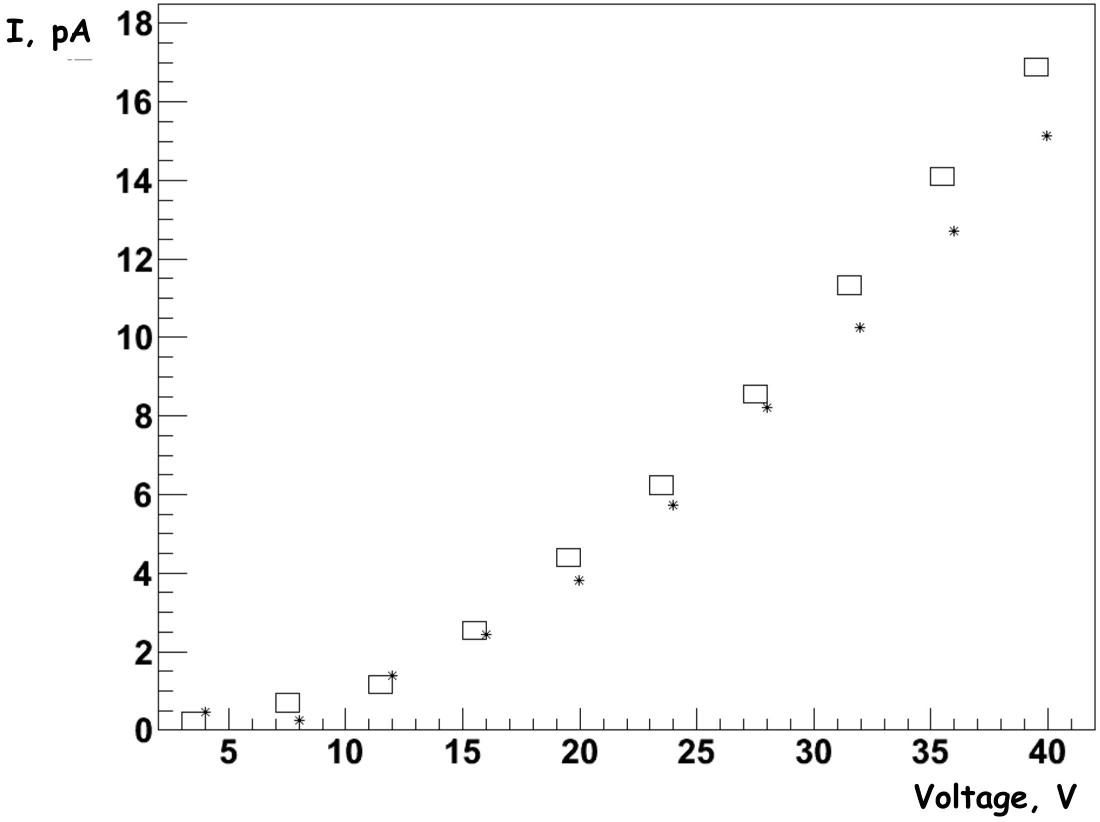
# Measurements of leakage current for AC coupled pixels

**I leakage , averaged (over 1792 pixels) per diode for two chips (squares and stars)**

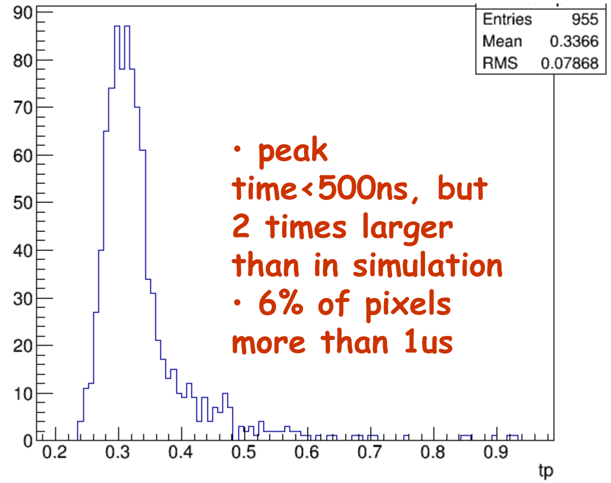


# Waveform measurement/analysis procedure

- charge is injected by pulse via coupling capacitance
- ~500 waveforms recorded from each amplifier (of 1023)
- peak, gain, peak position, t1 and t2 are extracted for each amplifier
- then pixel-to-pixel variation of extracted parameters is evaluated for a fixed amplifier bias voltage but for different feedback bias voltage

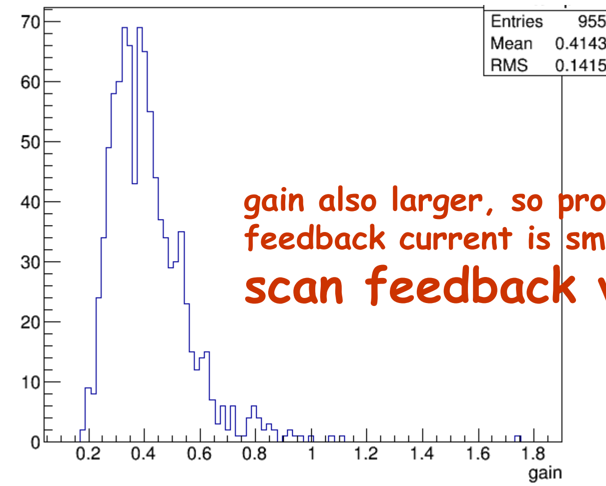
# Measurements, Ibias=48nA, Qin=100e
# Vfeedback=280mV~>2.25nA

peak time, µs




• peak time<500ns, but 2 times larger than in simulation
• 6% of pixels more than 1us

gain, mV/e

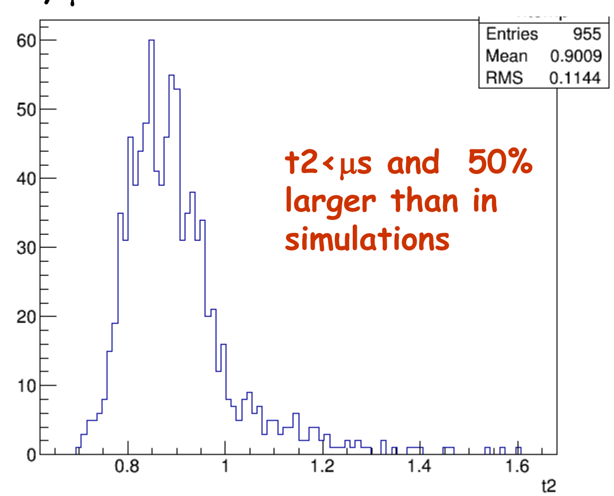



gain also larger, so probably feedback current is smaller ->

**scan feedback voltage**

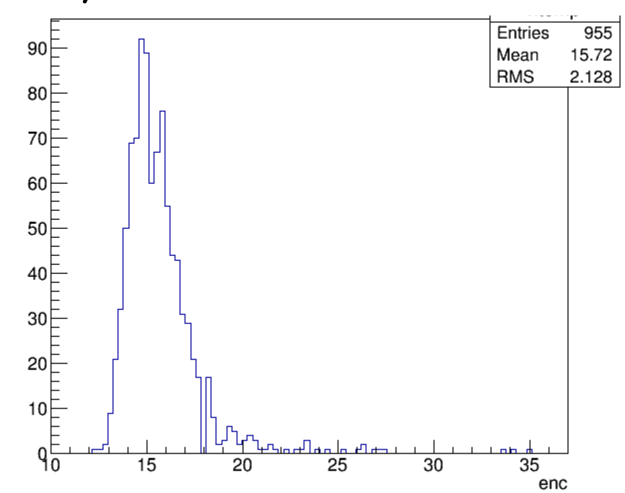
variation is much larger(~10times) than in MC simulations, but variation of parasitic capacitance was not taken into account

t2, µs

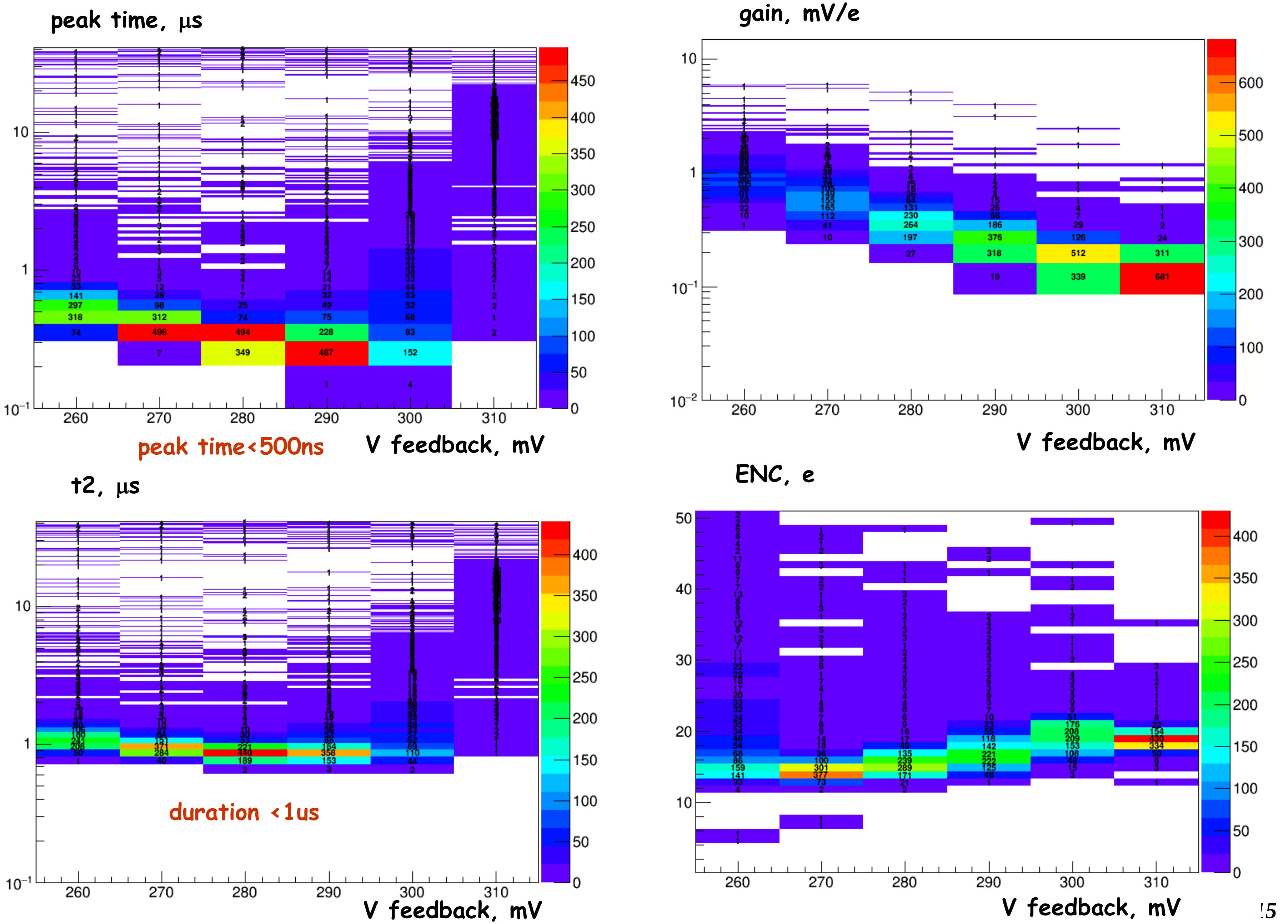



t2<µs and 50% larger than in simulations

ENC, e

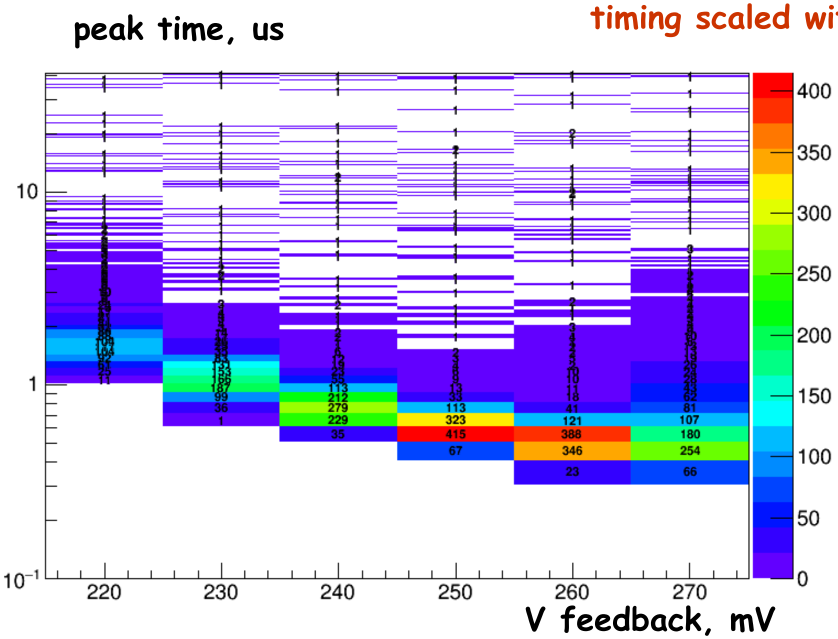


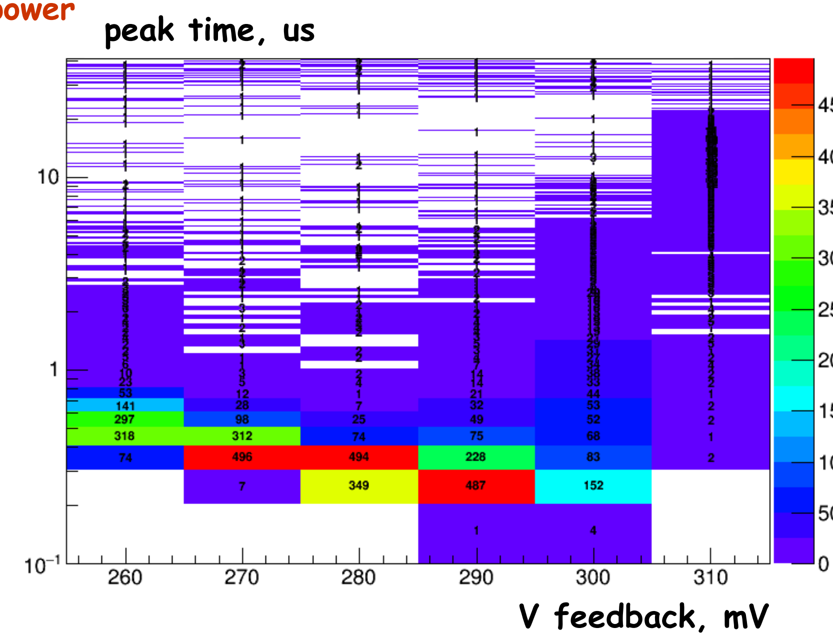
# Measurements, Ibias=48nA, Qin=100e

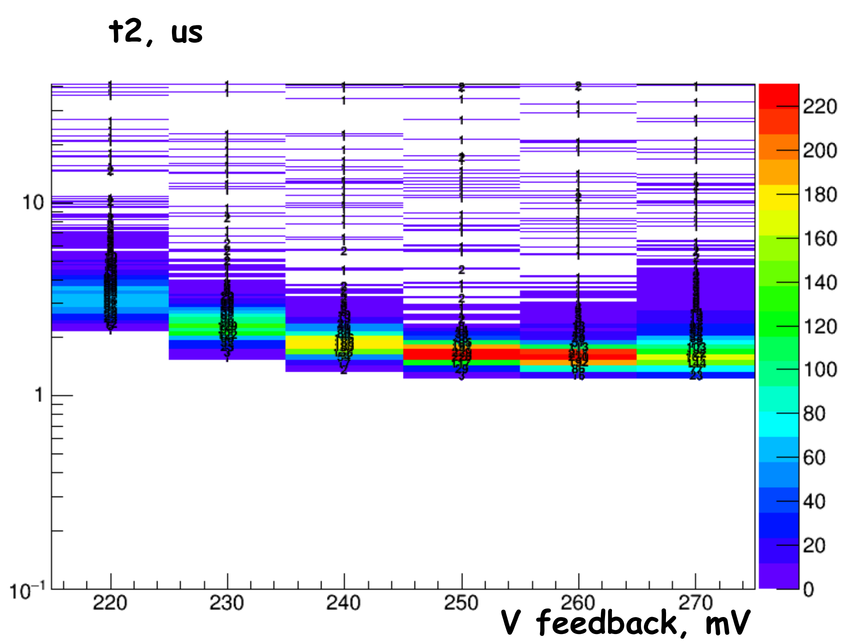


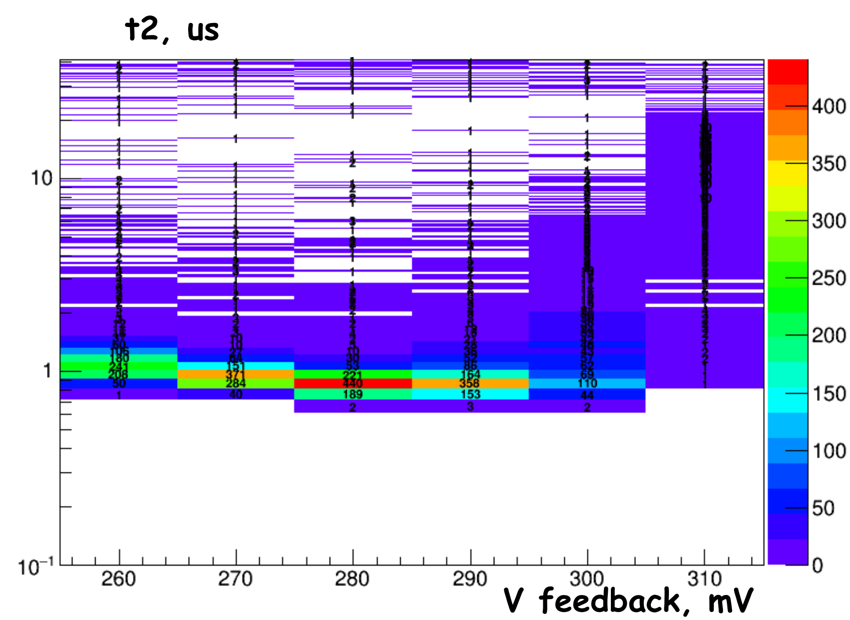
# Measurements, Qin=100e Ibias=20nA(left)/48nA(right)

timing scaled with power

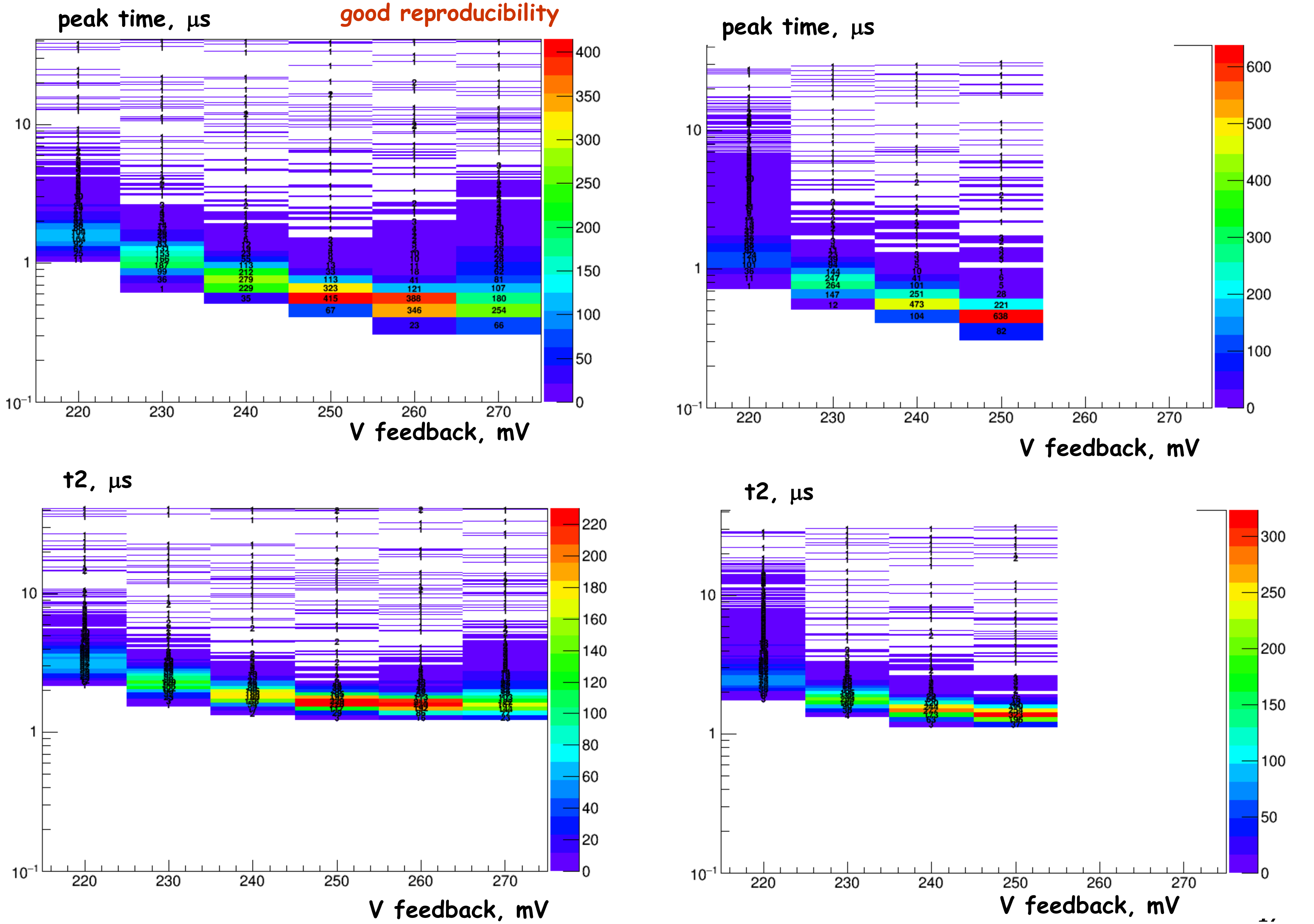


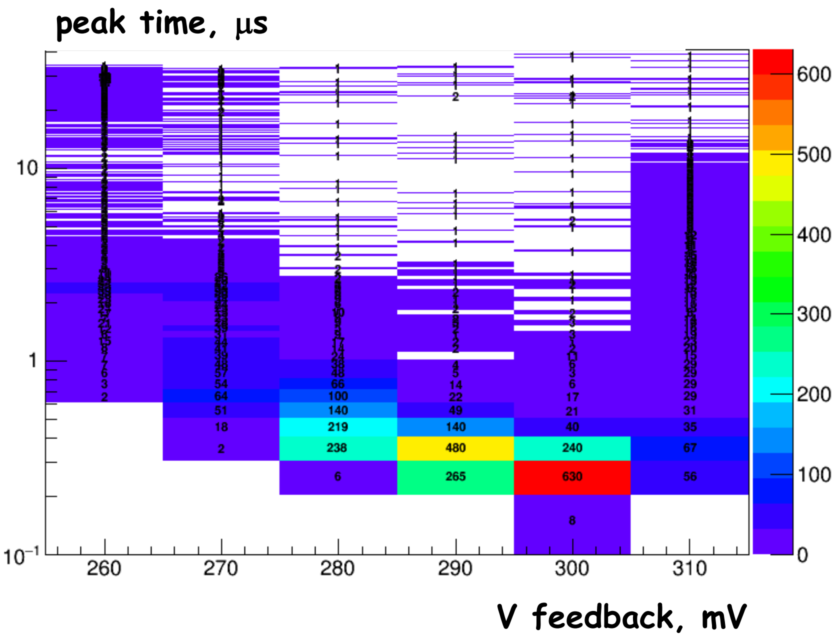



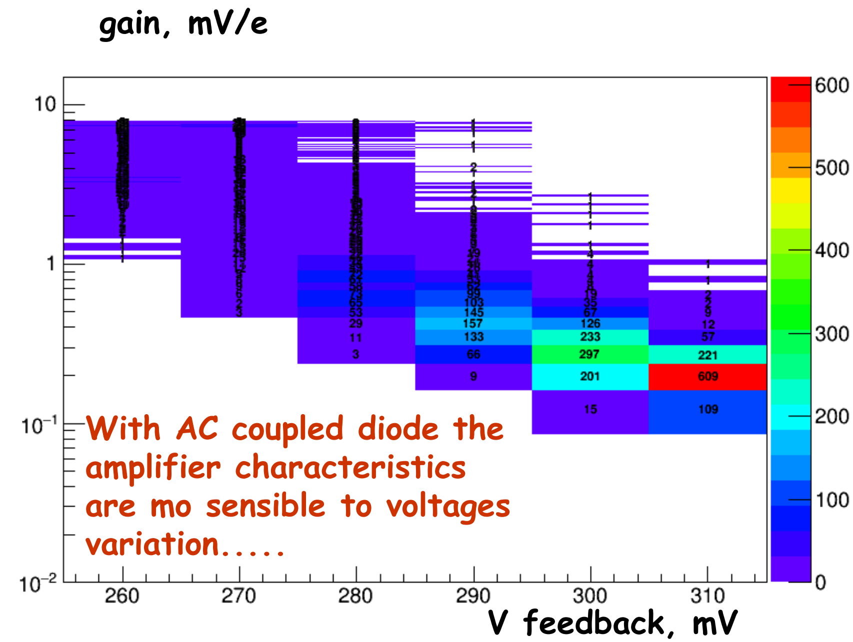



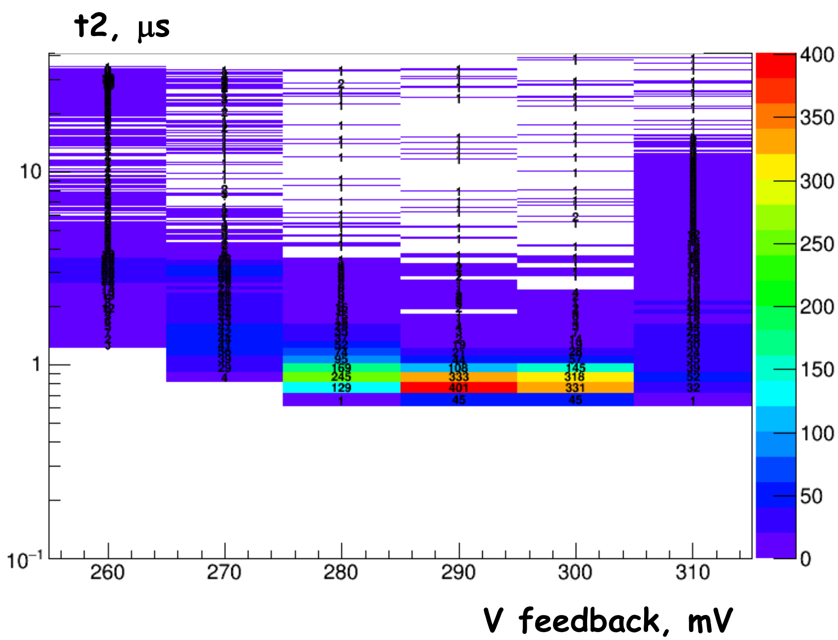
# Measurements, Ibias=20nA,Qin=100e, chip1(left)/chip2(right)

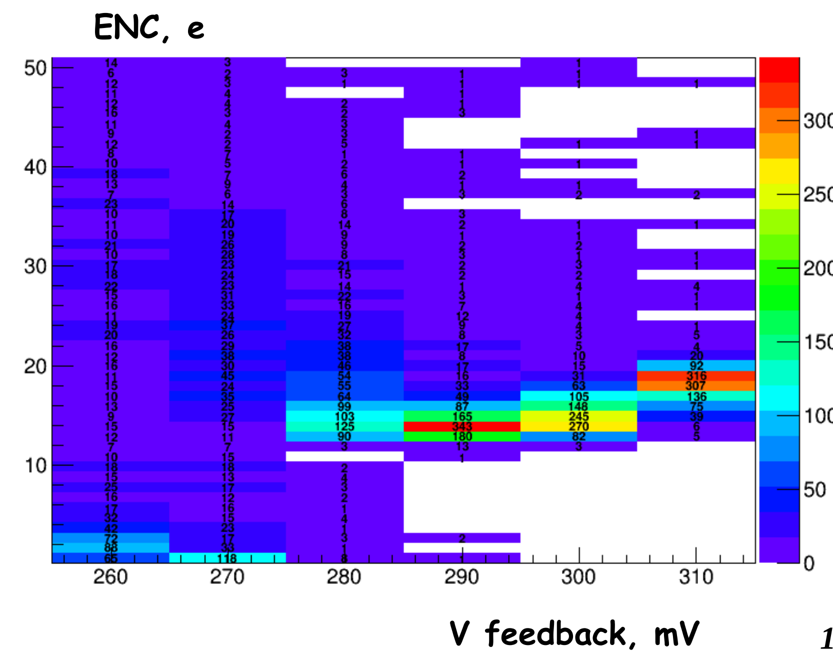


# Measurements, Ibias=48nA, Qin=100e, AC version



# Conclusions and future plans

1. new version of amplifier for MAPS has been designed and tested:
   - it shows that one can fulfill ILC requirements, power<100nA & time walk < 500ns, pulse duration <1$\mu$s
   - larger dispersion of parameters than simulated
   - RTS noise observed
   - AC coupled diode version working, but more sensitive to bias voltages
2. optimizations are in progress
3. irradiation tests are in progress

**Thank you for your attention !**