Data Readout Strategies for pixel detectors

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GOAL

- Classify the readout strategies currently being used in pixel detectors
- Identify pros and cons of these approaches
- Analyze point of failure in each scheme

Pixel Detectors Readout

ANALOG

- Lower speed
- In-pixel storage for fast systems (e.g. high speed burst mode imagers): Lengthy deadtime
- kT/C noise from sampling and transferring data
- Not high enough dynamic range (8-10 bit max) @ 20MHz
- Rolling shutter or global shutter type of readout

DIGITAL

- Higher speed (at least 10x faster than analog)
- Requires analog-to-digital conversion (e.g. ADC per pixel or counting instead of integrating)
- Insensitive to noise as transfer off-chip is digital
- Can use busses and send parallel data to improve speed

Pixel Detectors Readout

FULL FRAME

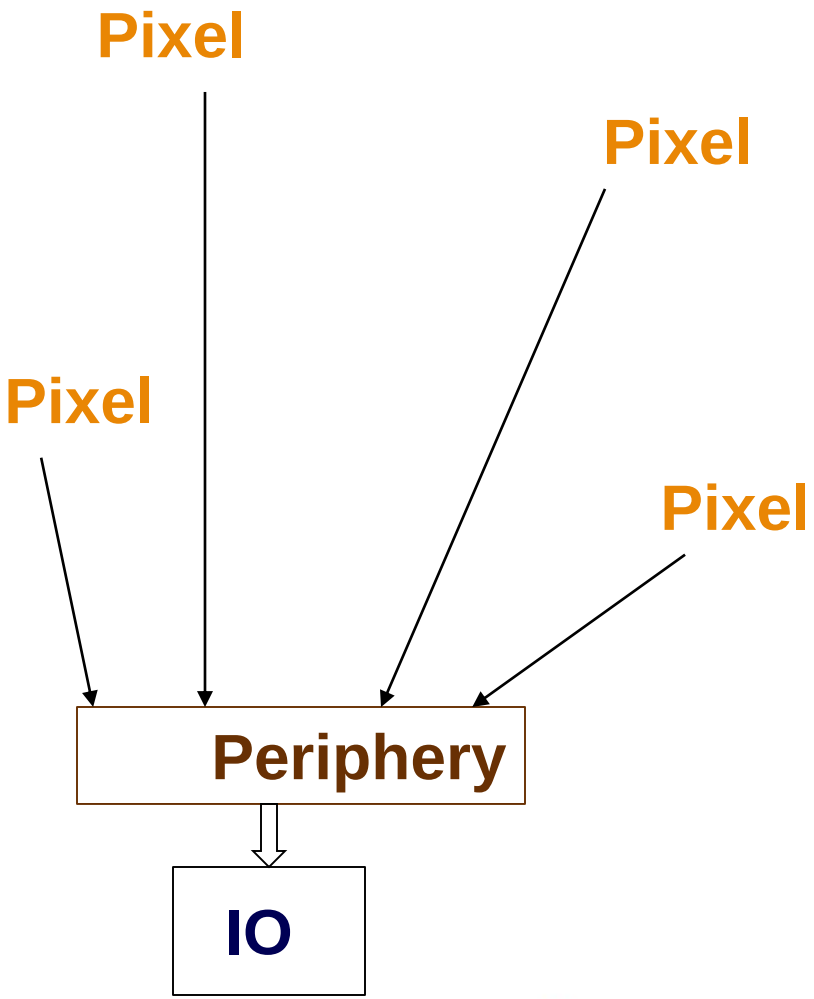
- Data from all pixels need to be readout
- Constant time to readout
- Dependent on the size of the frame, multiple parallel paths can increase speed

ZERO SUPPRESSION

- Low occupancy applications
- Overhead: Address (e.g. 5 bit data + 12bit address)
- Variable no. of pixels to be readout in each time frame
- Can lead to loss of data if time frame is too short

Pixels connected directly to periphery

- All pixels independent to communicate to the Periphery
- No single point of failure (if link is broken only 1 pixel is effected)
- Every pixel always has access
- Periphery is intelligent, acts as a central reservoir and can manage data from all pixels
- Cannot be sustained for large arrays of pixels
- Can expand to a limit by increasing the no. of peripheral units and multiple IO's

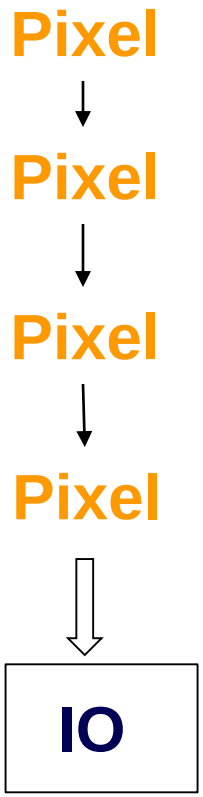


How to expand for larger systems?

- **Distribute periphery across the ROIC**
- **Share a common bus for data transfer**

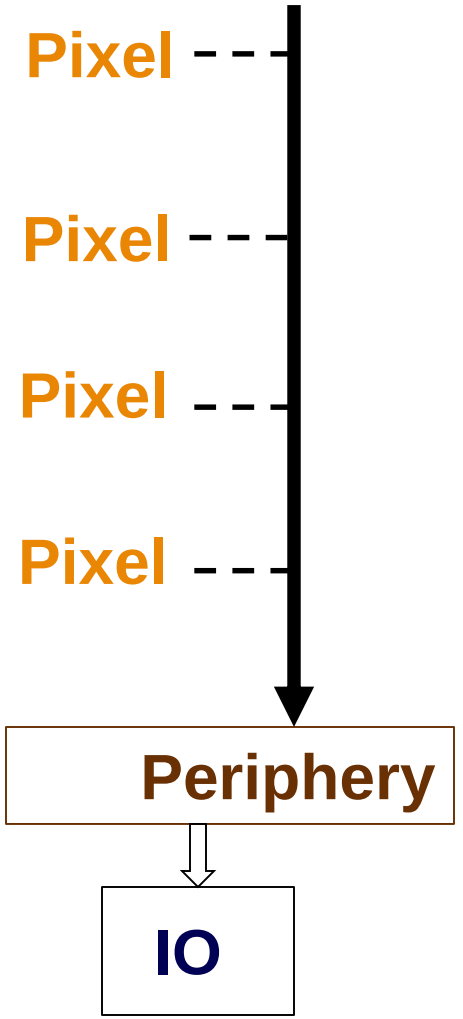
Shift Register – Distributed Periphery within a Pixel

- Daisy chaining of data from one pixel to next (only allowed to communicate with nearest neighbor)
- Two sets of registers for deadtimeless operation
- When one is collecting data the other is transmitting
- PROS
  - Simple
- CONS
  - Single point of failure exists (if one register connected incorrectly or damaged, data transfer can be interrupted)
  - Power consumption; all registers in all pixels are continuously switching



Pixels connected directly to periphery: Sharing a bus

- All pixels communicate to the Periphery via a shared bus
- Periphery is intelligent, gives access to a pixel to transfer data
- Several schemes available to access bus



KEY TERMS:

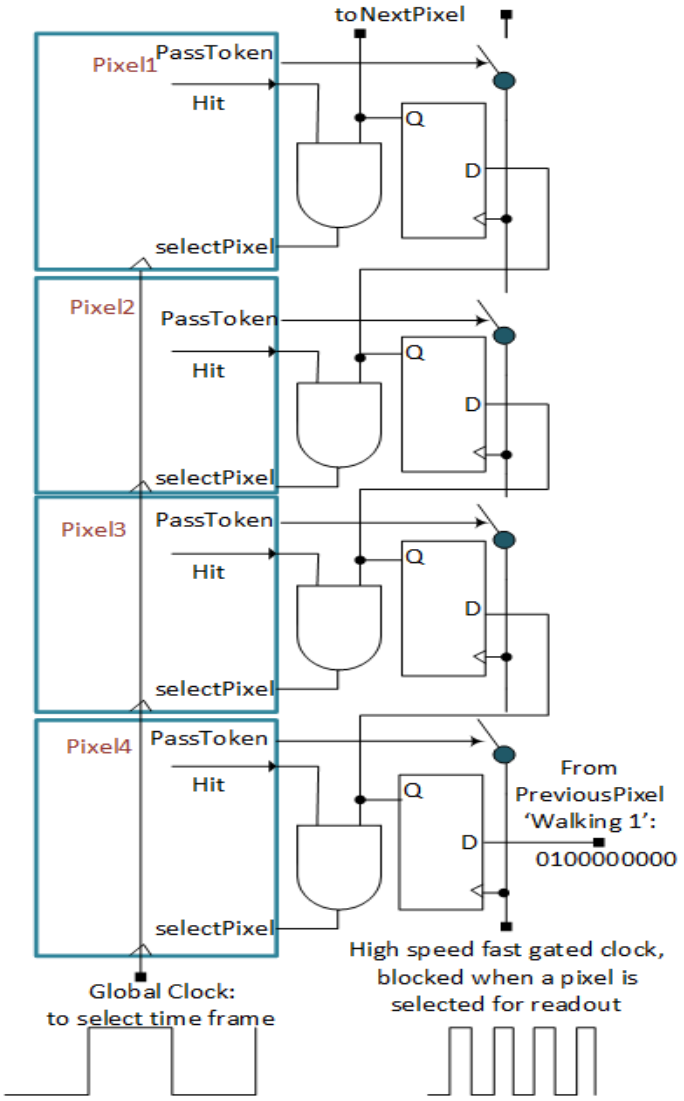
Request – pixel has data to be readout

Acknowledge - Select pixel for readout (access to bus)

Strobe – De-selects the pixel (releases access to bus)

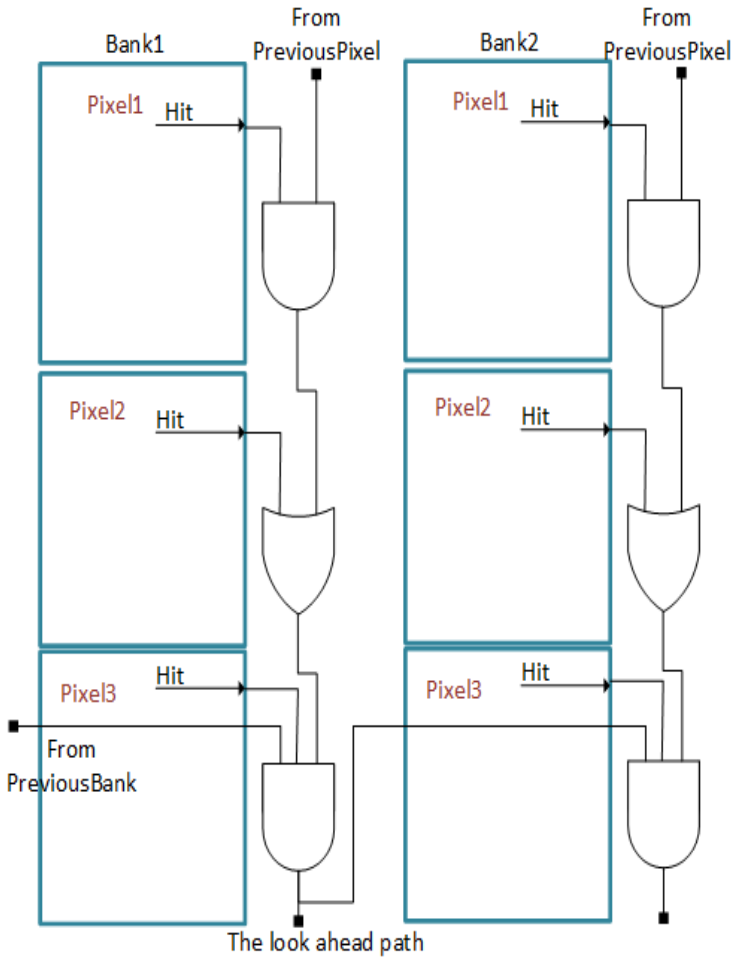
Token Passing

- First pixel that grabs the token can pass its data
- Uses a shared bus
- Once the pixel has finished then the token goes to the next pixel
- CONS
  - Limited by the time it takes the token to circle through a given bank of pixels
  - Single point of failure: Failure by a pixel to release the token (highly unlikely)
  - Mechanism for releasing a token either per pixel or utilize a strobe signal



Fast look ahead logic

- To make the Token passing scheme faster
- Arrays of pixels can be subdivided into smaller group
- Alternate bank of NAND and NOR to ripple a priority through the chain
- Effectively creates several parallel paths the token can take



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Bus Arbitration schemes – other implementation

- Trigger matching implemented in early ATLAS designs
- SuZe – Suppressed Zero
- Some form of end of column Token passing

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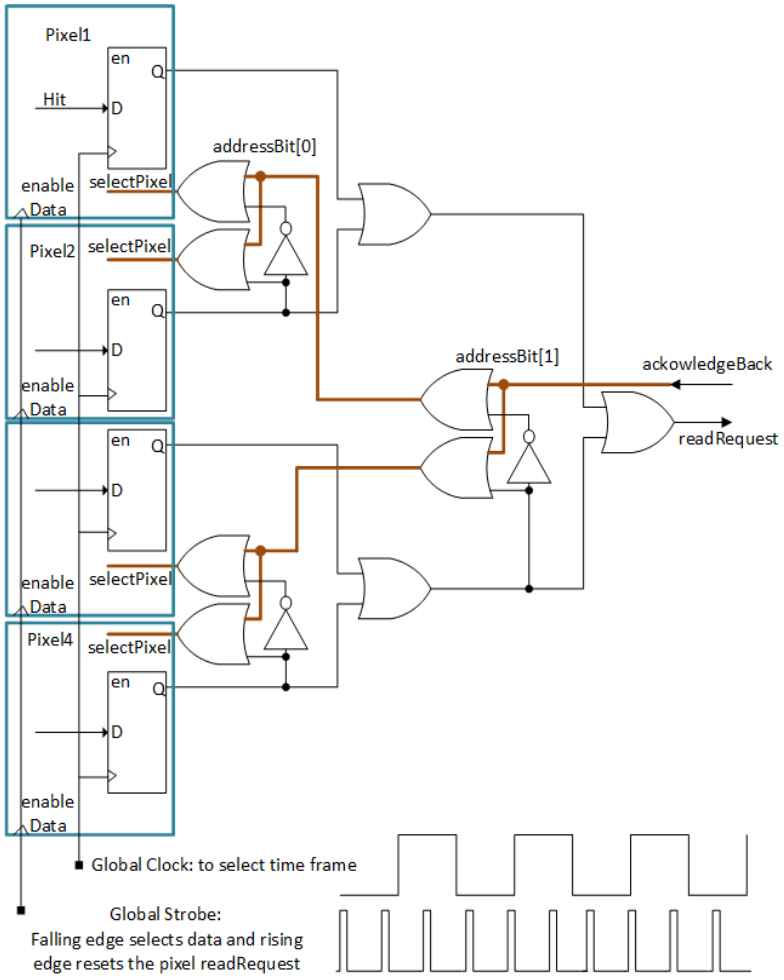
- J.J. Jaeger, C. Boutonnet, P. Delpierre, J. Waisbard, and F.Plisson,"A Sparse Data Scan Circuit for Pixel Detector Readout",IEEE Nucl. Sci., VOL.41, NO. 3, JUNE 1994.
- I. Peric, L. Blanquart, G. Comes, P. Denes, K. Einsweiler, P. Fischer, E. Man- delli, and G. Meddeler. The FEI3 readout chip for the ATLAS pixel detector. Nuclear Instruments and Methods in Physics Research, 565:178–187, 2006.

Priority encoder: MEPHISTO

- Binary Tree
- Can select a pixel and automatically generate address
- Acknowledge signal used to select a pixel
- Strobe is used to deselect the pixel when data has been transferred
- CONS
  - Mismatch in timing between select and strobe signals- varies across pixels



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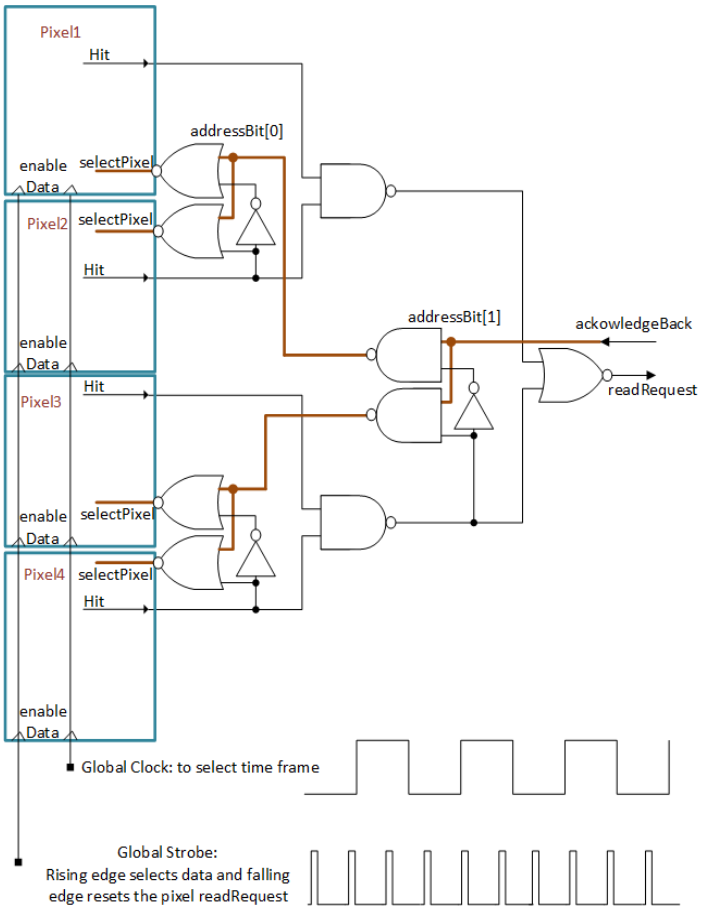
Priority Encoder: VIPIC

- MEPHISTO with least number of gates
- Almost like forward look ahead with 1 pixel per bank
- CONS
  - Requires a strobe signal to move to next pixel



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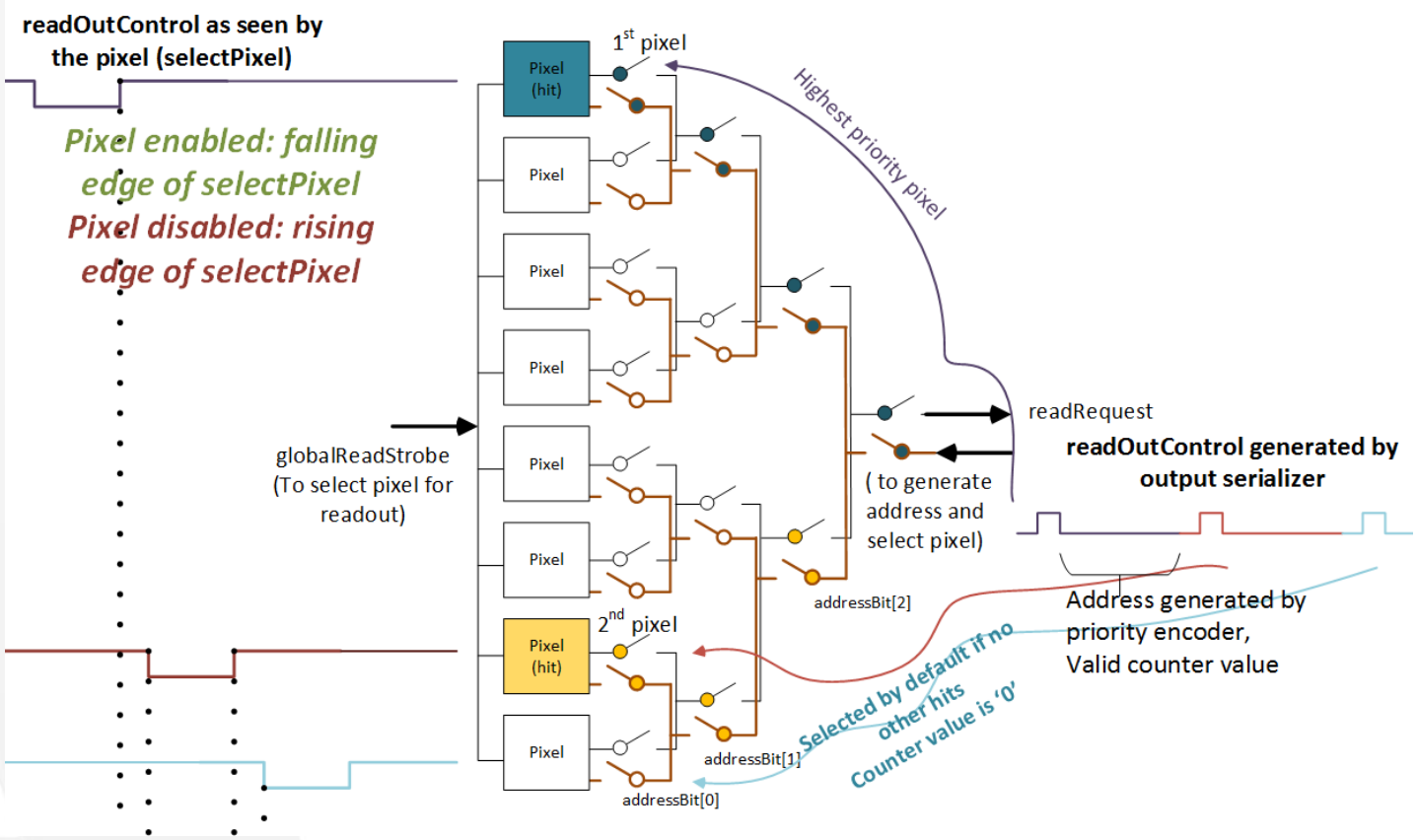
Strobeless Priority Encoder – VIPIC_L / FLORA



- No global strobe* signal – to reduce complexity in clock tree synthesis
- readOutControl generated by output serializer, uses the same path as the readRequest in the opposite direction to enable a pixel to use the shared bus
- Pixel with lowest priority is enabled when no valid data exists. Its counter value is '0', thus differentiating from an actual hit

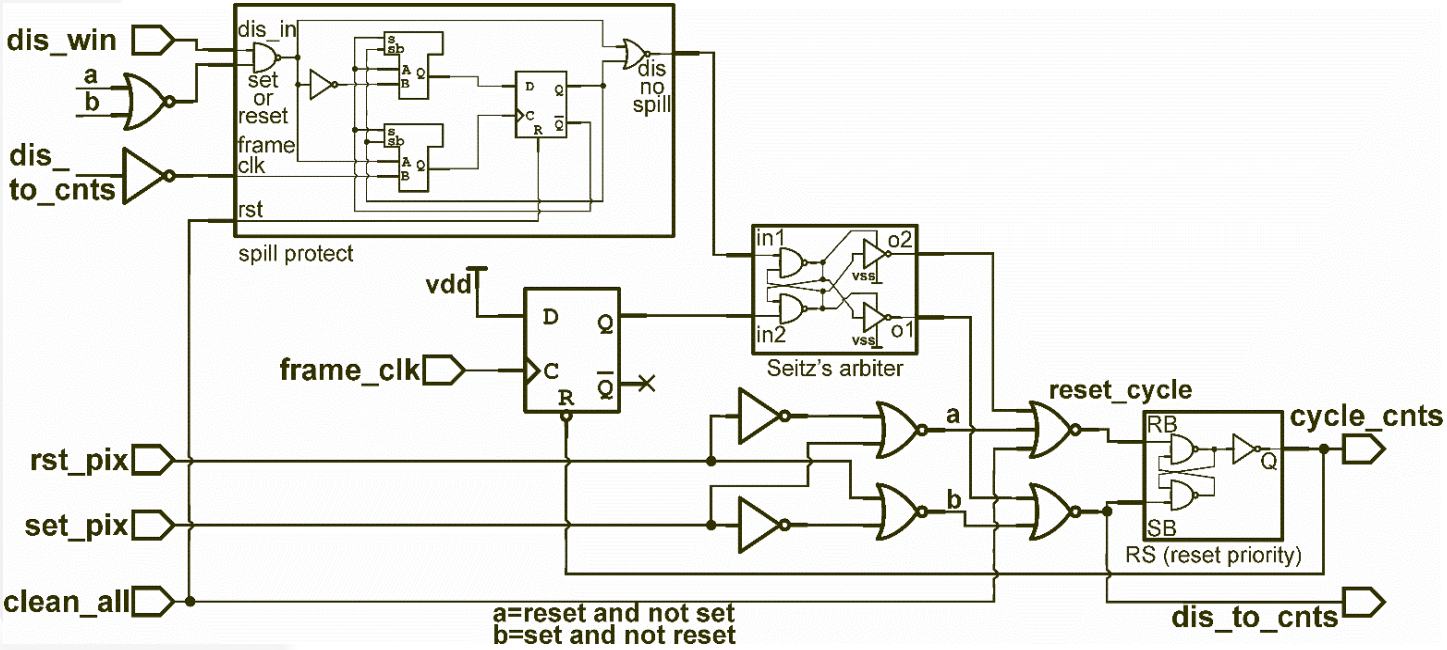
Fermilab

Power Consumption

Readout type	Power Consumption for speed of 400Mbps for 10bits of data per pixel for 1024 pixels	Total area per pixel for 10-bit storage register/shift register
Serial shift register	51.2 mW	211.7 μm^2
Strobeless priority encoder	0.634 mW	229.5 μm^2

Pixels with limited intelligence

- Should the hit be allocated to this frame or next – decided by an arbiter
- Deadtimeless without requiring 3 sets of registers (active during the short reset phase)
- Asynchronous logic to avoid hits being lost



Neuromorphic chips – Pixels with intelligence

- Pixel output connected to a SOMA circuits
- Asynchronous, time frame less operation
- “I have data” – “read me now”.
- Pixels with intelligence – self arbitrating the common bus with collision control
- Pixel is determining that it has control of the bus and not the periphery
- Extremely low power – might be useful for e.g. in XPCS – where you want to implement correlation functions. Could lead to self learning.

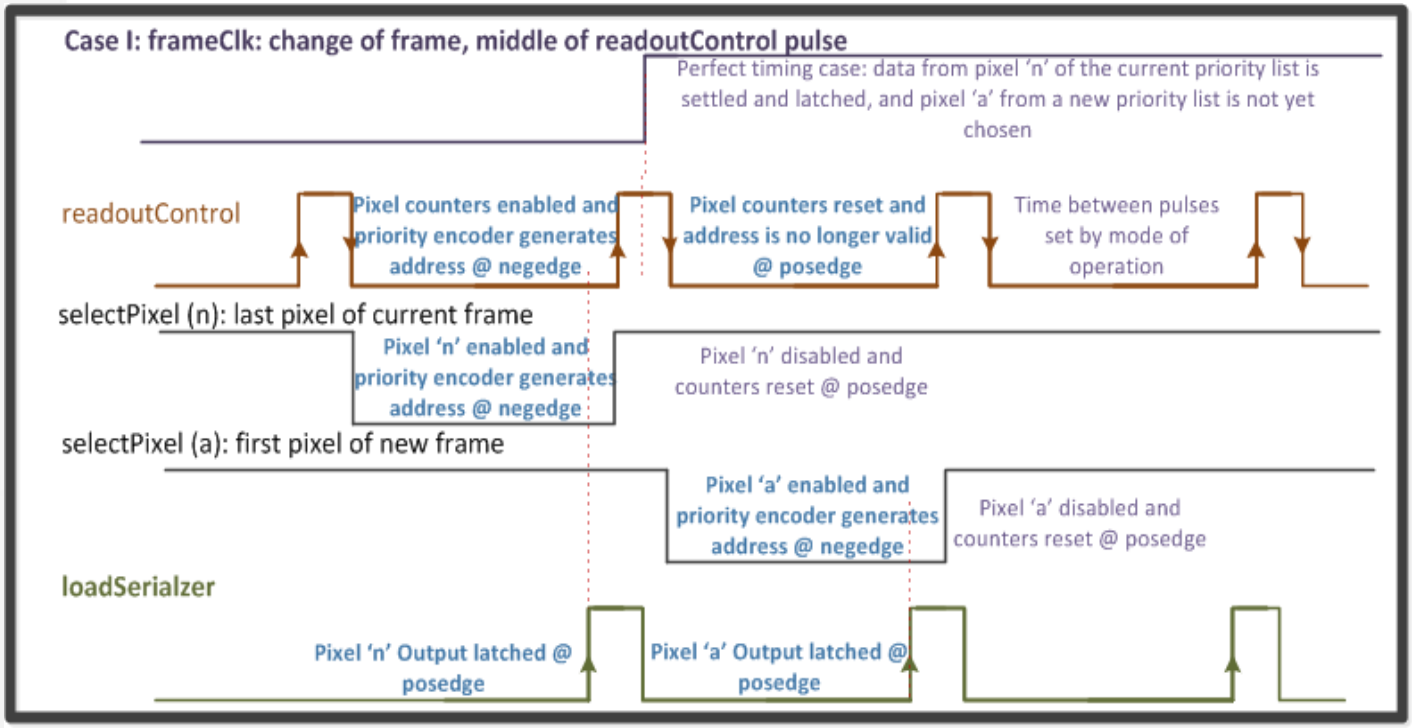
Operating within Time Frames vs. Event Driven

- Depends on in-coming photon count rates
- Time frames suitable for high count rates – window of operation.
- Time frame provides coarse timing information
- Event driven for low occupancy – as soon as data is generated move off chip (e.g. time stamps)

Moving data from Periphery to Off-chip

- **User programmable time frames**

Readout strategy for synchronous readout with user defined slow frame change



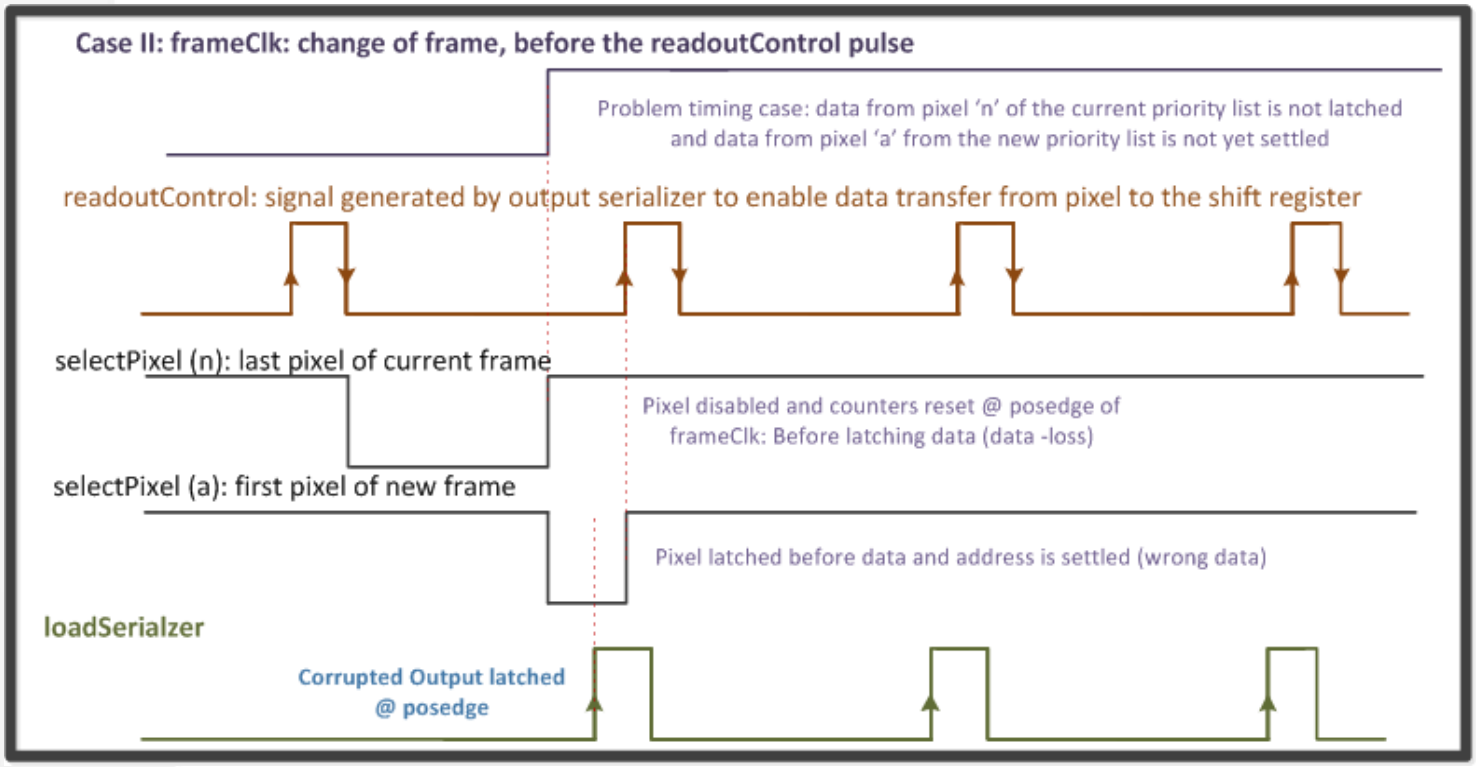
frameClk: rising edge used to indicate change of frame (external slow clock).

readoutControl: is used to enable data transfer from a pixel to the serializer register, which is generated by the output serializer. This signal is interleaved between the two 512 pixel banks and is alternately broadcasted to the top pixel matrix and then to the bottom pixel matrix for pixel selection. The readoutControl pulse width is 2.5 ns corresponding to the serializerClk of 400 MHz. The time between the pulses of readoutControl is set by the readout mode depending on the number of output bits.

selectPixel (n): allows for the contents of the counter to be enabled and the pixel address to be established by the priority encoder. Effectively, this signal is the readoutControl signal as seen by the pixel, controlled by the priority encoder. The negative edge of the readoutControl enables the pixel and the positive edge disables it. The next negative edge of readoutControl selects a new pixel, next in the priority list established by the priority encoder.

loadSerializer: is used to latch data alternately from the top and bottom pixel matrix. It is issued just before the next pixel is selected to ensure that the data has sufficient time to settle before being latched.

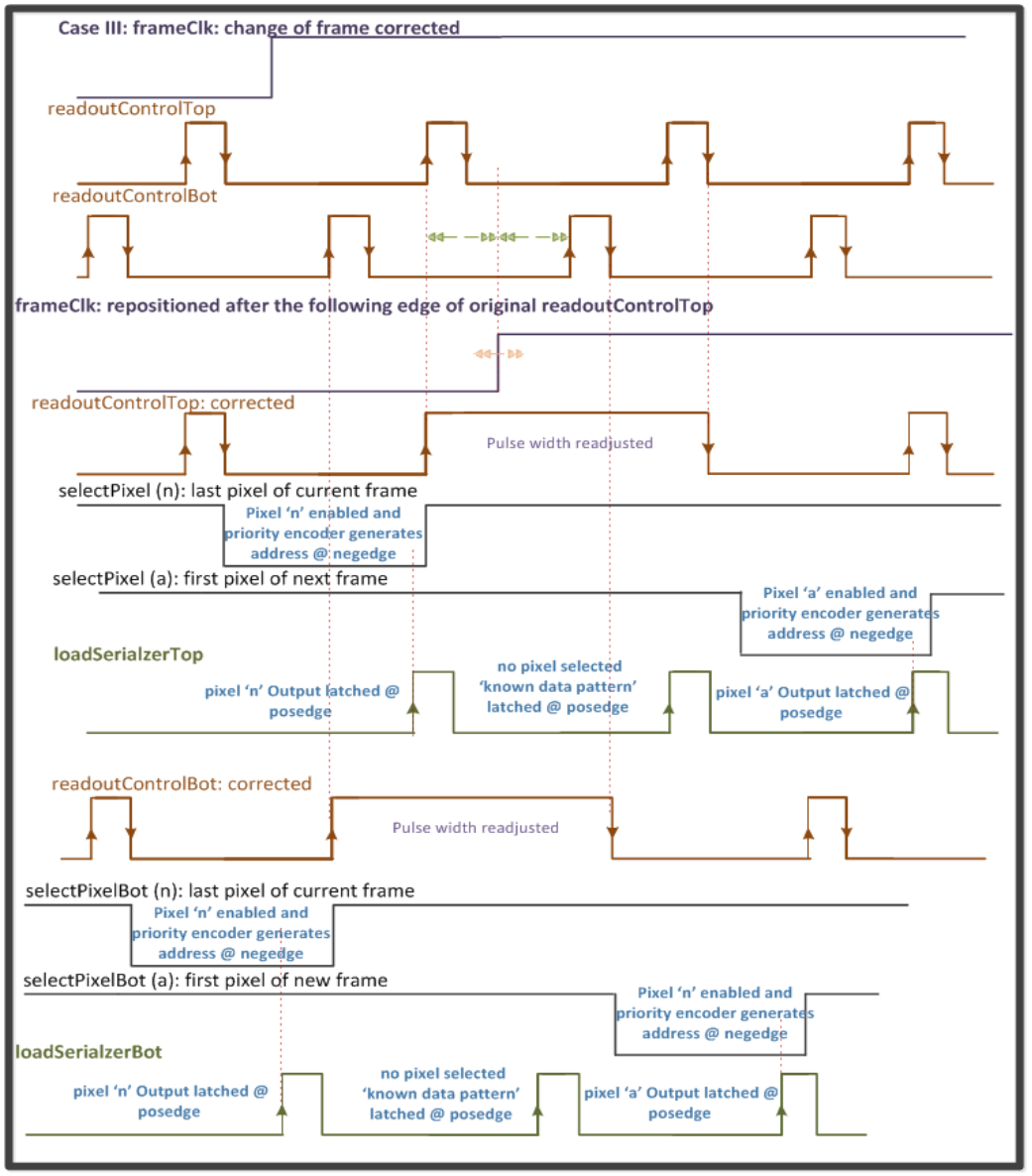
Readout strategy for synchronous readout with user defined slow frame change



- Change in priority
- Two independent paths of frameClk and readoutControl
- Corruption of data

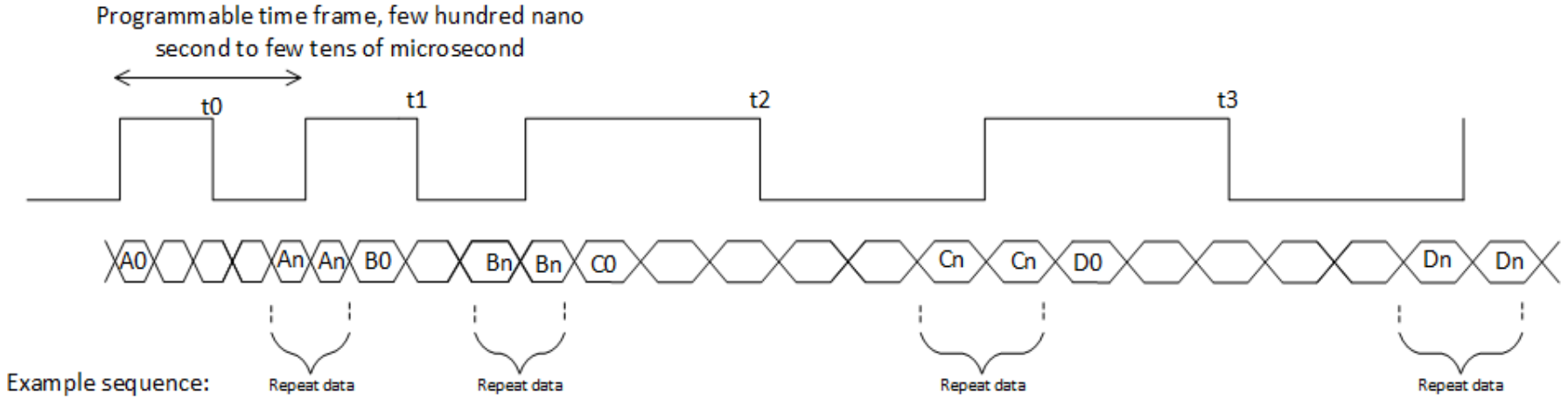
Strobeless Readout strategy

- Changes time frame seen by the pixel to avoid data corruption
- Allows random changes in mode, time frame and data packet length
- Inserts two known data packets or repeats data twice at the end of time frame, identifiable by DAQ for synchronization



Periphery communicating with DAQ – no resynchronization

- User programmable time frames
- Time frame can change at anytime.
  - How to ensure data is not lost or corrupted
- How to self-synchronize with the DAQ without long headers



Example sequence:
A0 - An: 5 bit imaging mode
B0 - Bn: 7 bit imaging mode
C0 – Cn: 20-bit FPGA synchronization mode
D0 – Dn: 17-bit Zero-suppressed mode with 7-bit counter

Generally clock frequency is changed or interrupted to resynchronize

- **Change time frame when no pixels are selected**
- **Use the exact same time duration of disabling all pixels by sending a 'known data packet'**
- **Use the 'known data packet' to identify start of new data packets**

Questions?

Key definitions

- Pixel: Position sensitive processing unit
- Periphery: Logic on chip directly communicating with I/O for data transfer from the pixel
- Time Frame: Window of operation in which pixel is allowed to count photons or integrate signal. Global shutter.
- Asynchronous photon arrival – Counting type (mostly digital) – e.g. can have an analog counter
- Burst mode – Integrating type (mostly analog); photons arrive together
- Deadtimeless: Continuous operation, frontend is always active
- Priority List: List of pixels which need to be read out
- Strobe: Global signal which removes a pixel from priority list when it has finished transferring its contents to the periphery