

# The CHIPIX65 asynchronous front-end for the HL-LHC experiment upgrades

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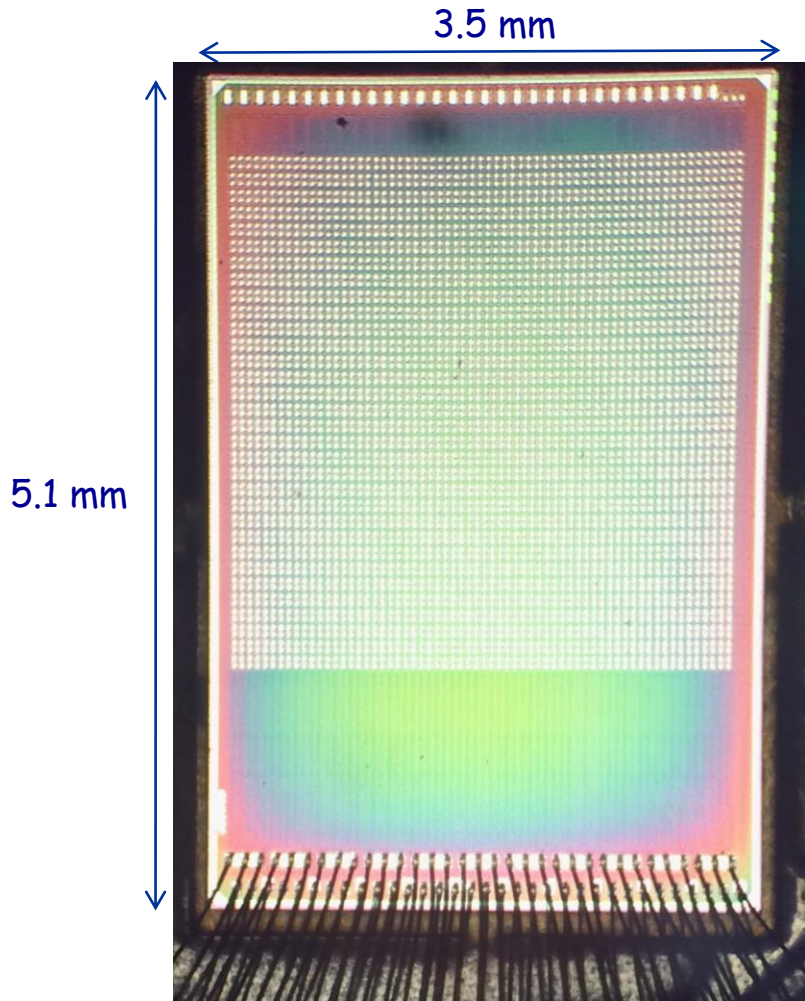
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# Motivation

- Development of an analog front-end in a 65 nm CMOS **mixed-signal chip for readout of high granularity silicon pixel sensors for particle tracking** in the innermost layers of ATLAS and CMS at HL-LHC: the international RD53 collaboration and the INFN CHIPIX65 group
- **Demanding specifications for noise, threshold dispersion, minimum threshold, power dissipation, area, tolerance to extremely high levels of ionizing radiation,...**
- This paper will discuss one of the proposed solutions for the front-end: **an asynchronous analog pixel cell with continuous time charge sensitive preamplifier and discriminator for ToT-based A/D conversion, local DAC for threshold adjustment**
- This front-end was integrated in single channel prototypes, in the CHIPIX65 demonstrator and in the RD53A large scale demonstrator: discussion of test results available so far

# The CHIPIX65 demonstrator chip

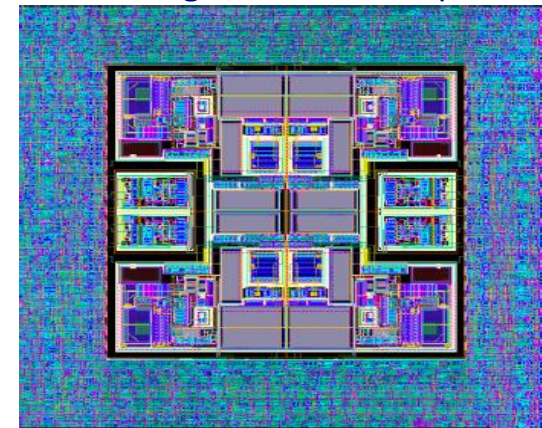


64x64 matrix,  $50 \times 50 \mu\text{m}^2$  pixel

- Two analog front-end architectures
- 5-bit ToT signal digitization, max ToT = 400 ns
- Minimum threshold  $< 600 e^-$ , In-time threshold  $< 1200 e^-$
- Noise  $\sim 100 e^-$  rms with no sensor connected
- 2x2 Analog Islands on 4x4 pixel region digital architecture
- FE & IP-blocks developed in RD53

INFN (Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa and Torino)

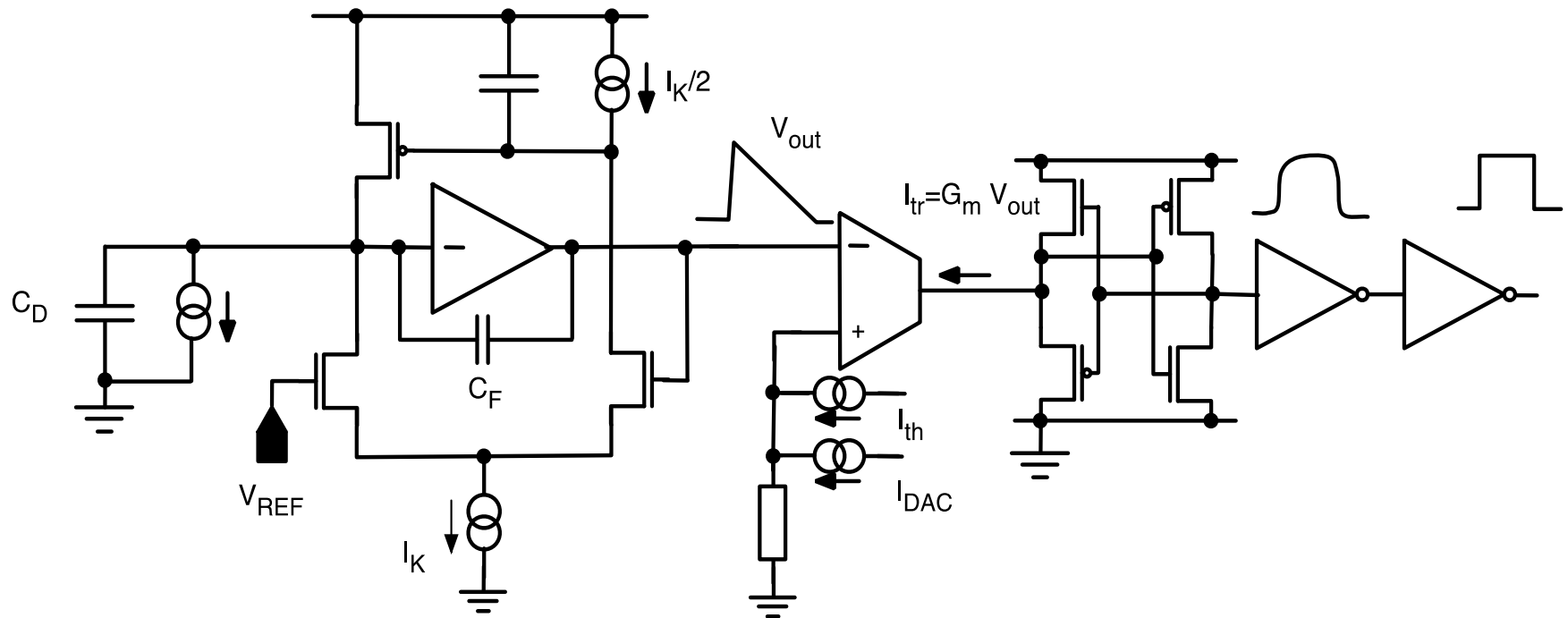
"Analog island" concept



# The CHIPIX65 demonstrator chip and its two analog front-ends

- The CHIPIX65 demonstrator served the goal of testing design solutions (analog and digital) on a small-scale 65 nm CMOS chip, allowing for a performance evaluation before the integration of the large scale RD53A chip
- **Two different analog front-end architectures** were integrated in the pixel cells of the CHIPIX65 chip:
  - a **synchronous** one with an autozero comparator (Torino)
  - an **asynchronous** one (Bergamo/Pavia) implementing a linear pulse amplification in front of the discriminator, which compares the pulse to a threshold voltage (locally adjusted by a DAC)
- Both front-ends were designed according to RD53A requirements, among which the capability of operating at a minimum threshold of  $600 e^-$ , with a power consumption not exceeding  $4 \mu W$  in a silicon area of  $35 \mu m \times 35 \mu m$

# The asynchronous analog front-end in the CHIPIX65 demo chip

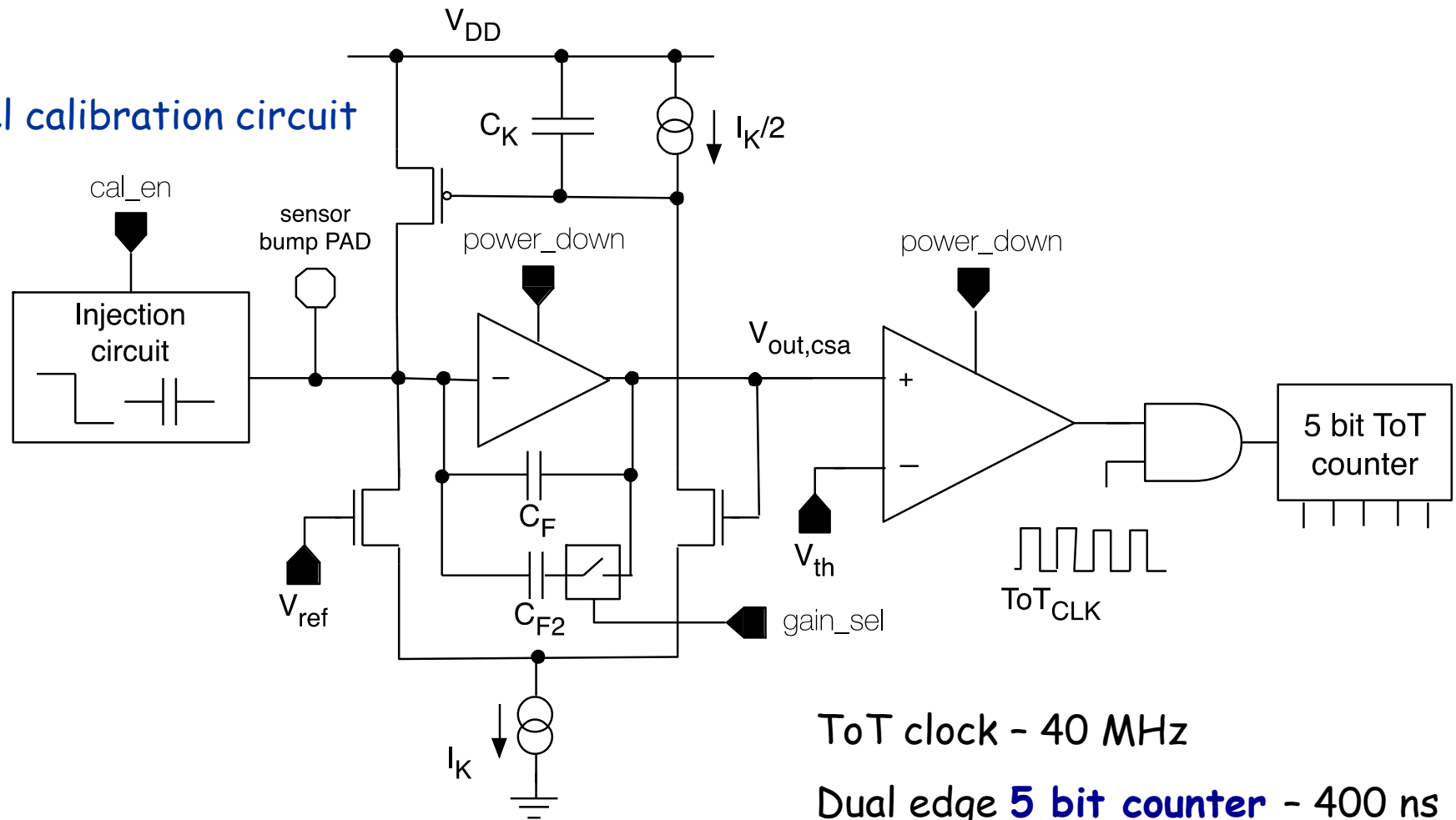


- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- High speed, low power **current comparator**
- **4 bit local DAC for threshold tuning**

- **30000 electrons** maximum input charge, ~450 mV preampli output dynamic range
- Selectable gain and recovery current
- Overall **current consumption**: ~4  $\mu\text{A}$

# The asynchronous analog front-end in the CHIPIX65 demo chip

In-pixel calibration circuit



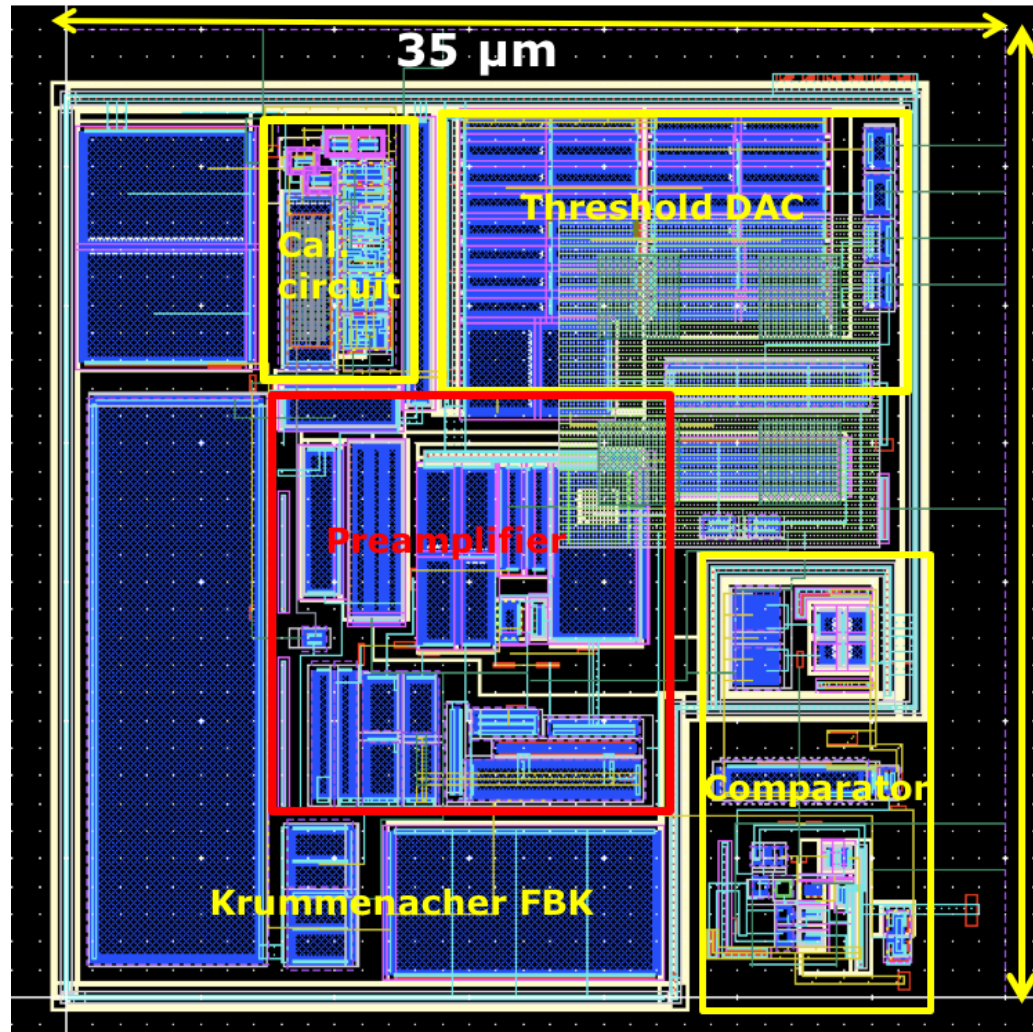
ToT clock - 40 MHz

Dual edge **5 bit counter** - 400 ns  
maximum time over threshold



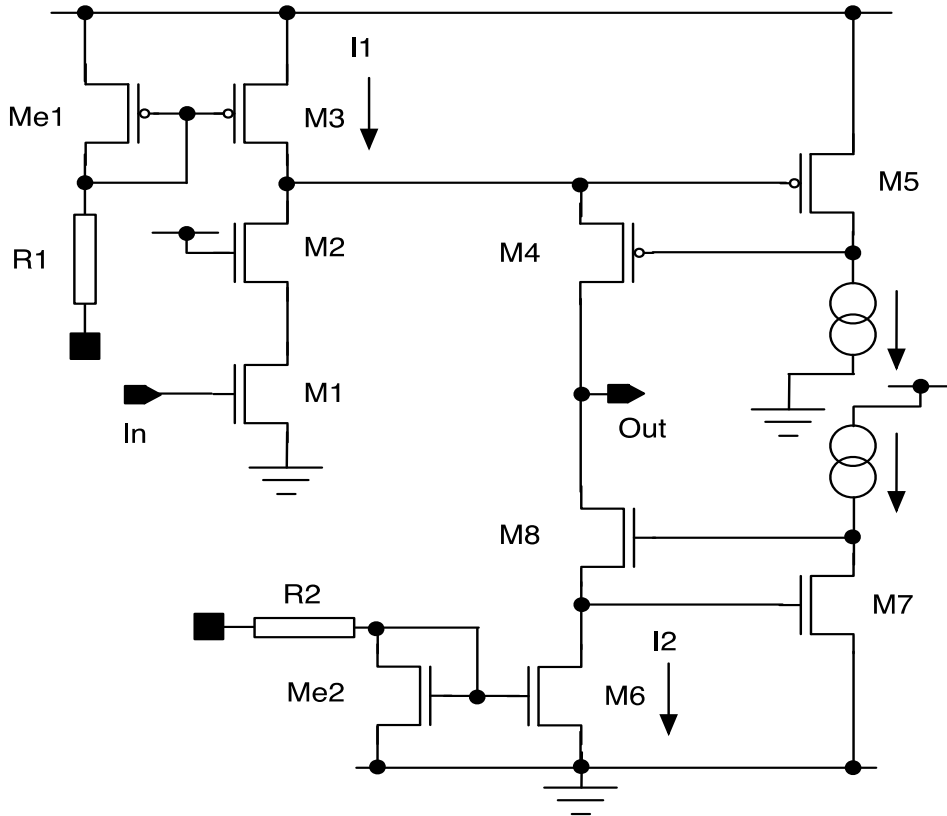
# Layout of the asynchronous analog cell

- Analog FE in DNW
- Local routing  
M1, M2, M3



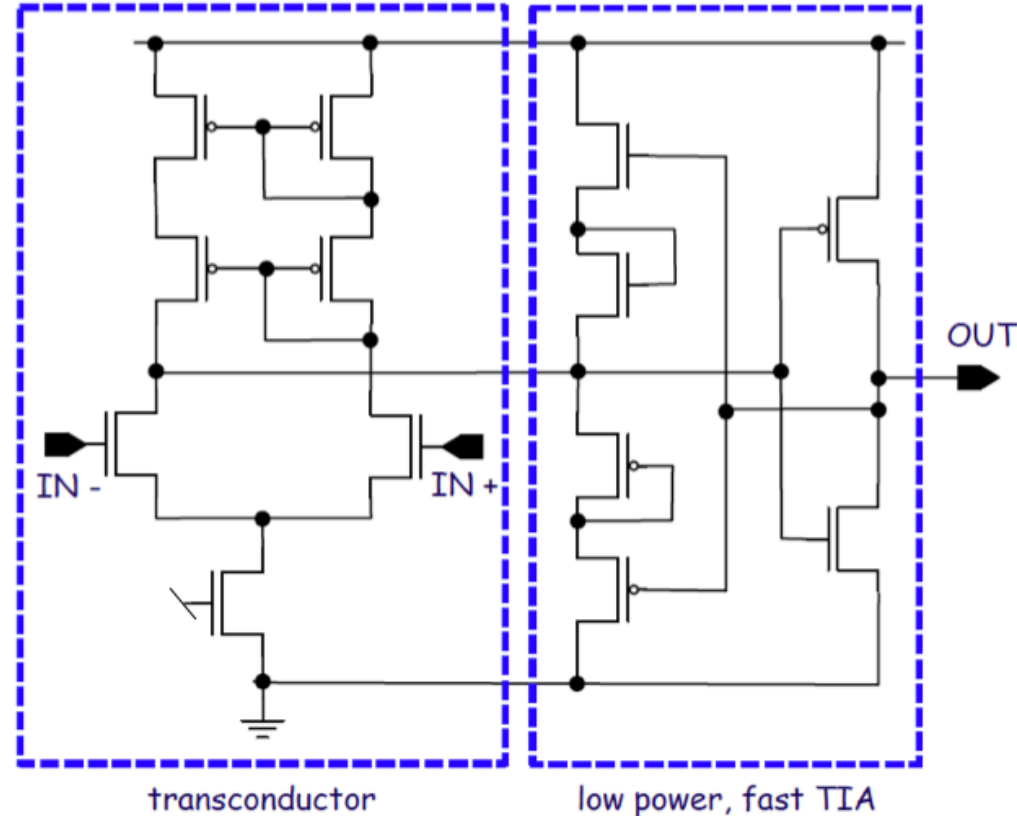
# Schematics

## Preamplifier



- Gain stage based on a **folded cascode** configuration ( $\sim 3 \mu\text{A}$  absorbed current) with a regulated cascode load

## Comparator

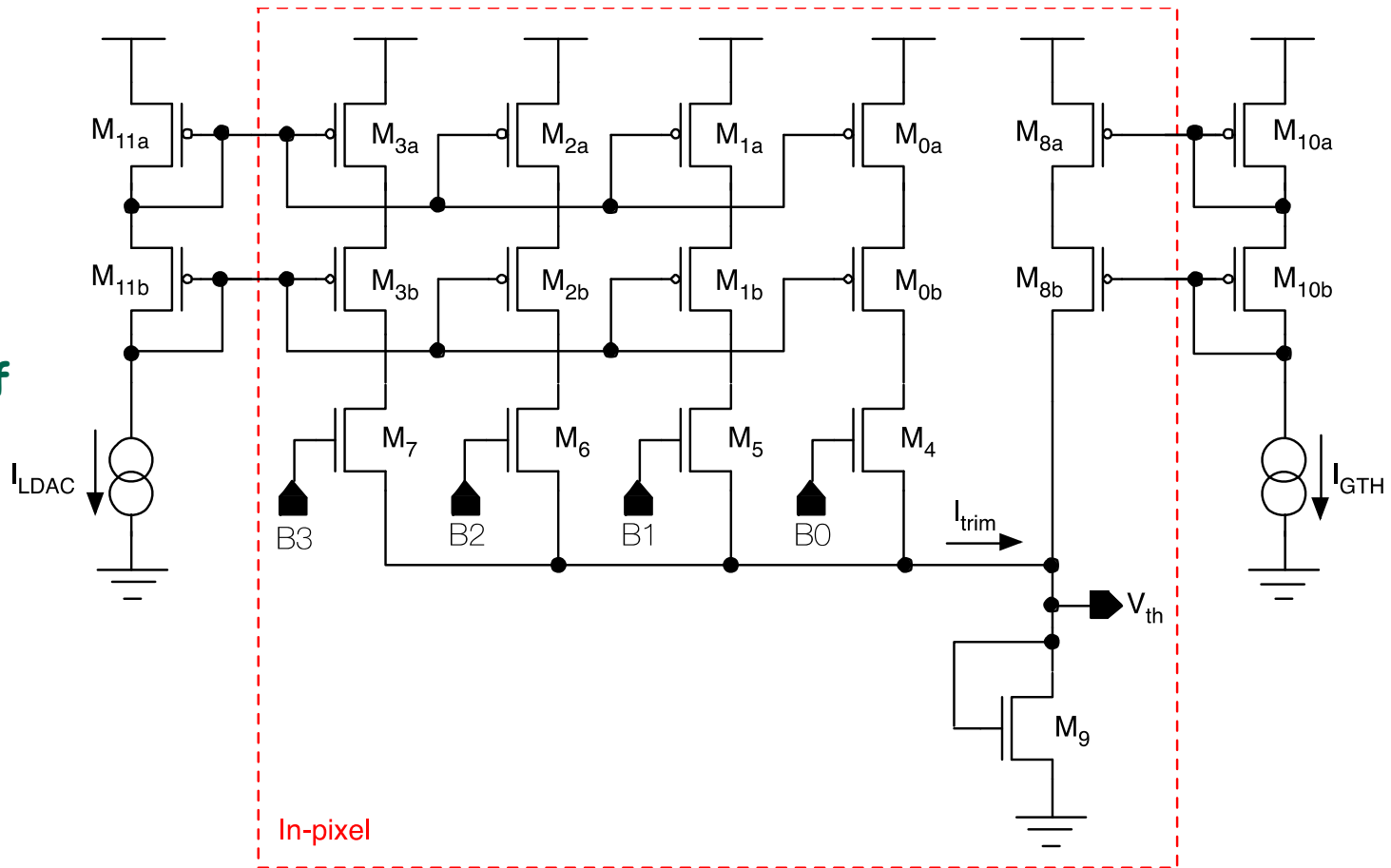


- Low power, **fast discriminator** ( $\sim 1 \mu\text{A}$  absorbed current) including  $G_m$  stage and a transimpedance amplifier providing a low impedance path for fast switching



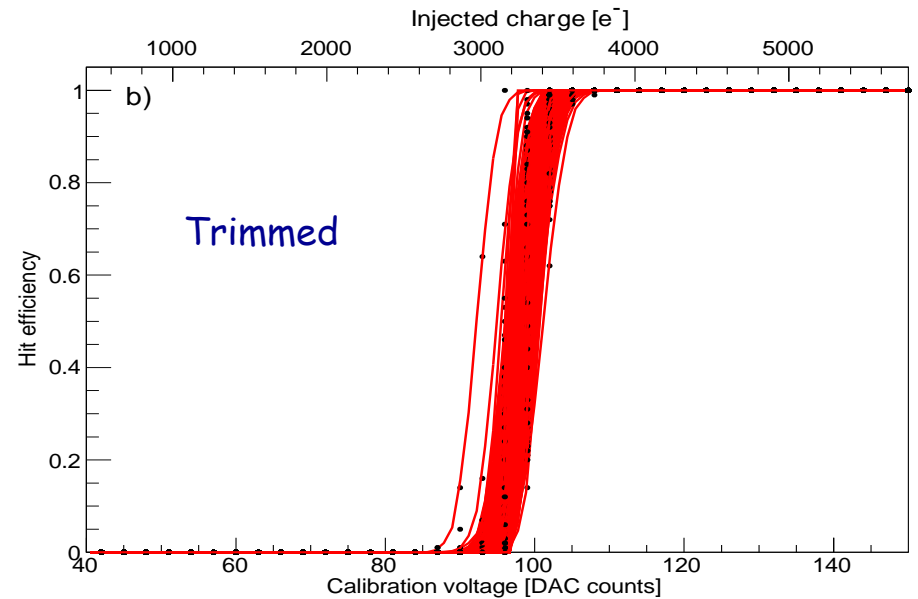
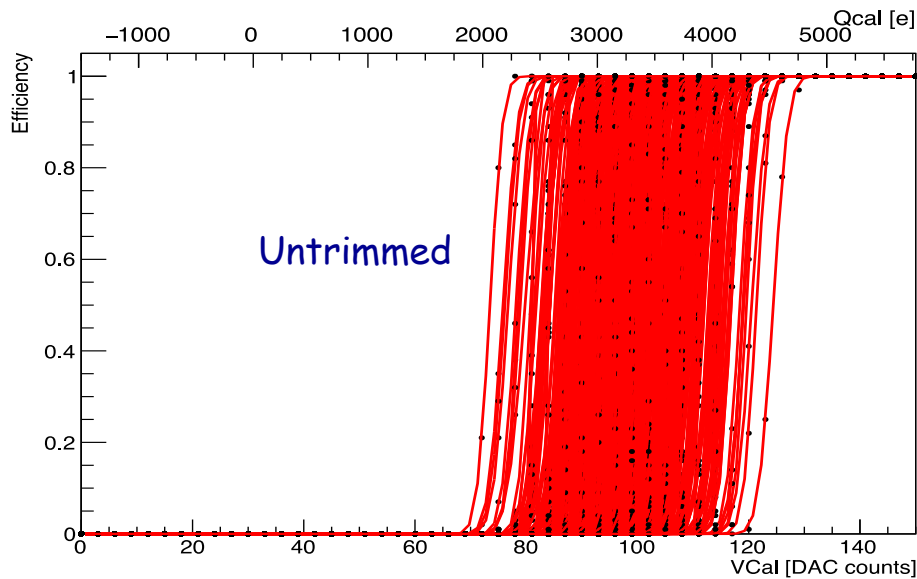
# 4-bit Threshold DAC

Output range of the threshold trimming DAC

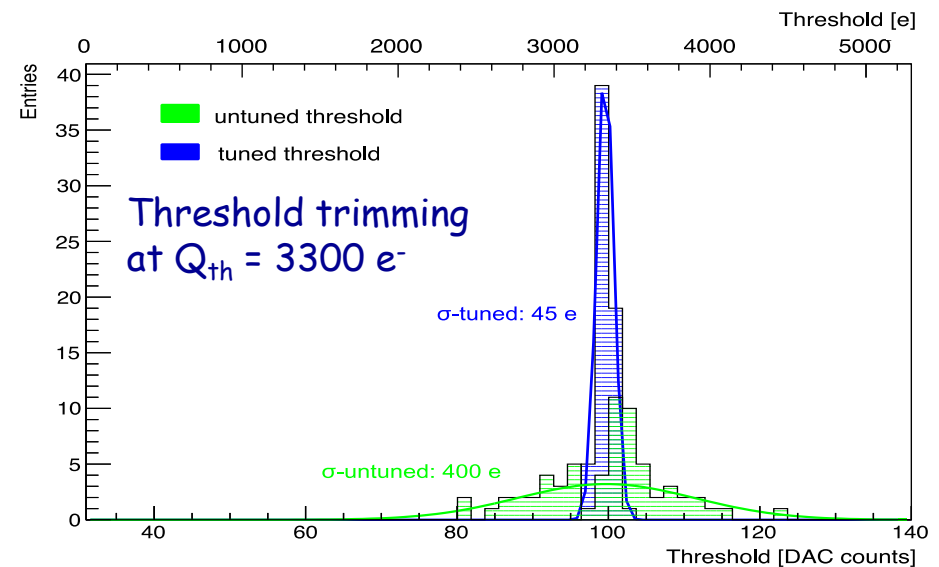


Global threshold reference

# Experimental results: threshold dispersion and noise

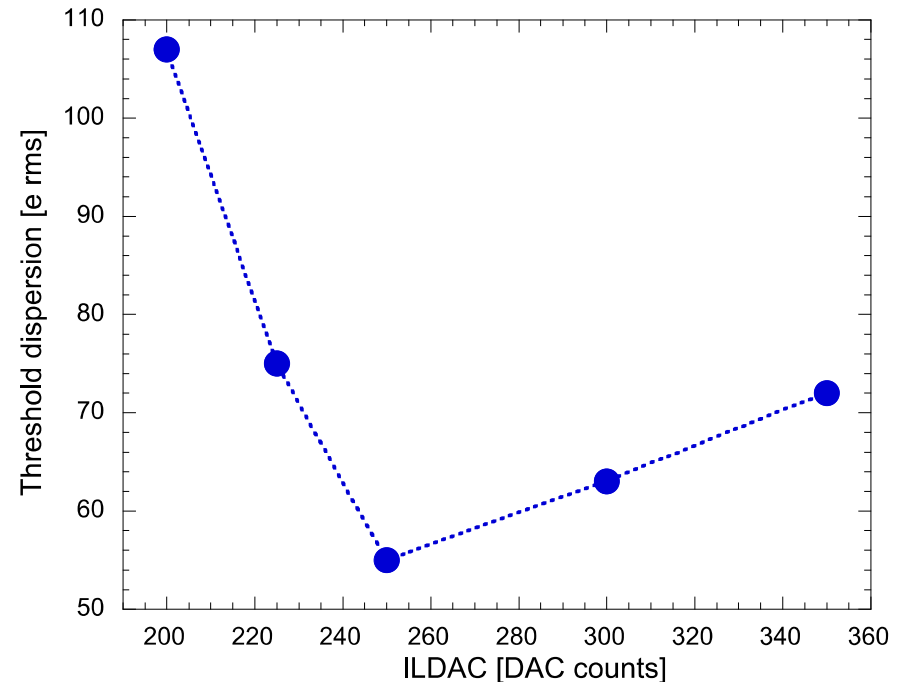
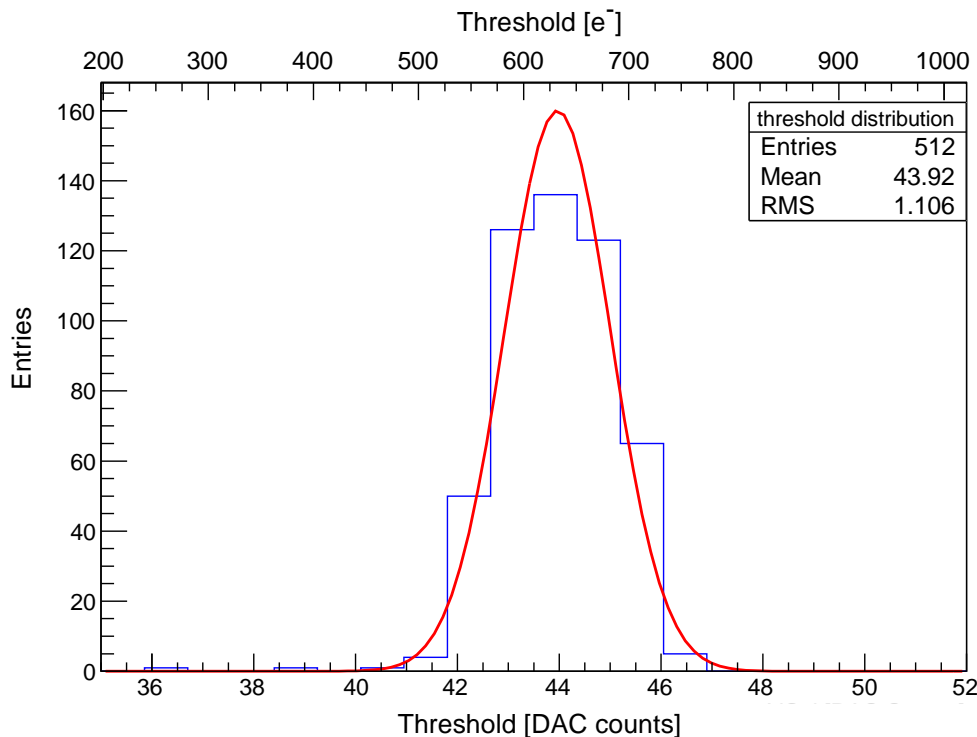


- All pixels tested and fully working
- $\approx 400$  e rms untrimmed threshold dispersion
- per-pixel DAC codes extracted from untrimmed S-curves using a set of ROOT macros and then loaded into the chip
- $\approx 45$  e rms trimmed threshold dispersion, in good agreement with CAD simulations



# Threshold dispersion at $Q_{th} \approx 600$ electrons

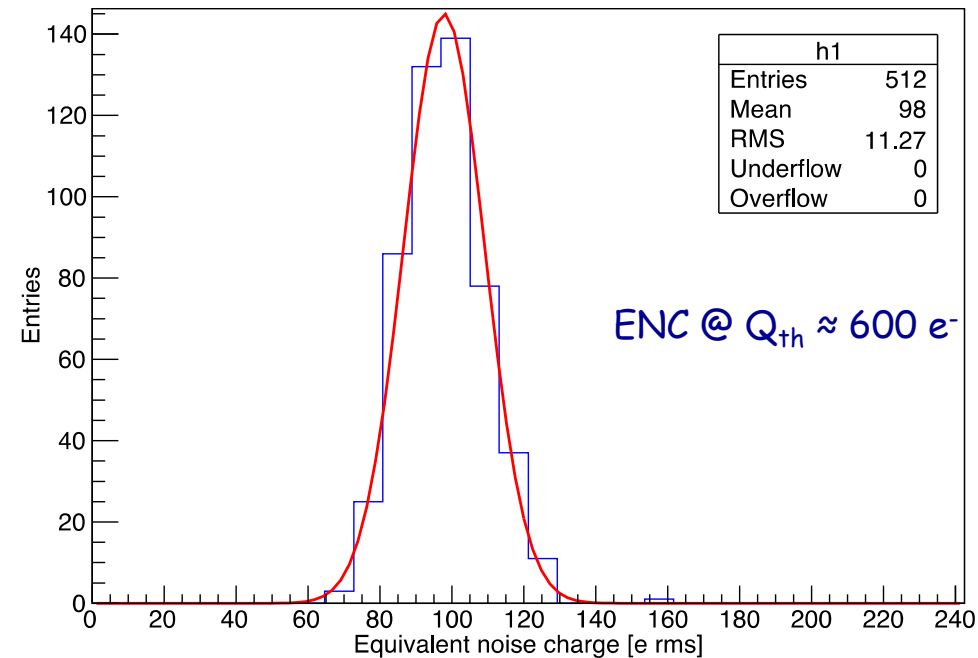
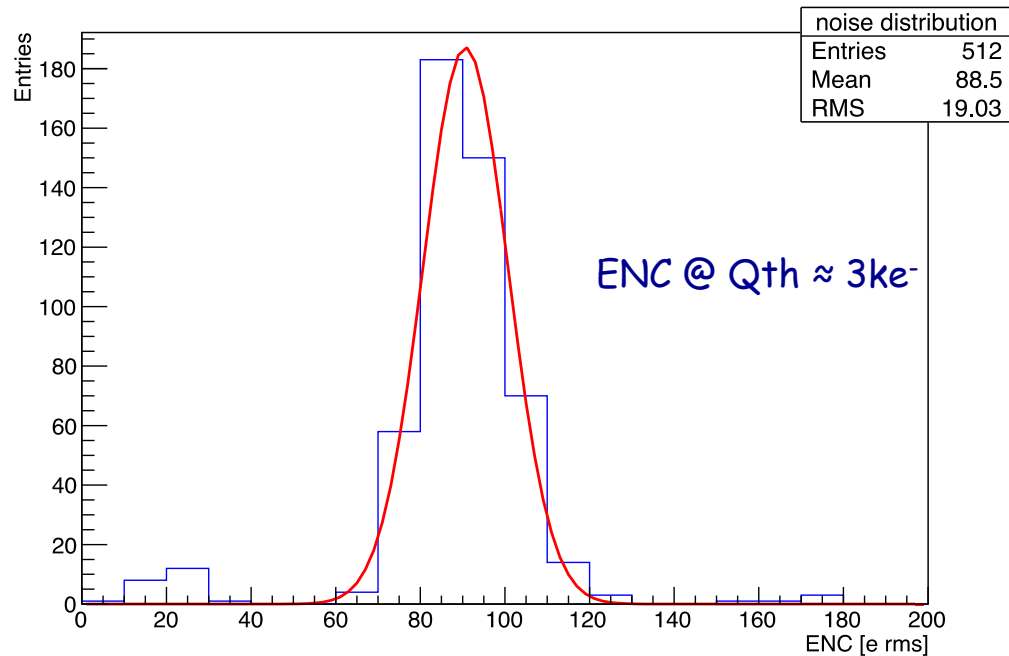
The capability of operating at low threshold settings is demonstrated



Threshold dispersion  $\sigma(Q_{th}) \approx 55$  e rms  
after tuning at 600 electrons threshold  $Q_{th}$

Optimum threshold DAC range at  
about 2000 electrons corresponding to  
about  $5 \times \sigma(Q_{th})$  before tuning

# Low noise operation at low threshold setting

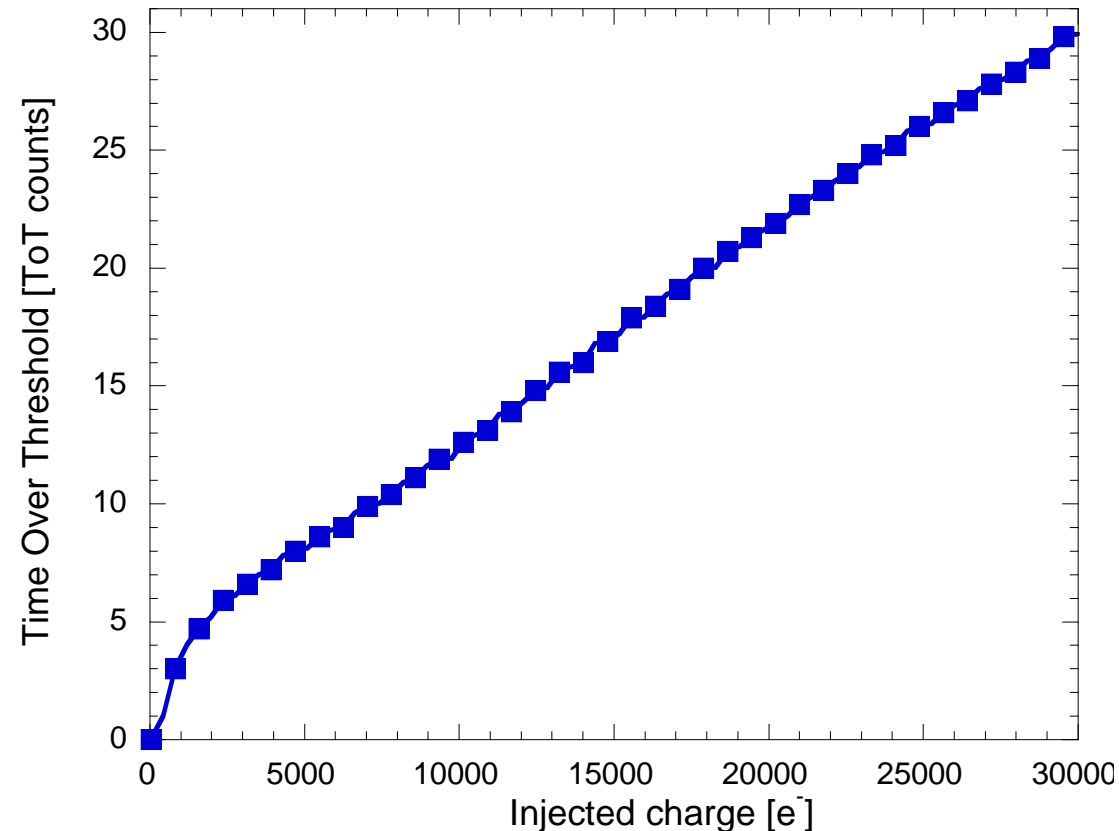


**Mean ENC  $\approx 90 e$  rms before irradiation  
(no sensor connected)**





# Time-over-Threshold linearity as a function of the input charge



At input charge  $Q_{in}$  large enough to saturate the Krummenacher feedback, the preamplifier feedback capacitor is linearly discharged by a constant current  $I_K/2$ :

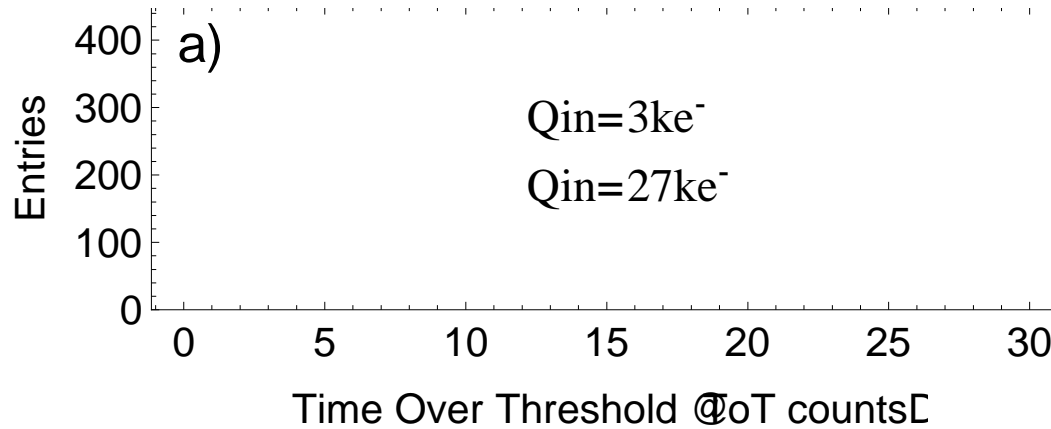
$$\text{ToT} = 2 \frac{Q_{in} - Q_{th}}{I_K}$$

The value of  $I_K$  (25 nA) is set according to the maximum ToT (400 ns) over the expected  $Q_{in}$  range (30 ke<sup>-</sup>).

ToT is affected by the threshold dispersion and by channel-to-channel mismatch of the Krummenacher feedback current  $I_K$

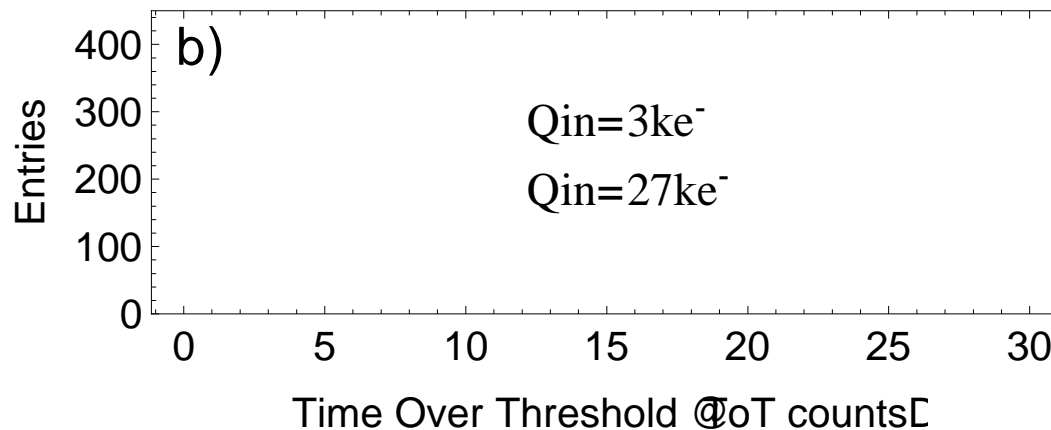
# Time-over-Threshold dispersion

Untrimmed  
threshold  
(nominal  $Q_{th} = 2800$  electrons)



For large  $(Q_{in} - Q_{th})$  values, ToT dispersion is dominated by the dispersion of the Krummenacher current  $I_K$ .

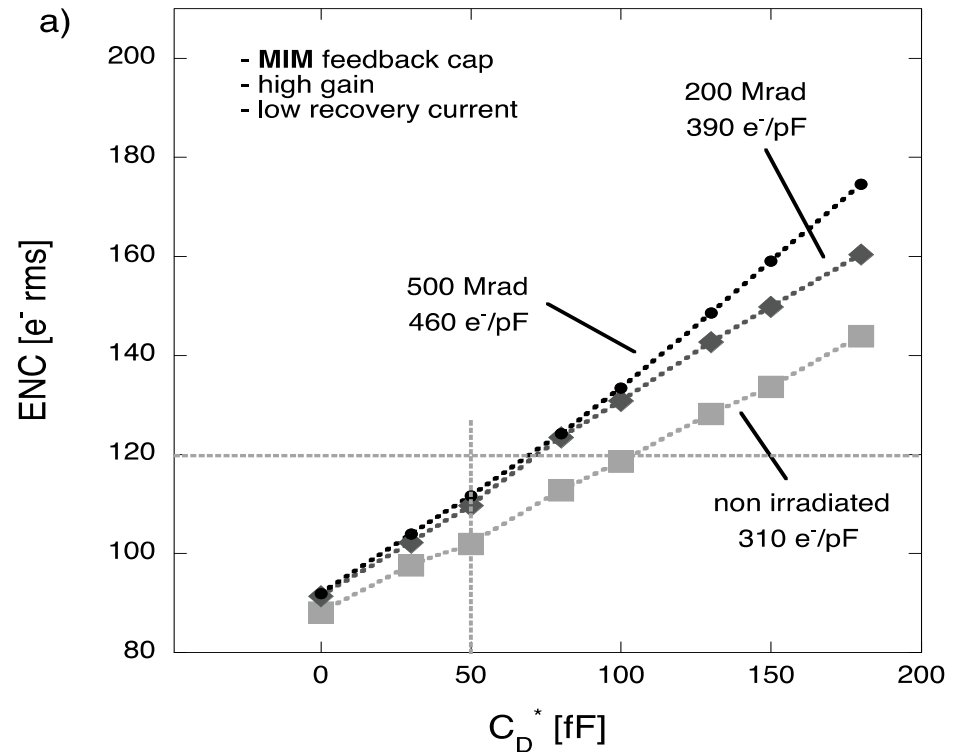
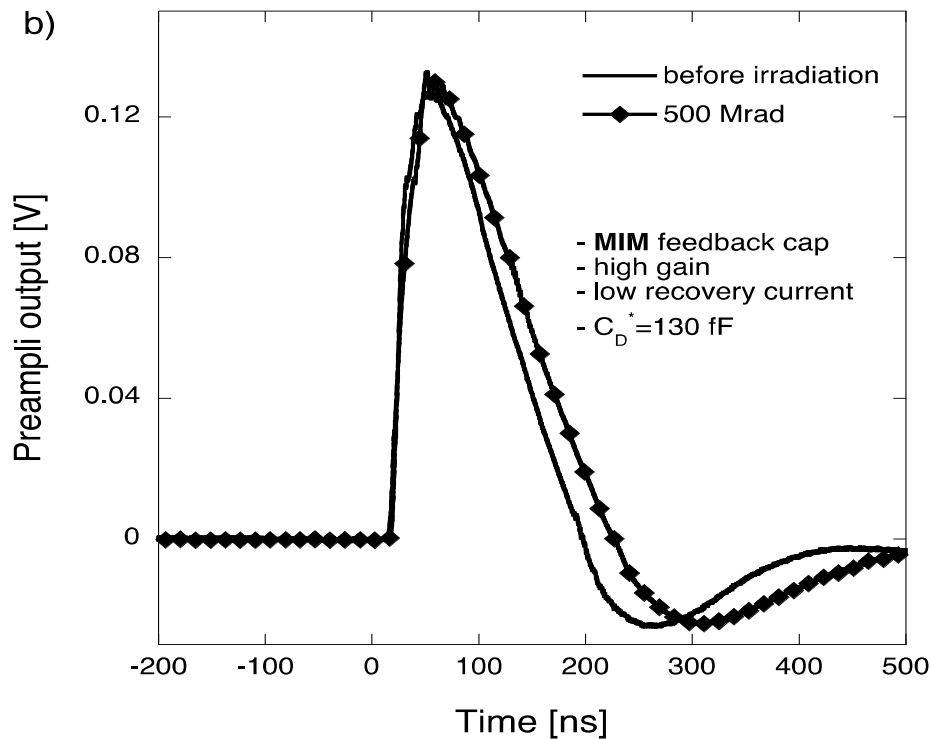
Trimmed  
threshold  
(nominal  $Q_{th} = 2800$  electrons)



For small  $(Q_{in} - Q_{th})$  values, ToT dispersion is dominated by the dispersion of the threshold  $Q_{th}$ .

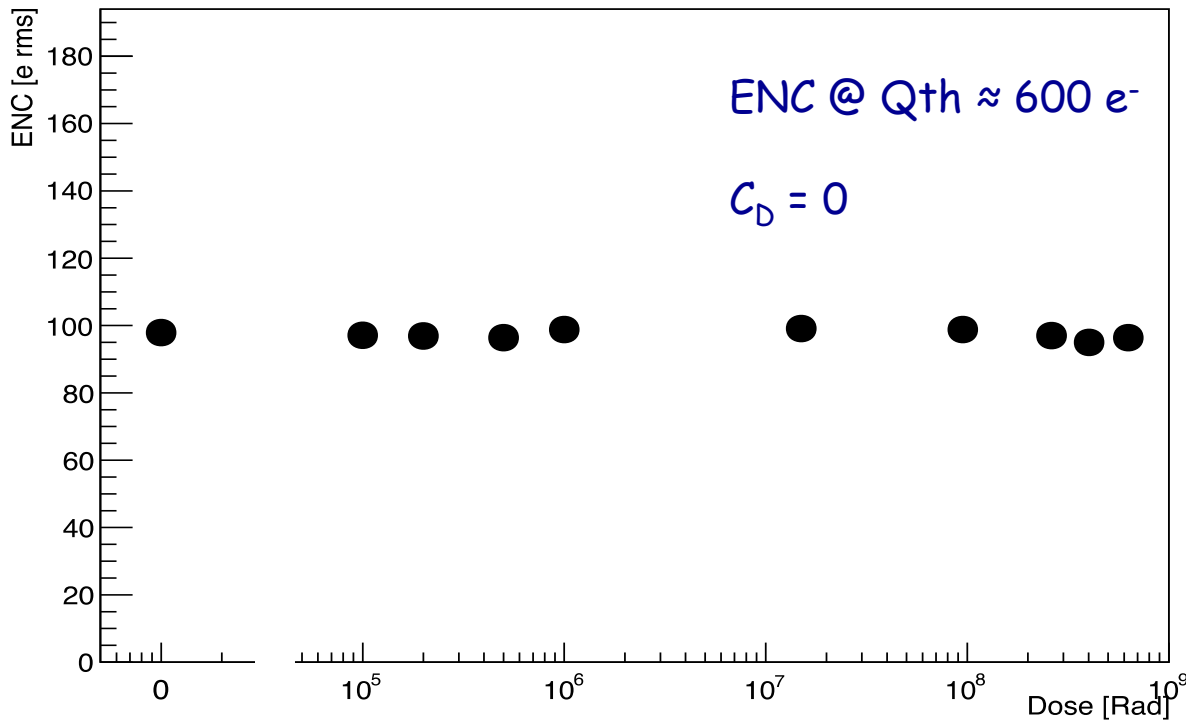
# Irradiation tests up to 500 Mrad TID: single channels

- Prototypes of the front-end exposed to 3 MeV protons and to 10 keV X-rays (room T)
- The analog channel remains fully functional up to 500 Mrad TID; moderate noise increase is due to 1/f noise degradation in preamplifier input device



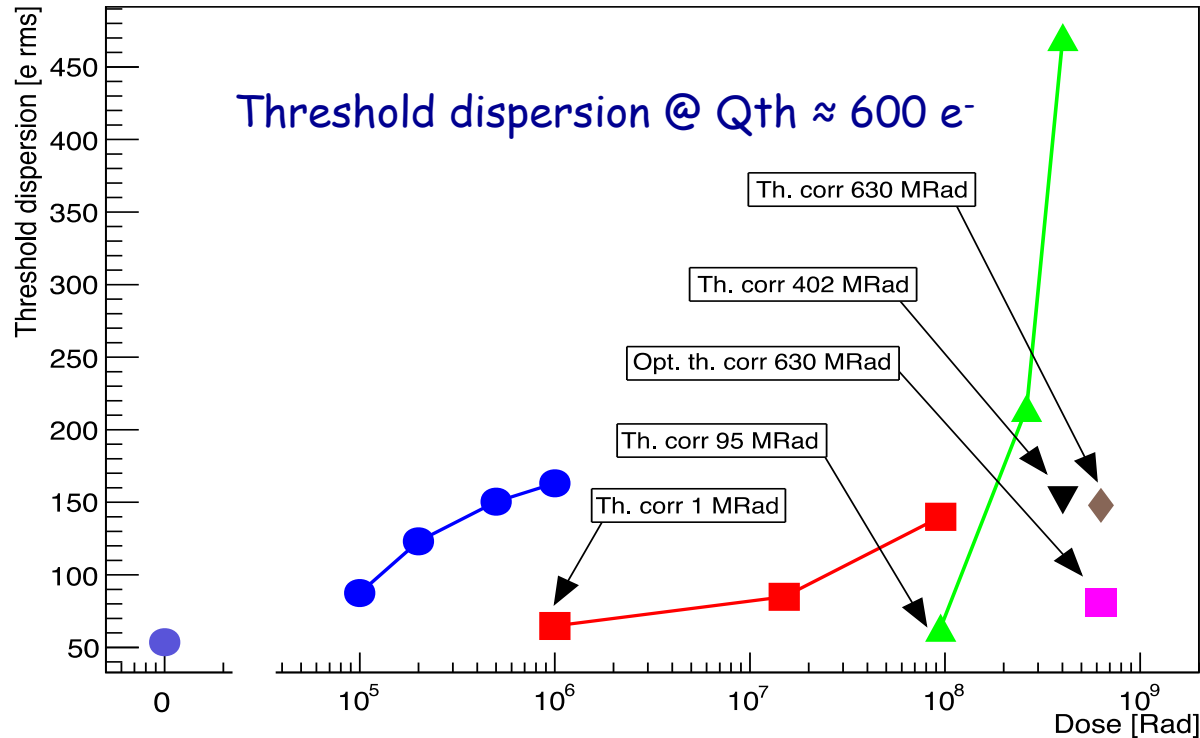
# Irradiation tests up to 630 Mrad: the CHIPIX65 demo chip

CHIPIX65 demonstrator chip with the Pavia/Bergamo front-end exposed to 10 keV X-rays up to 630 Mrad



- 1 sample irradiated with X-rays at Padova INFN at **room temperature**
- Chip biased at nominal operating conditions
- 350 krad/h dose rate for TID < 15 Mrad
- 3.5 Mrad/h dose rate for TID ≥ 15 Mrad
- **chip fully-functional at 630 Mrad TID and one week room temperature annealing (need to restore operation of digital readout)**

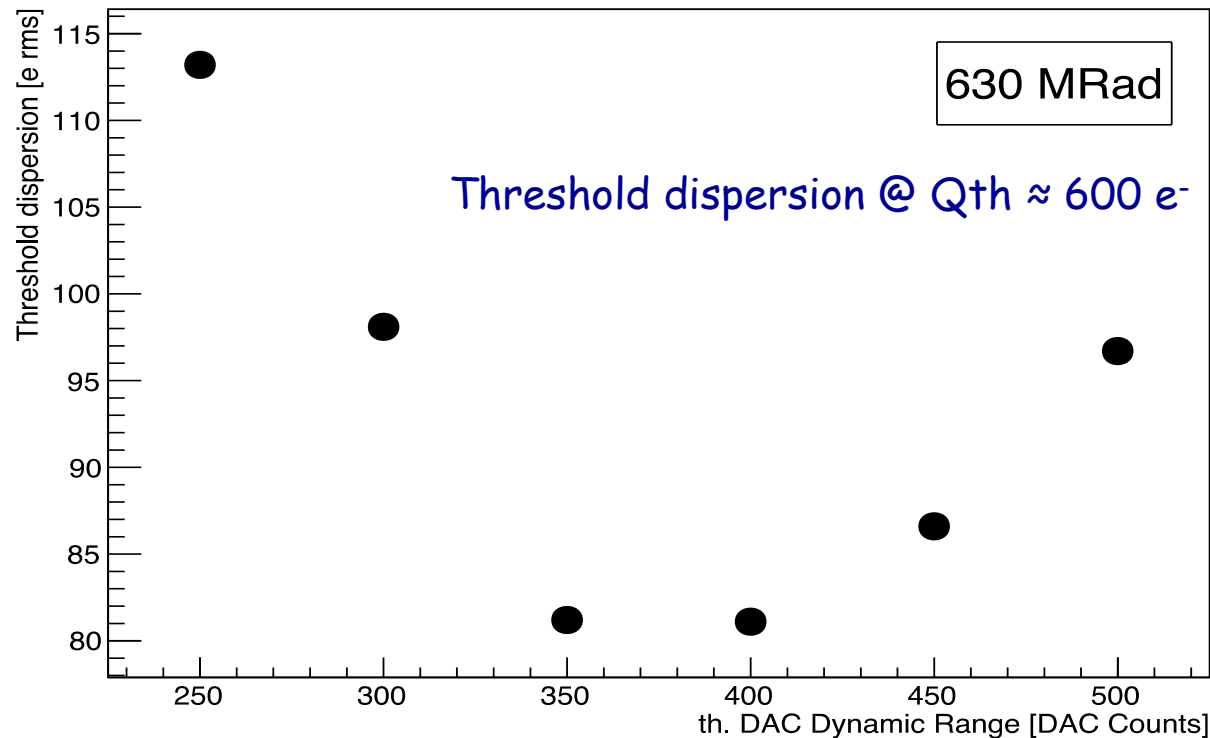
# Irradiation tests up to 630 Mrad: the CHIPIX65 demo chip



- Threshold trimming performed @ 1Mrad, 95 Mrad, 402 Mrad and 630 Mrad
- **After trimming, the threshold dispersion does not exceed about 80 e rms even at the highest TID values**

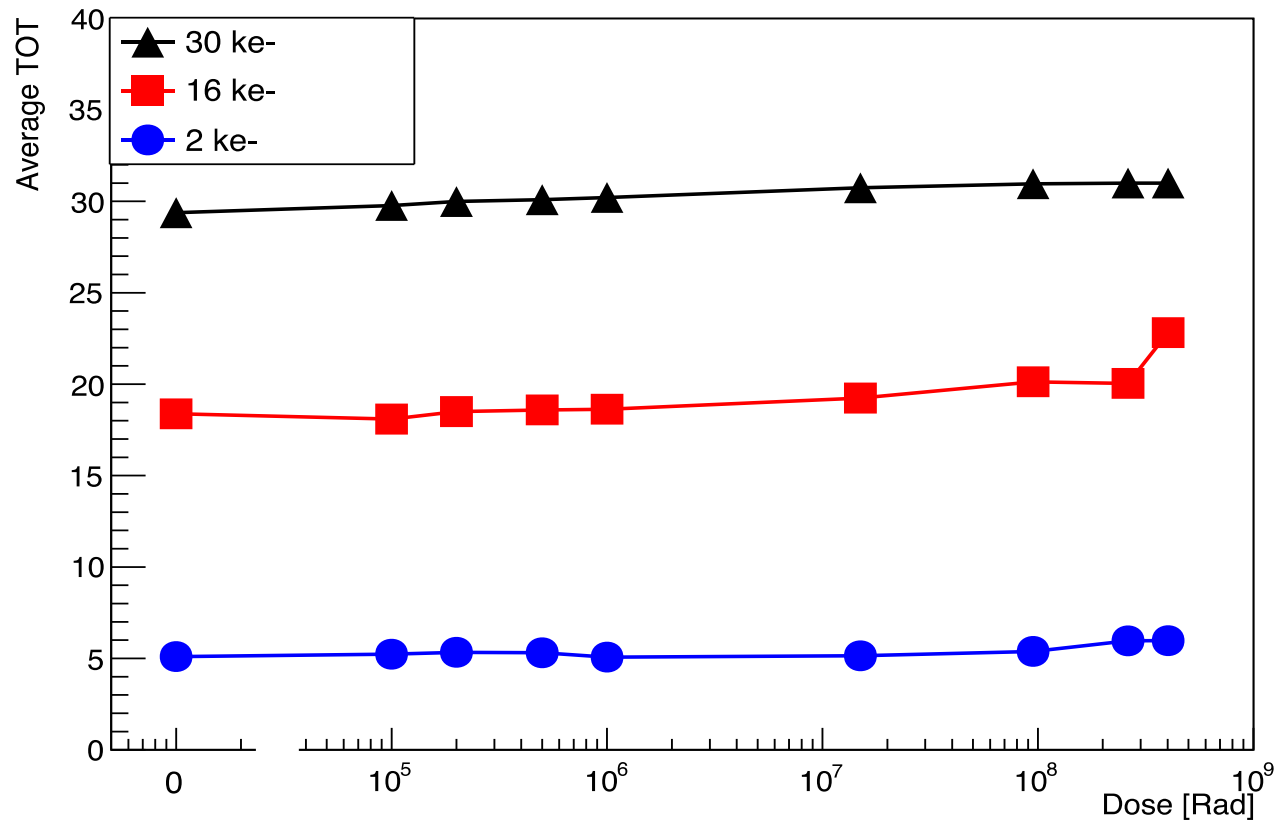


# Irradiation tests up to 630 Mrad: the CHIPIX65 demo chip



- Optimizing threshold dispersion (630 Mrad, 3 weeks annealing at room T) also requires an adjustment of the threshold DAC dynamic range (up to 3000 electrons)

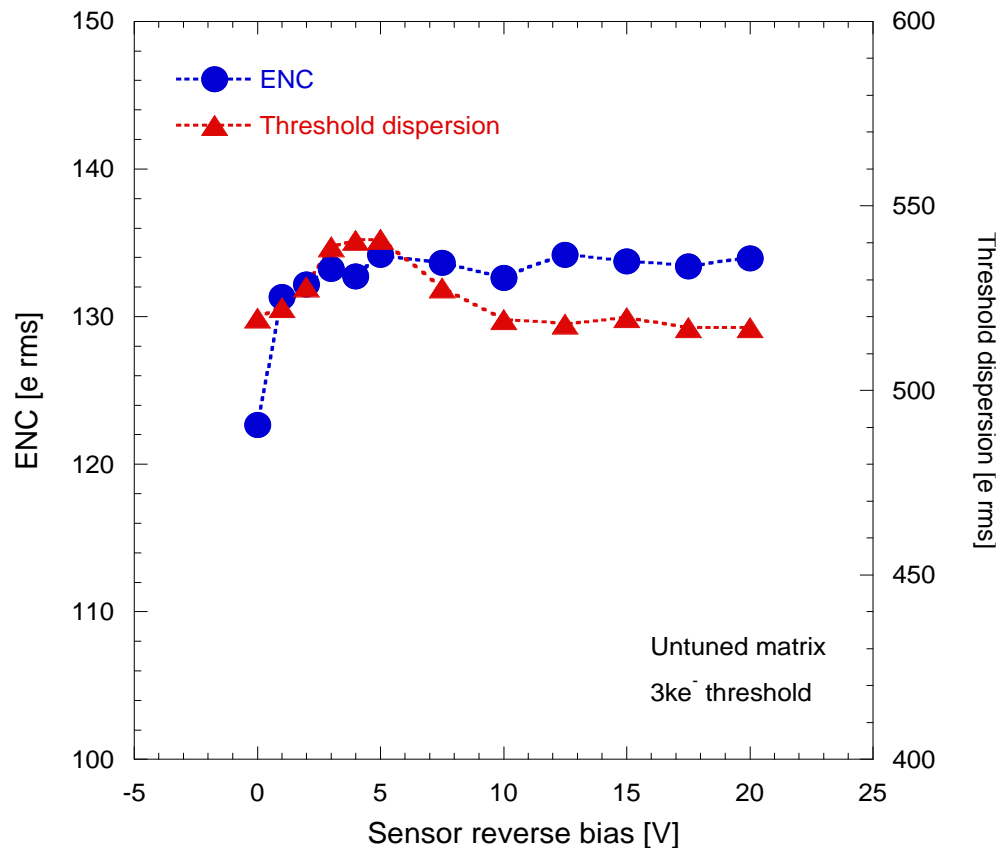
# Irradiation tests up to 630 Mrad: the CHIPIX65 demo chip



Average ToT evaluated at 2k, 16k and 30k electrons

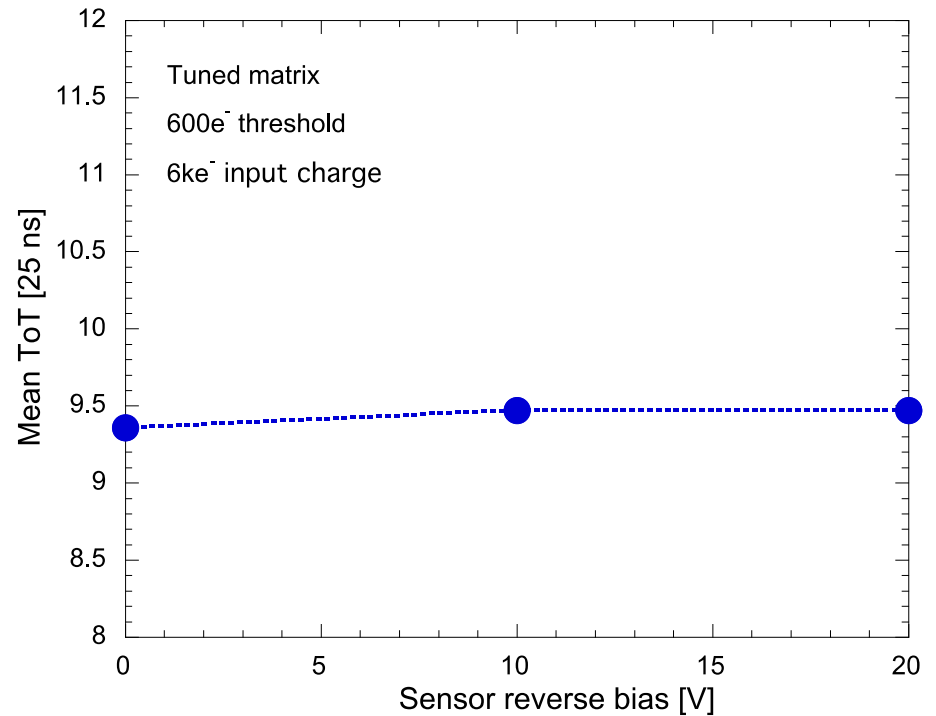
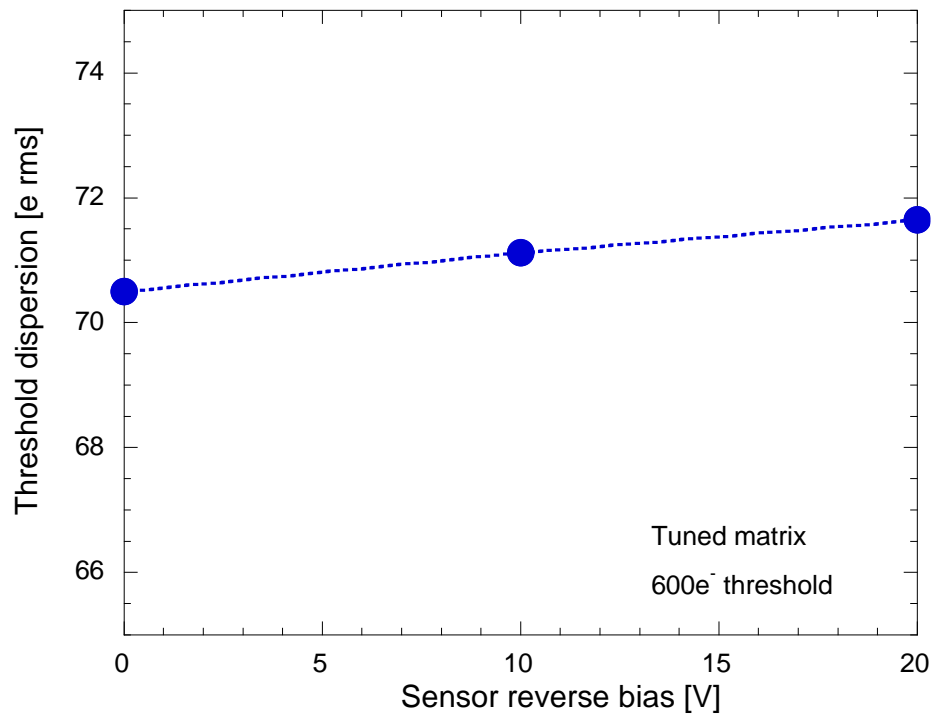
# Tests with 3D pixel sensors

- bump-bonding performed at SLAC with FBK 3D pixel sensors (2016 wafers) (acknowledgements to G.F. Dalla Betta and M. Meschini, and to INFN Torino group)
- sample prototypes coupled to  $50\ \mu\text{m} \times 50\ \mu\text{m}$  pixels, sensor capacitance of about 50 fF (+ about 50 fF from parasitics associated with bumps)



# Tests with 3D pixel sensors: threshold tuning

The asynchronous analog channel can be operated at low threshold also when it is connected to a sensor

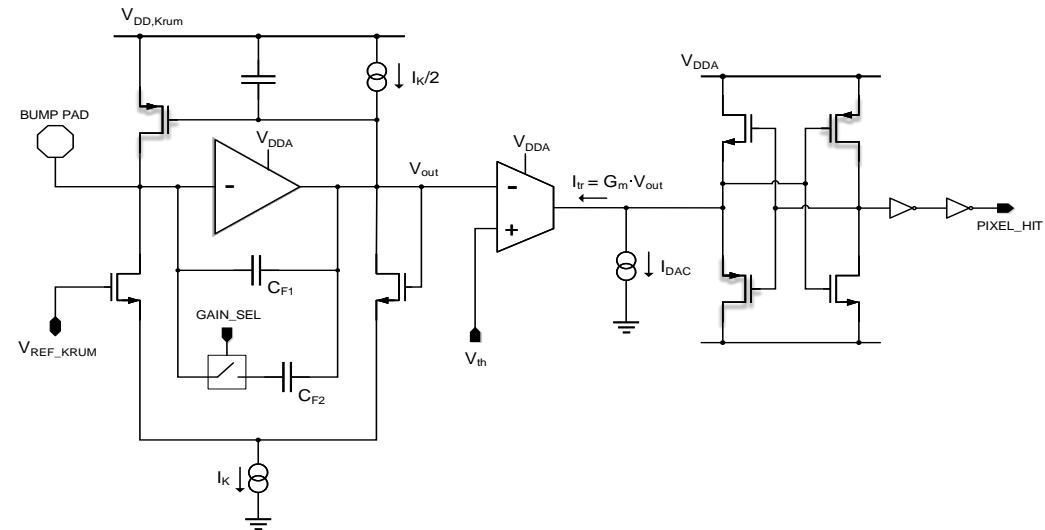
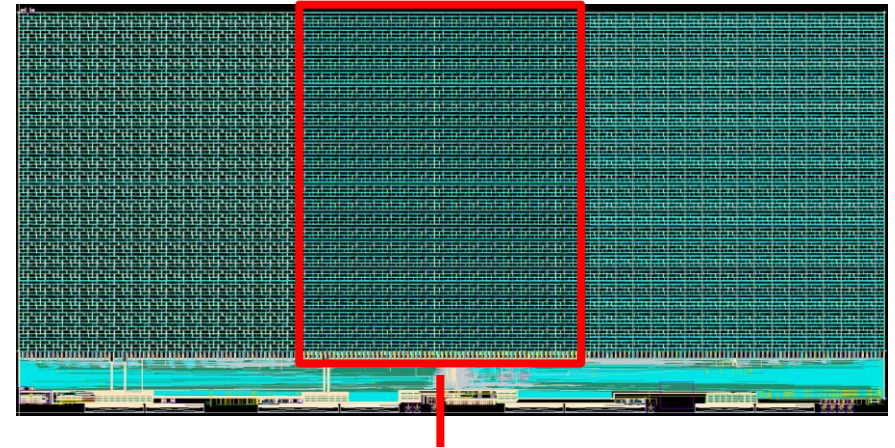


# Front-end integration in RD53A

RD53A is intended to demonstrate in a large format IC (20x11.8 mm<sup>2</sup>) the suitability of the chosen 65nm CMOS technology for HL-LHC upgrades of ATLAS and CMS

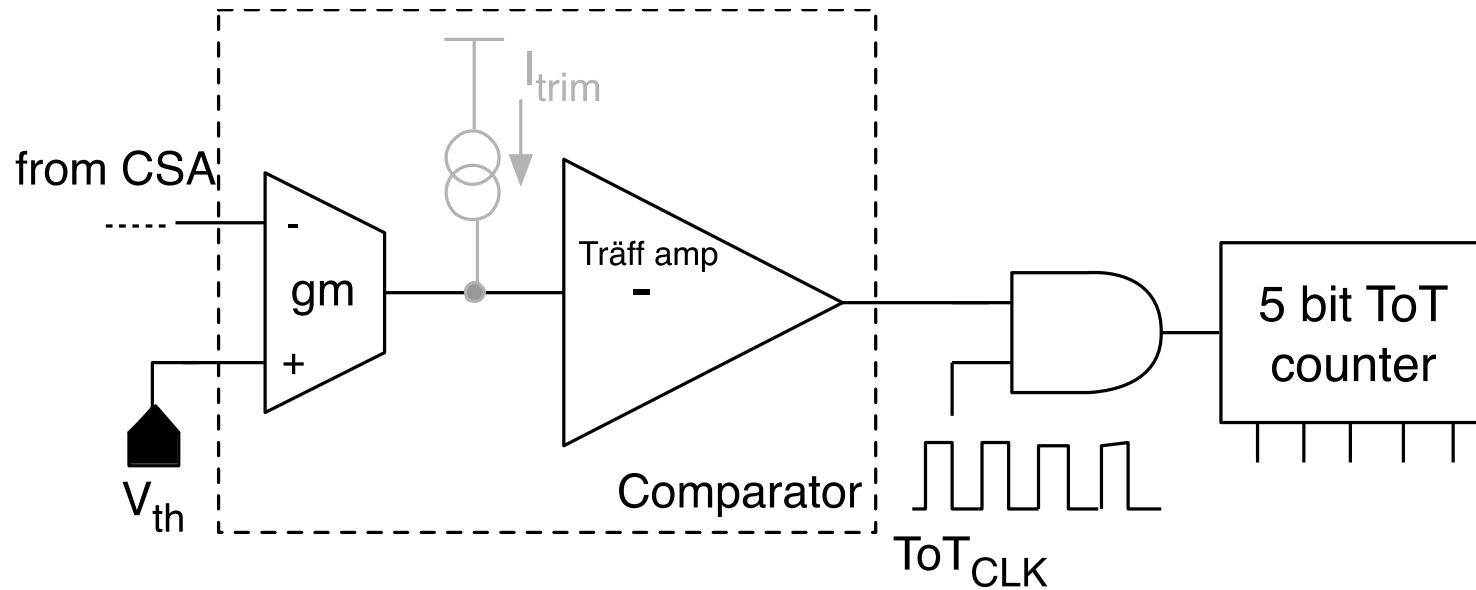
**RD53A integrates an improved version of the CHIPIX asynchronous (aka "Linear") front-end:**

- Isolation strategy: two DNWs (analog+digital) in RD53A / only analog FE in DNW in CHIPIX65
- Dedicated Krummenacher power supply  $\rightarrow$  T<sub>0</sub>T less sensitive to voltage drop on power supply lines
- Threshold tuning implemented at the transconductor output node  $\rightarrow$  V<sub>TH</sub> less sensitive to temperature and TID
- Increased charge sensitivity  $\rightarrow$  improved threshold dispersion performance
- Analog inverters for most of the configuration  $\rightarrow$  improved digital noise immunity
- In-pixel protection diodes for most of the analog bias lines





# Threshold trimming in the linear front-end of RD53A



**CHPIX65 asynchronous front-end:** tuning range completely defined by the characteristics of the trimming DAC, but threshold setting rather sensitive to temperature. Additional threshold dispersion contribution from gradients across a large chip

**RD53A linear front-end:** programmable current injected at the output of the transconductance stage of the comparator, instead of generating a threshold voltage at its input; tuning capability also depends on the transconductance of the comparator input device

# Conclusions

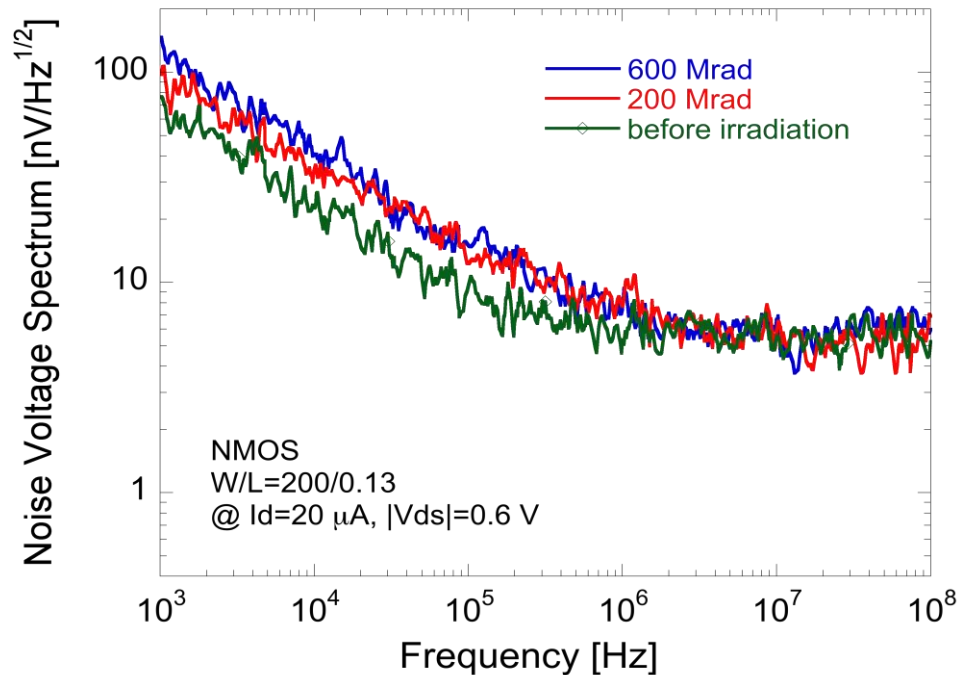
- Test results confirm that the proposed continuous-time analog front-end complies with the specifications set by RD53, in view of the development of 65 nm CMOS readout pixel chips for the innermost detector layers of ATLAS and CMS (radiation tolerance, noise, stable low threshold operation)
- This analog front-end was integrated in the large scale demonstrator chip RD53A and in an upgraded version of the CHIPIX65 demo chip; test results will be discussed in the RD53A talk by F. De Canio
- An evaluation of different front-end architectures is required for the next step: the design of the actual chip for the HL-LHC experiments

# Backup slides

<b>RD53A specifications</b> [ <a href="#">CERN-RD53-PUB-15-001</a> ]	
<i>Technology</i>	65 nm CMOS
<i>Pixel size</i>	50 x 50 $\mu\text{m}^2$
<i>Pixels</i>	192 x 400 = 76800 (50% of production chip)
<i>Detector capacitance</i>	< 100fF (200fF for edge pixels)
<i>Detector leakage</i>	< 10nA (20nA for edge pixels)
<i>Detection threshold</i>	< 600e <sup>-</sup>
<i>In-time threshold</i>	< 1200e <sup>-</sup>
<i>Noise hits</i>	< 10 <sup>-6</sup>
<i>Hit rate</i>	< 3 GHz/cm <sup>2</sup> (75 kHz avg. pixel hit rate)
<i>Trigger rate</i>	Max 1 MHz
<i>Trigger latency</i>	12.5 $\mu\text{s}$
<i>Hit loss at max hit rate (in-pixel pile-up)</i>	≤ 1%
<i>Charge resolution</i>	≥ 4 bits ToT (Time over Threshold)
<i>Readout data rate</i>	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
<i>Radiation tolerance</i>	500Mrad, 1 x 10 <sup>16</sup> 1Mev eq. n/cm <sup>2</sup> at -15 °C
<i>SEU affecting whole chip</i>	< 0.05/hr/chip at 1.5GHz/cm <sup>2</sup> particle flux
<i>Power consumption at max hit/trigger rate</i>	< 1W/cm <sup>2</sup> including SLDO losses
<i>Pixel analog/digital current</i>	4 $\mu\text{A}$ / 4 $\mu\text{A}$
<i>Temperature range</i>	-40°C ÷ 40°C

# 65 nm NMOSFETs - up to 600 Mrad low current density

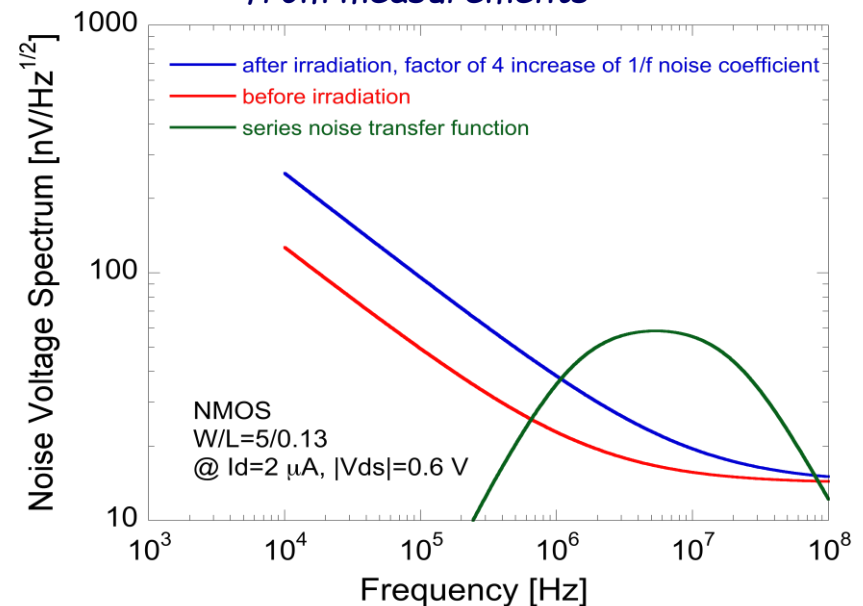
- Moderate  $1/f$  noise increase, no increase in the white noise region is detected
- The behavior as a function of the current density is different at high TID, as compared to 10 Mrad
- At 200 Mrad (and even 600 Mrad), at low  $I_D$   $1/f$  noise increase with respect to pre-irradiation values is smaller than at 10 Mrad



## Ionizing radiation effects on the signal-to-noise ratio in a pixel readout channel

- The noise data reported here can provide the basis to **estimate the performance of an analog front-end for pixel detectors at extremely high TID**
- **Even at a signal peaking time of 25 ns, radiation-induced 1/f noise increase has an effect** in the bandwidth of an analog channel (input transistor operates at very small  $I_D$ , in the low current density region)
- Using realistic parameters for **65nm CMOS pixel front-end prototypes** developed in the frame of RD53, a **15 - 20% ENC increase** (from 120 to 140  $e$  rms at 100 fF  $C_D$ ) can be predicted, which is consistent with measurements on irradiated chips

Noise voltage spectrum of NMOS,  $W/L = 5/0.13$ , before irradiation and at 600 Mrad TID, calculated using data from measurements



*Transfer function of a shaperless front-end with 25 ns peaking time superimposed to the spectra*