The RD53A pixel front-end chip: design and test results

Francesco De Canio[a,b]

On behalf of the RD53 Collaboration

[a]University of Bergamo

[b]INFN Pavia

Acknowledgment to

AIDA 2020

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http://aida2020.web.cern.ch/

2018 Front-End Electronics

May 20-25, Orford, Canada

The RD53 Collaboration

RD53 is a collaboration among ATLAS-CMS communities for the development of LARGE scale pixel chips for ATLAS/CMS phase-2 upgrades

24 Institutions from Europe and USA:
Annecy-LAPP, Aragon, Bergen, Bonn, CERN, FH-Dortmund, FNAL, INFN (Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino), LBNL, Marseille-CPPM, New Mexico, NIKHEF, Orsay-LAL, Paris-LPNHE, Prague IP-FNSPE-CTU, RAL-STCF, Sevilla, Santa Cruz

RD53 goals:

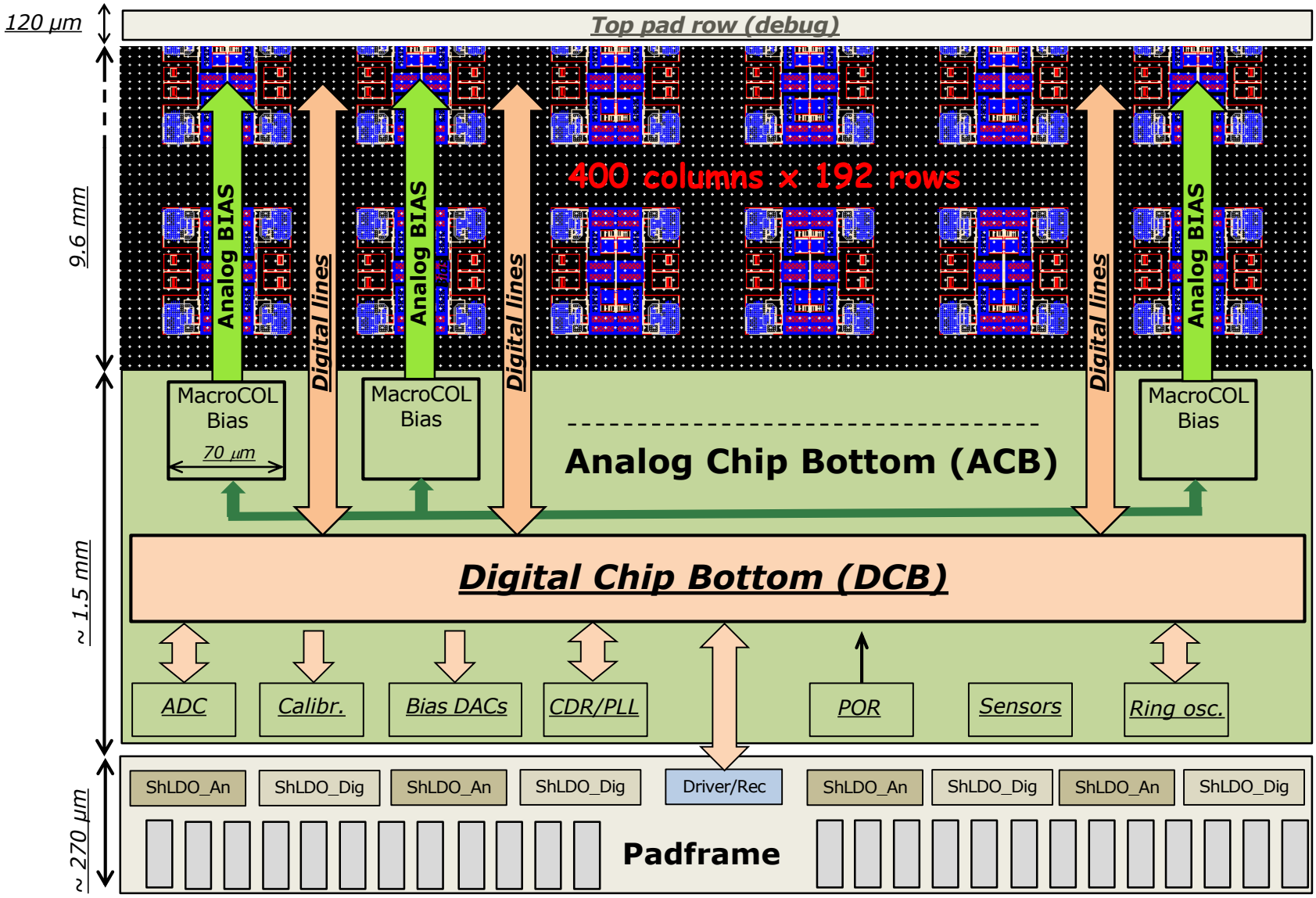
- detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
- Development of **tools and methodology** to efficiently design large complex mixed signal chips
- Design of a **shared rad-hard IP library**
- Design and characterization of **full sized pixel array chip**

RD53A - Large Scale prototype

- The efforts of the RD53 collaboration led to the submission of the RD53A chip
- 400 x 192 pixel, 50um x 50um pixel, 20mm x 11.5mm chip
- **Goal**: demonstrate in a large format IC
  - suitability of 65nm technology (including radiation tolerance)
  - high hit rate: 3 GHz/cm^2
  - trigger rate: 1 MHz
  - Low threshold operation with chosen isolation strategy and power distribution
- Submitted at the end of August 2017
  (shared engineering run with CMS MPA/SSA and other test chips for cost sharing)

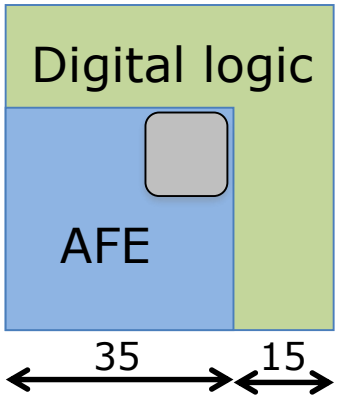
- **Not intended to be a production chip**
  - contains design variations for testing purposes (with 3 different versions of the analog very front-end)

RD53A floorplan



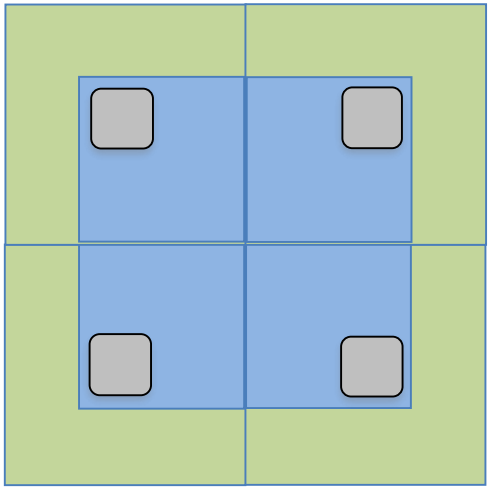
RD53A Pixel floorplan

- 50% Analog Front End (AFE) - 50% Digital cells



The "analog island" concept

A "quad"



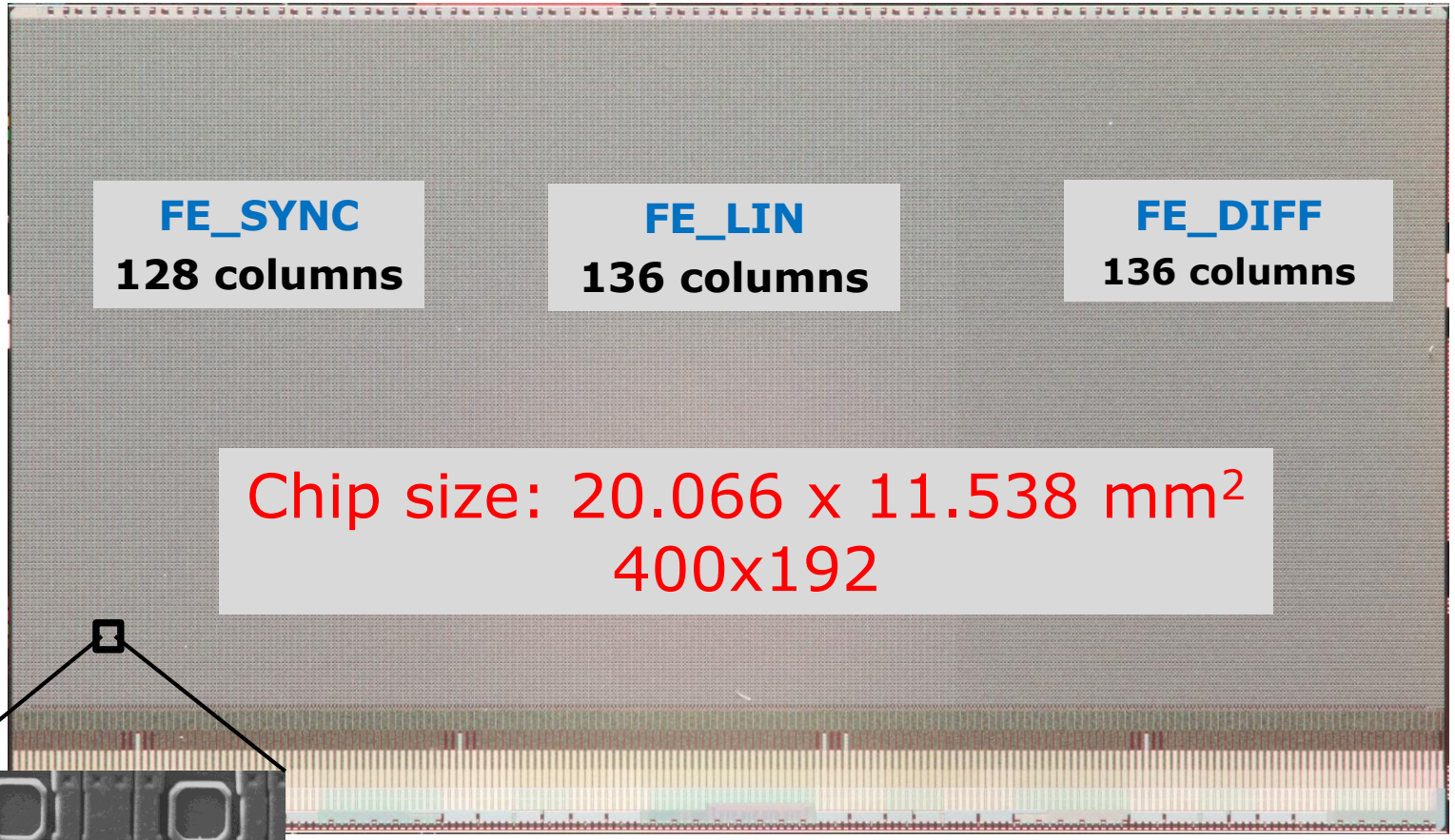
- The pixel matrix is built up of **8x8 pixel cores** → 16 analog islands (quads) embedded in a flat digital synthesized sea
- One Pixel Core contains multiple Pixel Regions and some additional arbitration and clock logic
- Pixel Regions share most of logic and trigger latency buffering

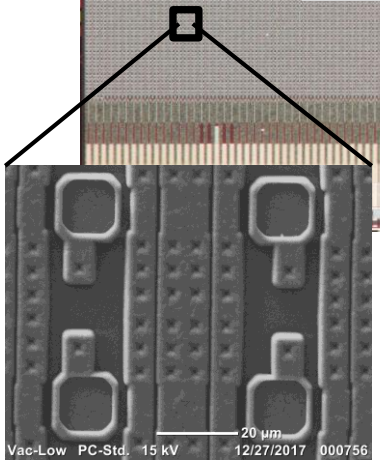
↙ ↘

Distributed Buffering Architecture (FE65_P2 based):
- distributed TOT storage
- Integrated with Diff and Lin FE

Centralized Buffering Architecture (CHIPIX65 based (4x4)):
- centralized TOT storage
- Integrated with Synch FE

RD53A - Large Scale prototype



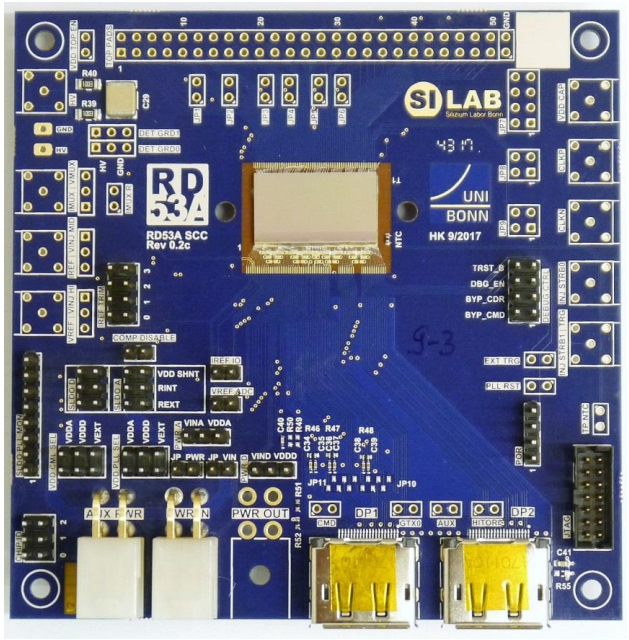


- Submitted on 31st August 2017
- First diced chips received in Bonn 06.12.2017
- > 50 chips loaded on PCBs and under test
- Apr. 13, 2018: First bump-bonded chip test

RD53A testing plans #1

- Two test systems:
  - BDAQ53 – Bonn University https://gitlab.cern.ch/silab/bdaq53
  - YARR – LBNL https://gitlab.cern.ch/YARR/YARR
    https://gitlab.cern.ch/YARR/YARR-FW

RD53A chips assembled on a SCC (designed in Bonn)



- Functional testing of RD53A (on-going)
- Debugging of test systems (now): improvements in software, firmware, hardware
- Distribution of setups across collaboration has started
- RD53A will be integrated into DAQ/testbeam framework of the experiments

Weekly RD53A testing meetings with latest test results, where anybody from ATLAS and CMS pixel communities can join in

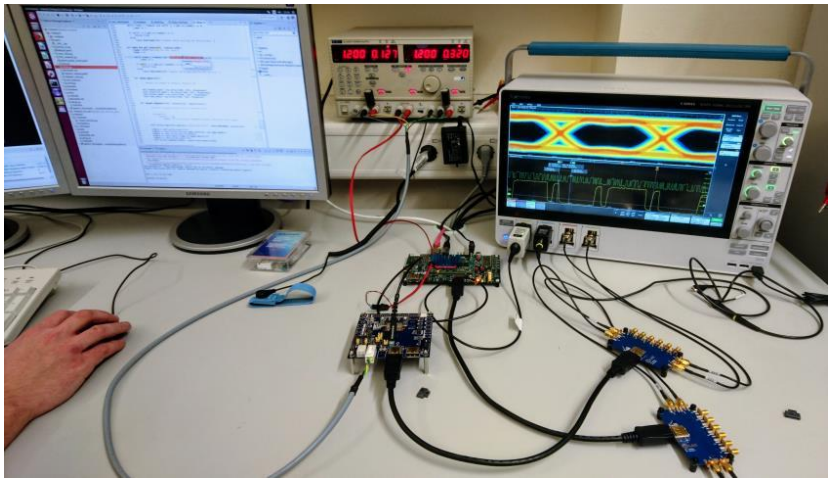
RD53A testing plans #2

- Radiation campaigns in different sites
  - Irradiation with X-rays @ CERN (March 2018: done, next period t.b.d.)
  - Low dose rate X-rays irradiation (May-June)
  - Gammas, protons, low-dose betas, all being planned
- Serial powering tests
- Wafer probing:
  - Bonn: developed a needle card for RD53A wafers
  - LBNL: also doing trials with their wafer prober
  - CERN: will get a copy of the Bonn needle card for CERN wafer prober
  - INFN-Torino: later
- Bump-bonding with first sensors:
  - 3 wafers under processing at IZM for bump-bonding to CMS and ATLAS sensors (April 2018)

Needle card for wafer probing (developed in Bonn)

RD53A measurements

- Preliminary results shown in next slides are from measurements performed by:
  - Bonn University
  - CERN
  - INFN Torino
  - LBNL
  - FH-DORTMUND

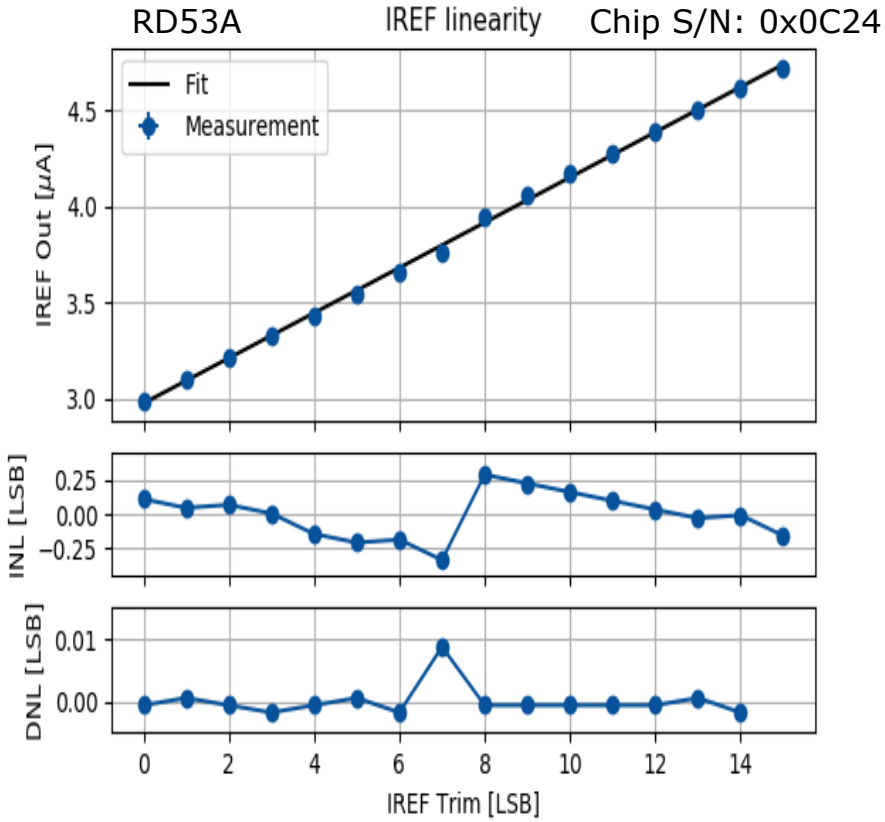


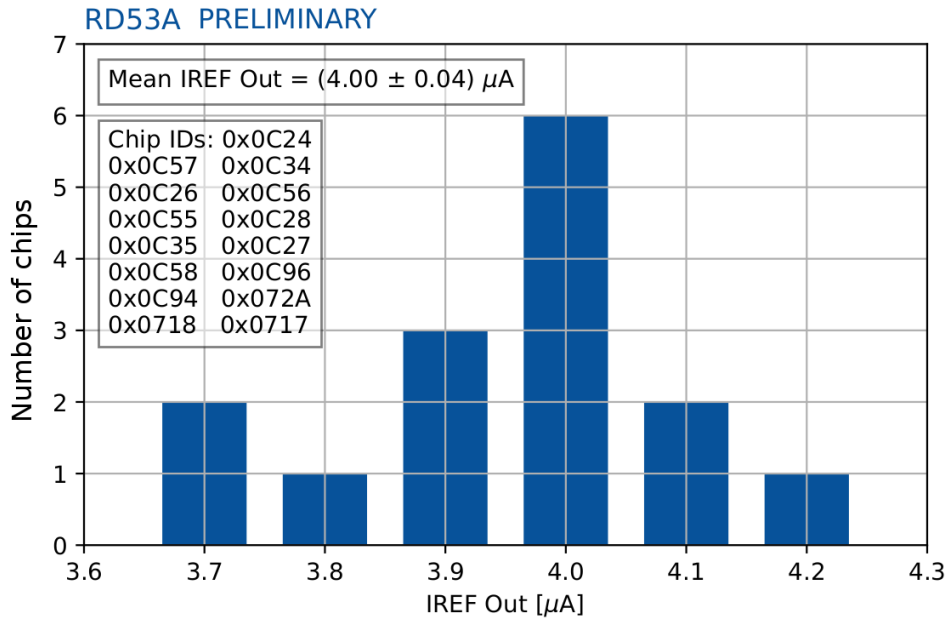
- **The chip is fully operating using its normal I/O ports**
  - 160 Mbps CMD input (LVDS) → Clock + Data
  - CML output (Aurora link)

  - PLL locks
  - Aurora link is stable (single link @ 1.28 Gbps)
  - Command decoder responds → We can configure and readout the chip

IREF measurement and trimming

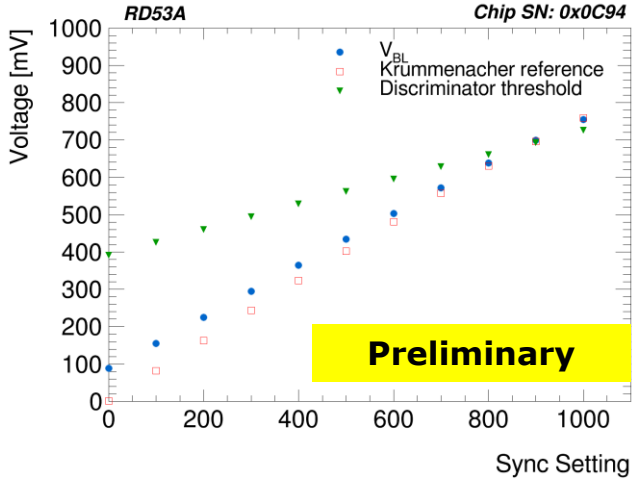
- All biases provided by internal current DACs, using an internally generated reference current IREF (4 μA nominal) derived by a Bandgap Reference circuit (independent from T, tolerant to TID)
- To compensate for process variations, we can tune IREF by means of 4-bit DAC set by hard-wired connections
- 10 chip average is 3.99 μA (expected 4 μA)

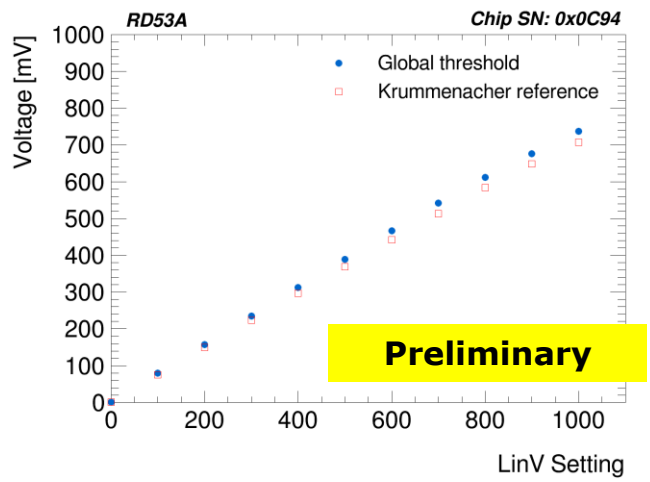


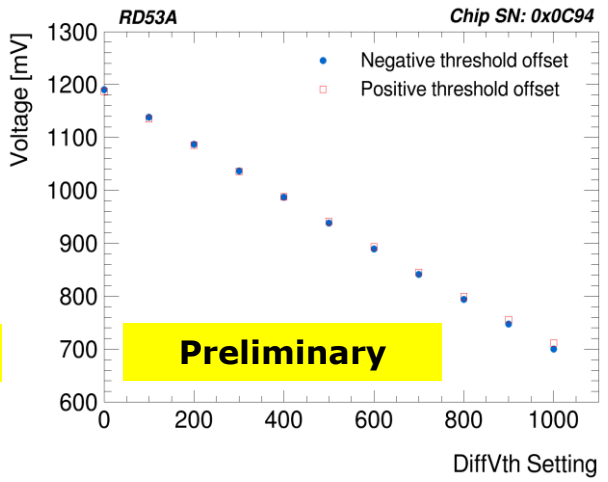


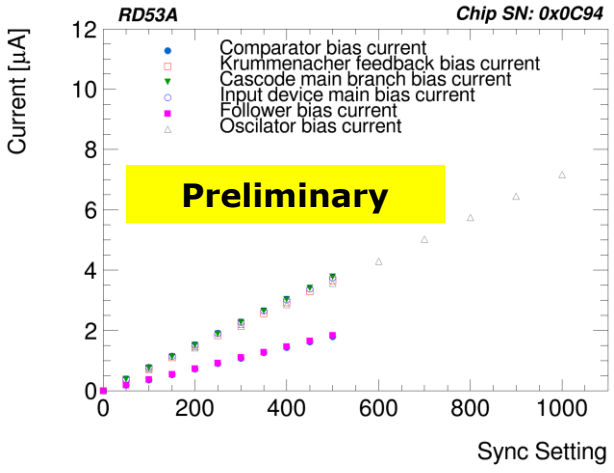
Scan of Bias 10-bit DACs

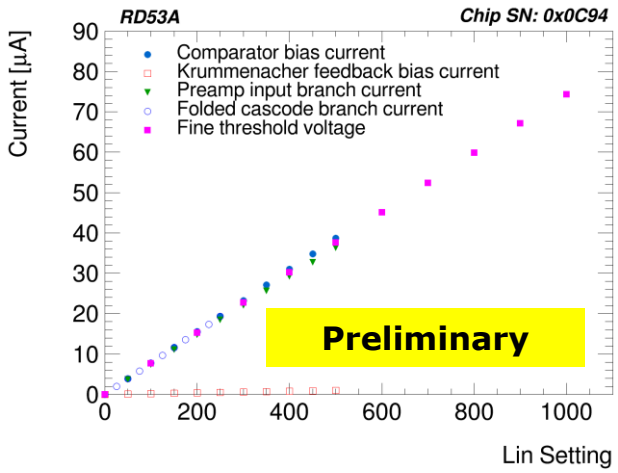
- All internal bias currents and voltages can be monitored using internal 12-bit ADC and can be accessed on two multiplexed outputs: IMUX and VMUX (used also for ADC calibration)
- Voltages on top row, currents on bottom row

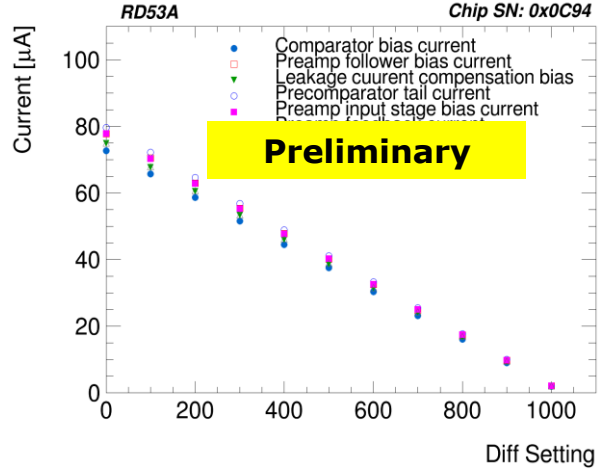






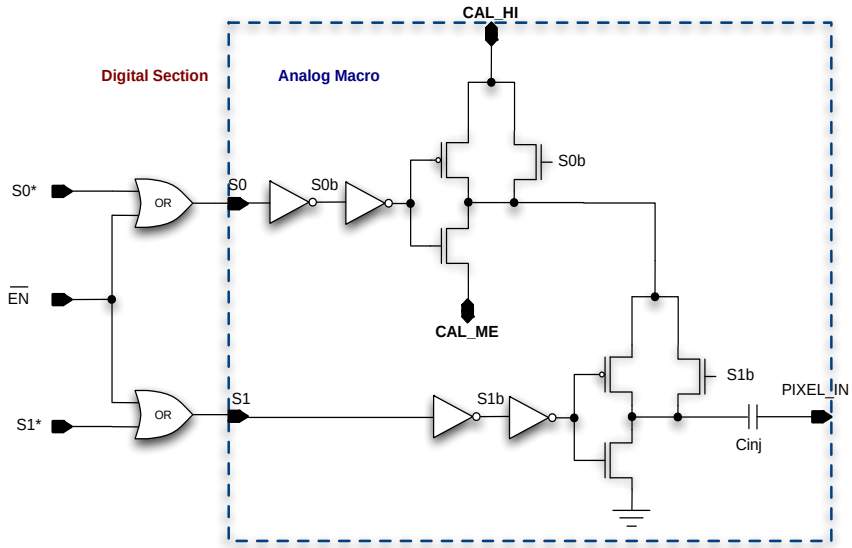


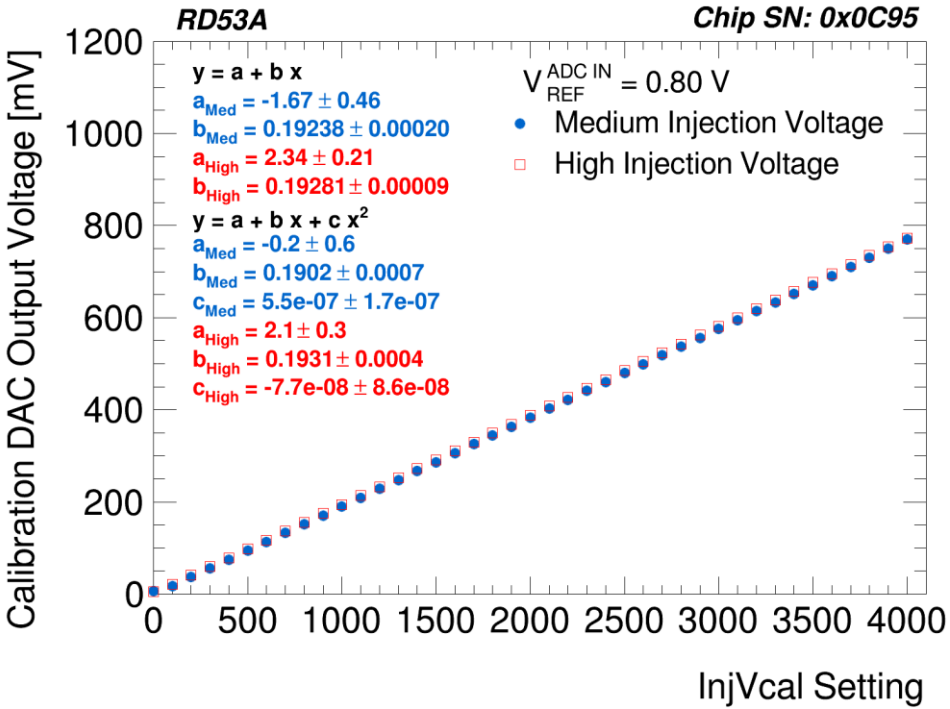




Calibration circuit (in-pixel)

- Local generation of the analog test pulse starting from 2 defined DC voltages CAL_HI and CAL_MI distributed to all pixels and a 3rd level (local GND)
- Two operation modes which allow to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time

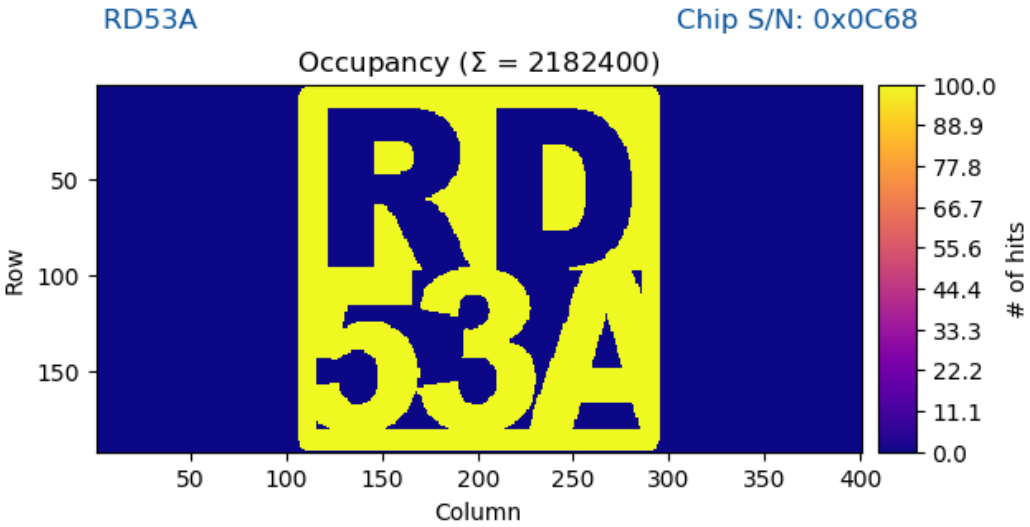


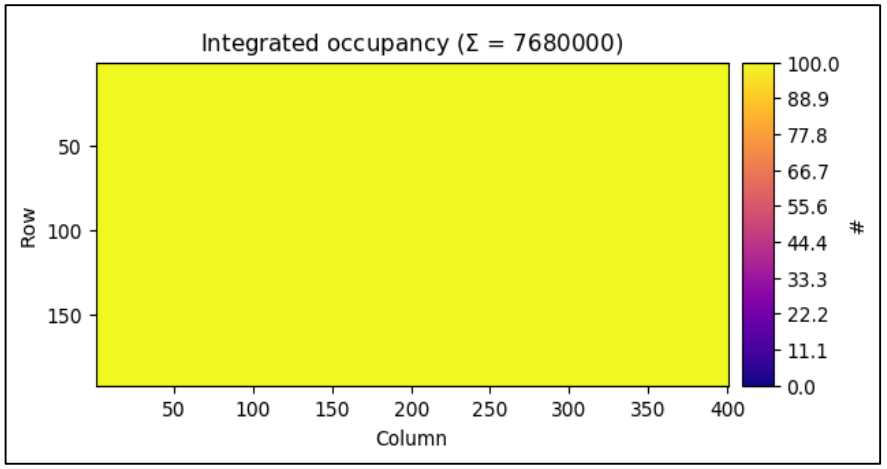


- **Injection DACs fully functional**
- Assuming 8.5fF in-pixel injection cap -> 10.08 e-/DAC
  - Close to simulation results (~11 e-/DAC)
- All biasing DACs (can be monitored using internal 12-bit ADC and are accessible on a dedicated pad) work fine

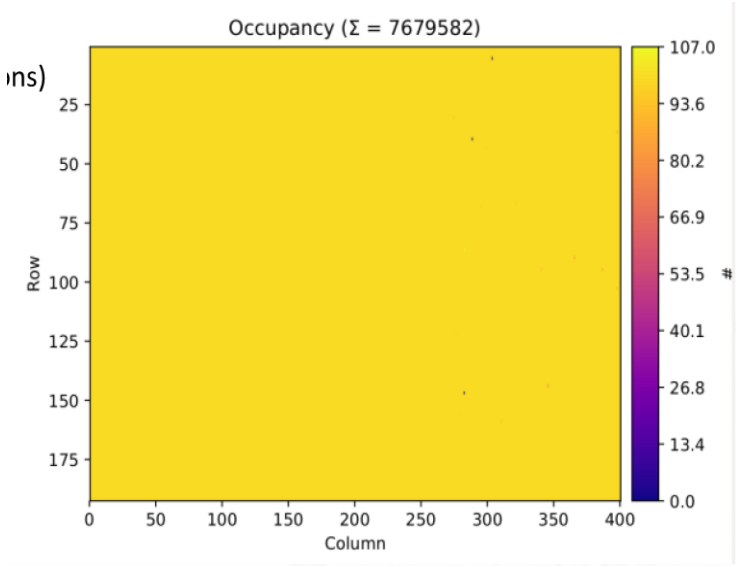
Digital and Analog scan (all FE flavours)

- Digital scan



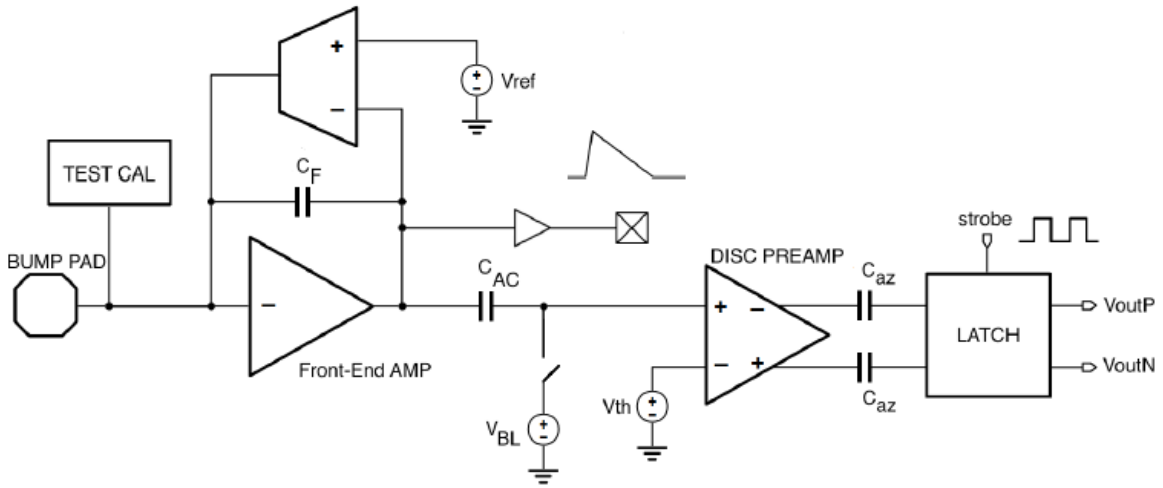


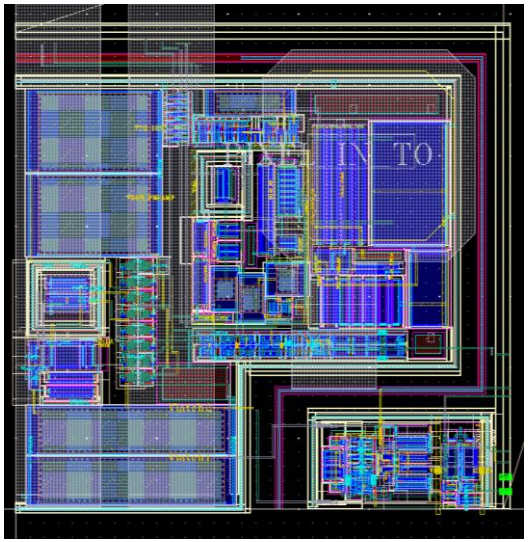
- Complex masking implemented
- Full chip responds



- Analog scan
- Full chip responds
- High injection (30 ke-)

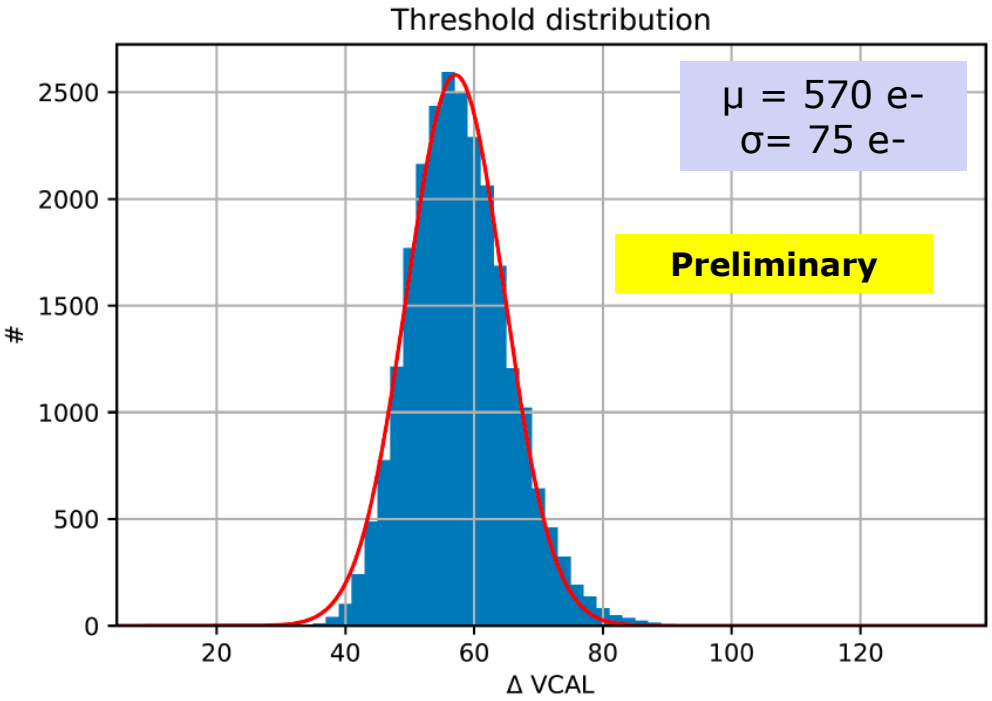
Synchronous Analog Front-end

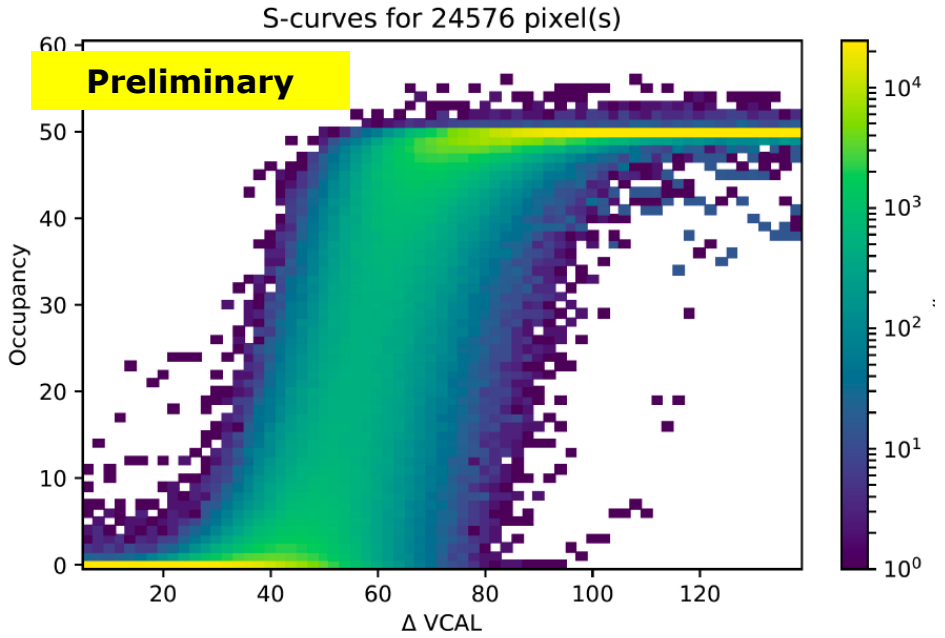


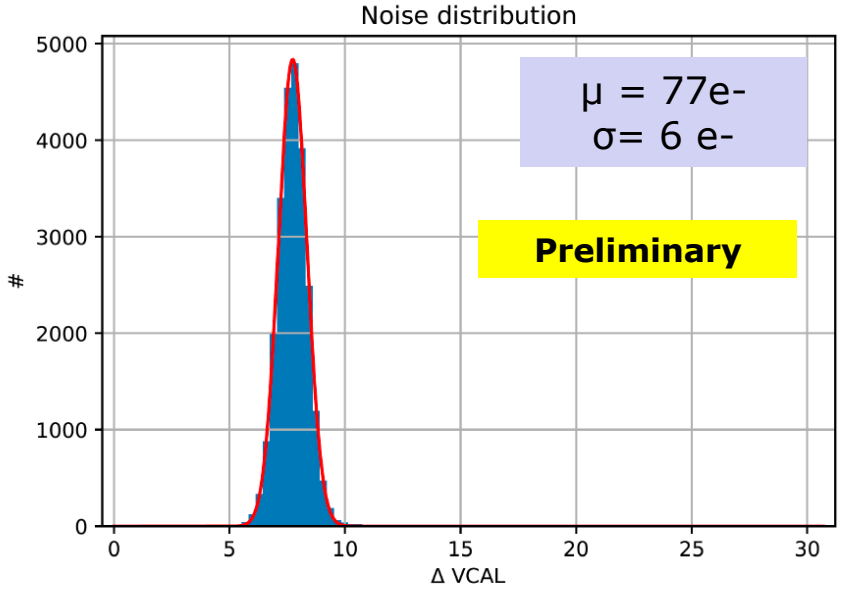


- **Telescopic cascode CSA** with **Krummenacher** feedback for linear ToT charge encoding
- **Synchronous discriminator**, AC coupled to CSA, including offset compensated differential amplifier and latch
- Threshold trimming by means of autozeroing (no local trimming DAC)
- **Fast ToT counting** with latch turned into a local oscillator (100-900 MHz)
- **Improved version of the CHIPIX65 synchronous FE**

Synchronous Analog Front-end #1



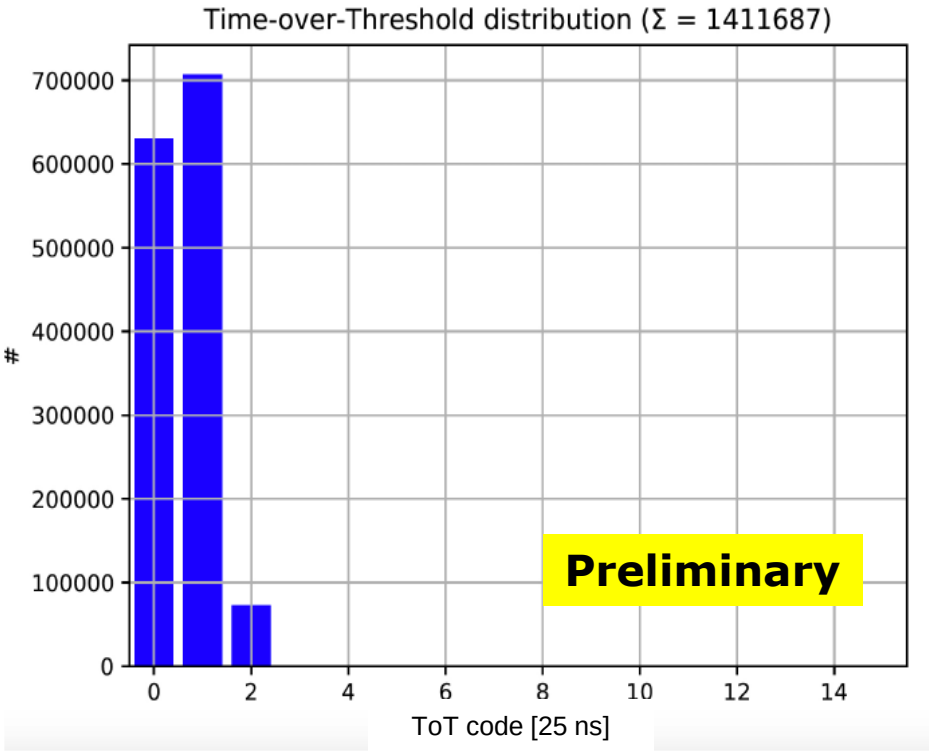




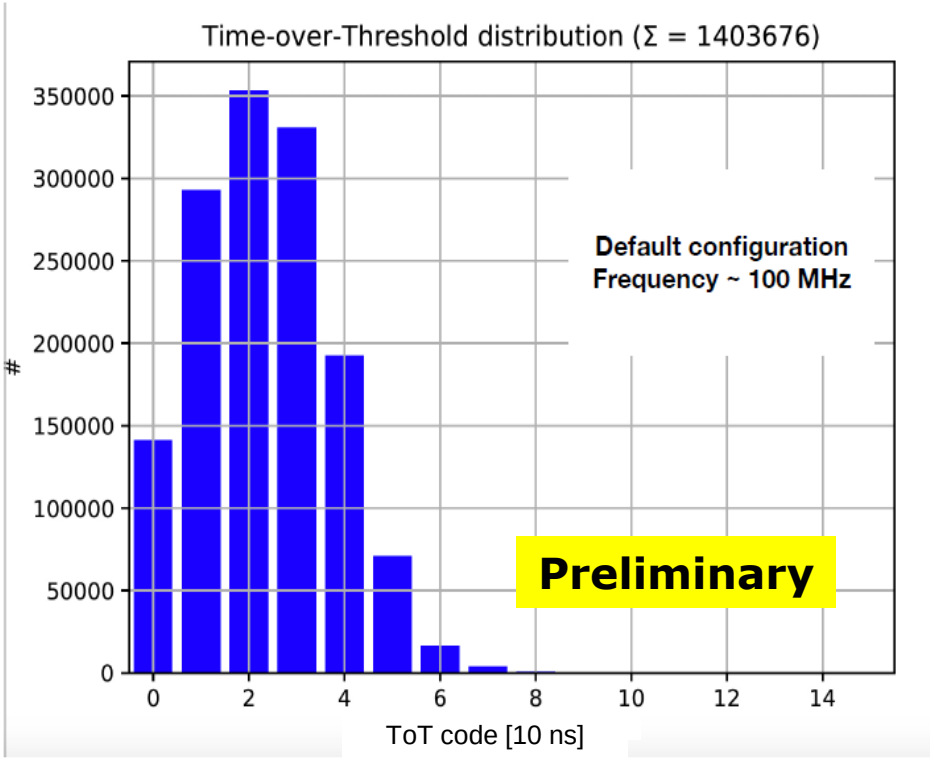
- Synchronous FE fully functional and can be operated at low threshold

Synchronous Analog Front-end #2

ToT - Without fast ToT



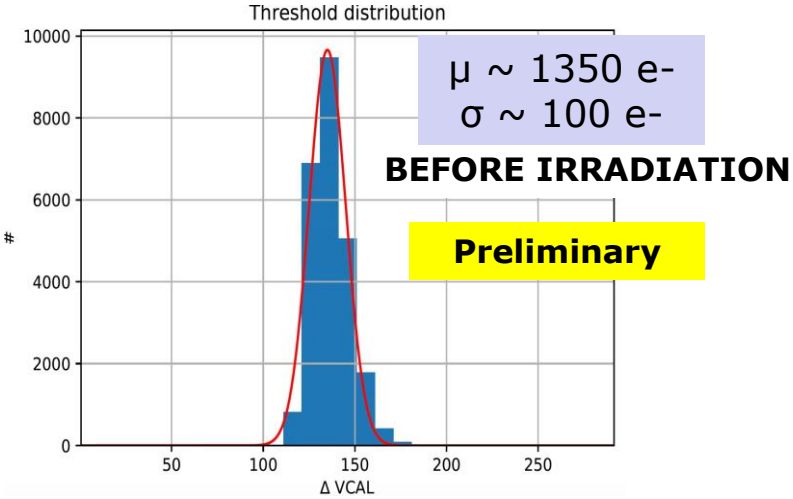
ToT - With fast ToT

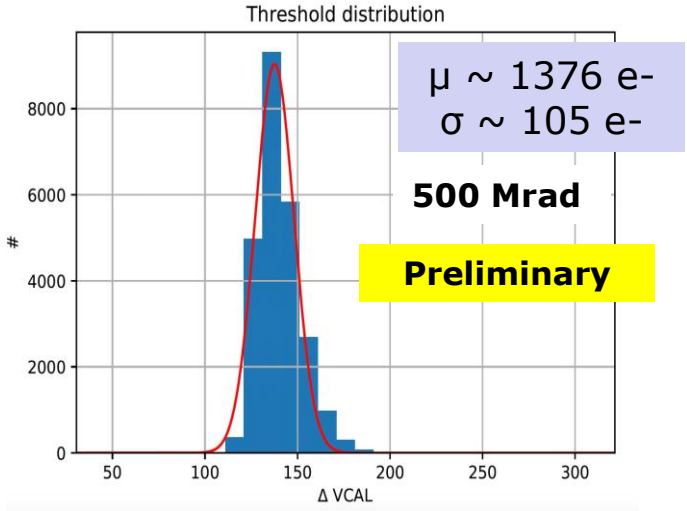


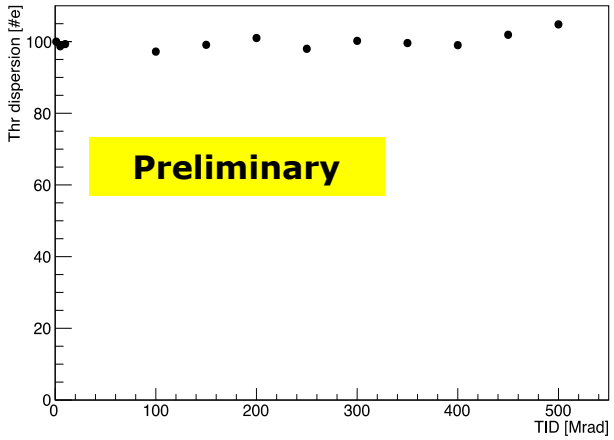
Synchronous FE irradiation test results

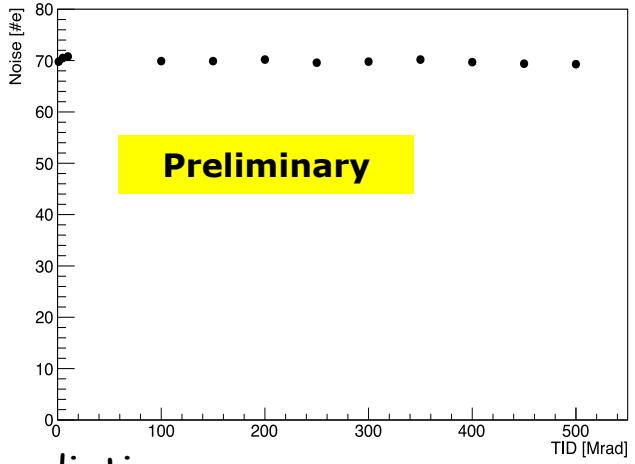
An X-ray irradiation campaign has been performed at CERN in March.

- Temperature: -10° C TID up to 500 Mrad





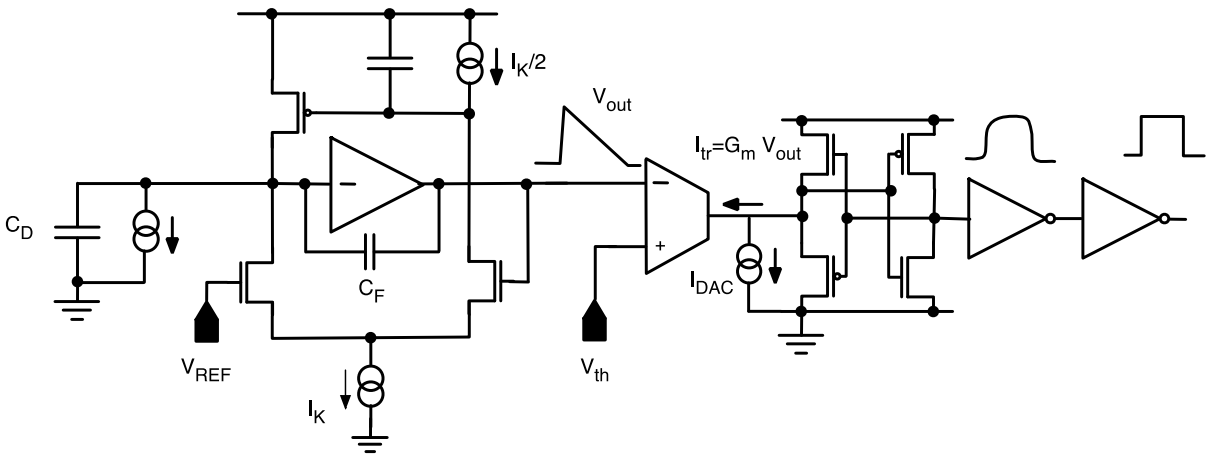


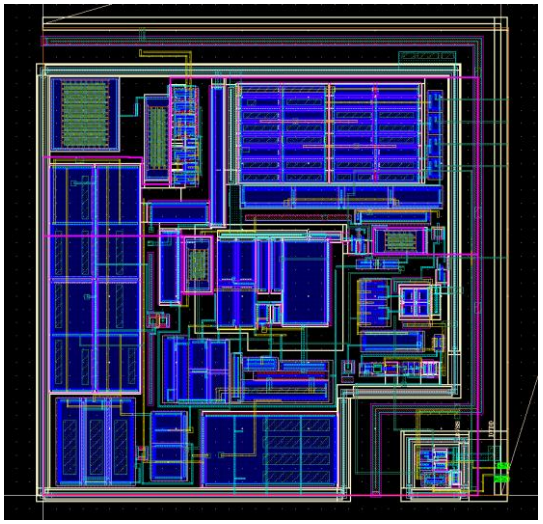


The behavior of the synch FE is very slightly modified by radiation

- The threshold dispersion increases of around 5 electrons
- The threshold mean decreases of around 25 electrons
- **Both threshold dispersion and noise do not show significant changes as a function of TID**

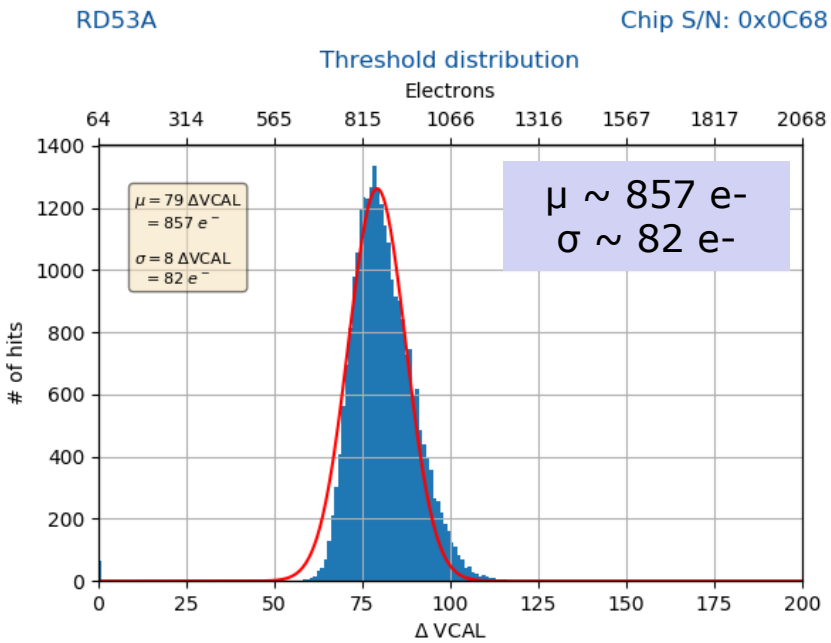
Linear Analog Front-end

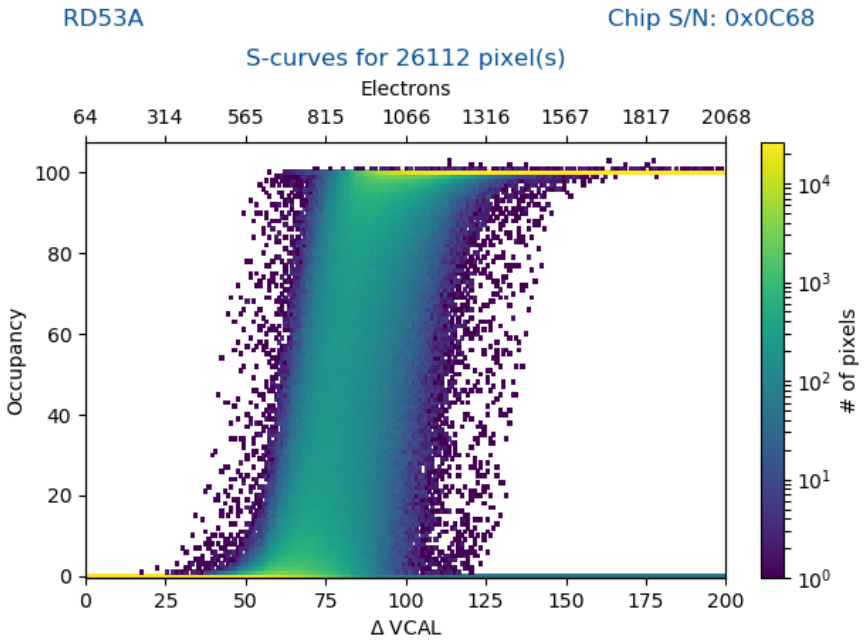


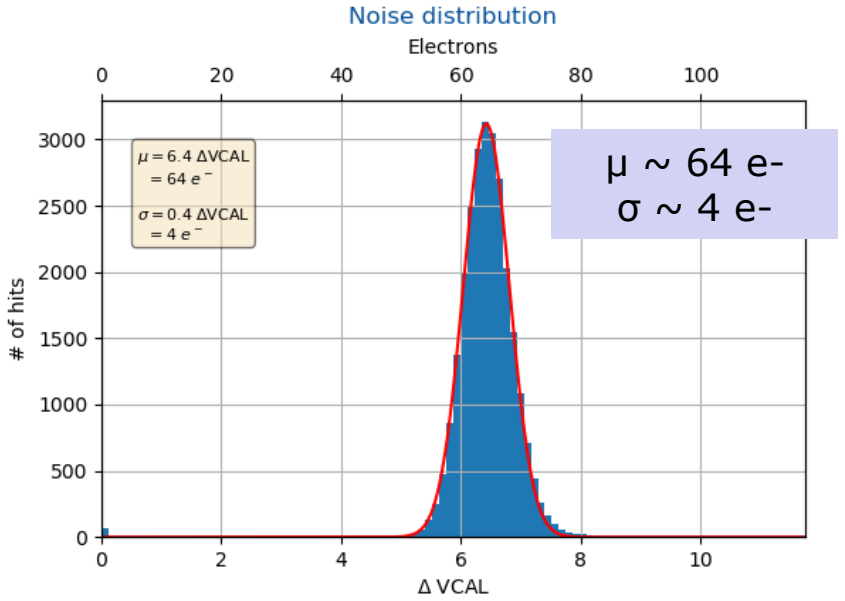


- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- High speed, low power **current comparator**
- **4 bit local DAC for threshold tuning**
- **Improved version of the CHIPIX65 asynchronous FE**

Linear Analog Front-end – Baseline/noise tuning

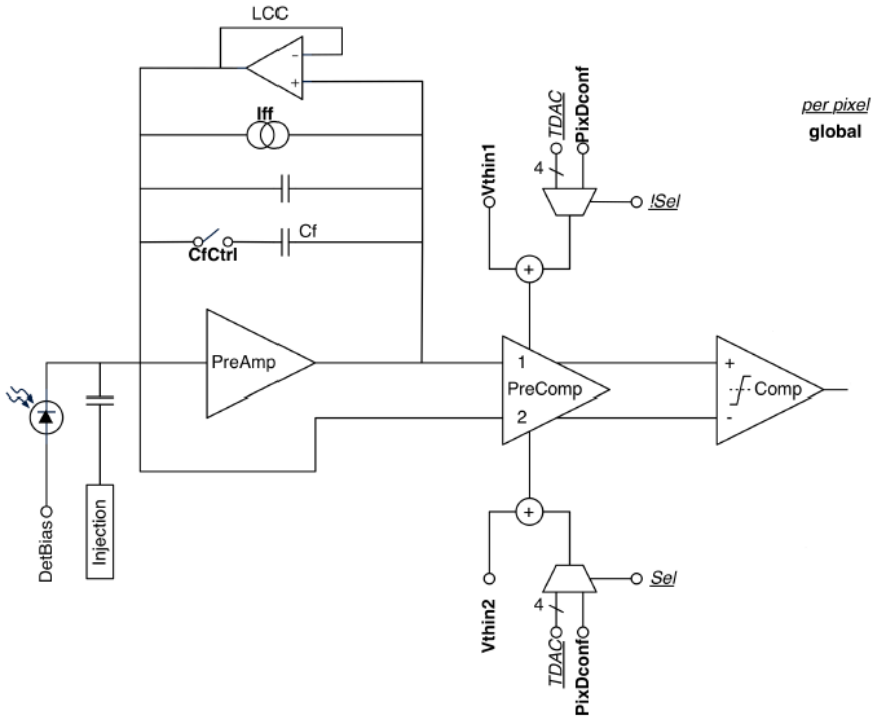


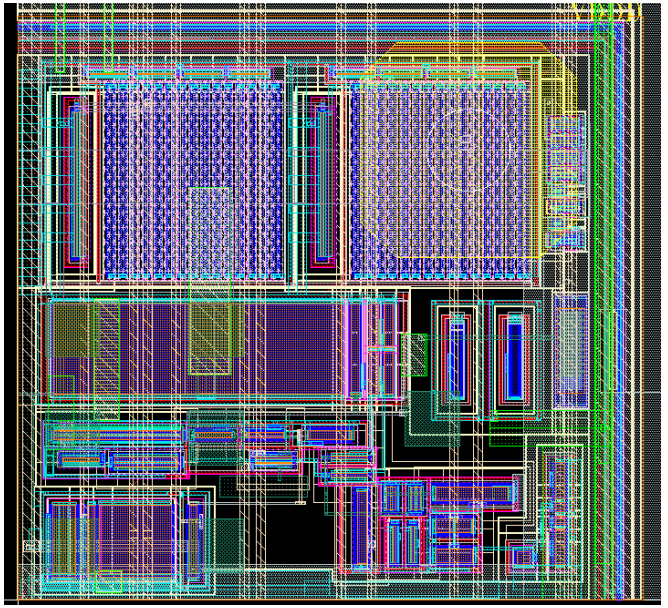




- Linear FE is fully functional
- Tuning procedure under optimization
- ENC ~ 64 e- rms

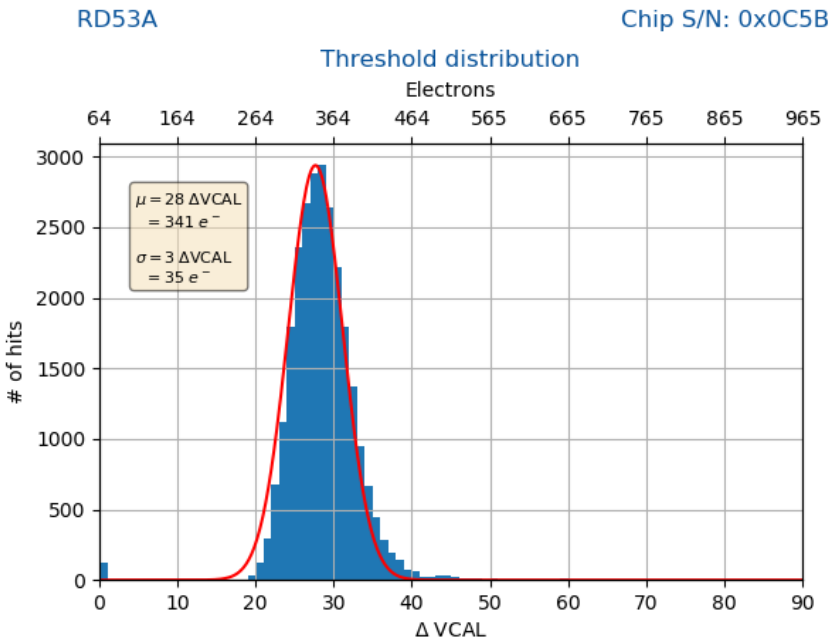
Differential Analog Front-end

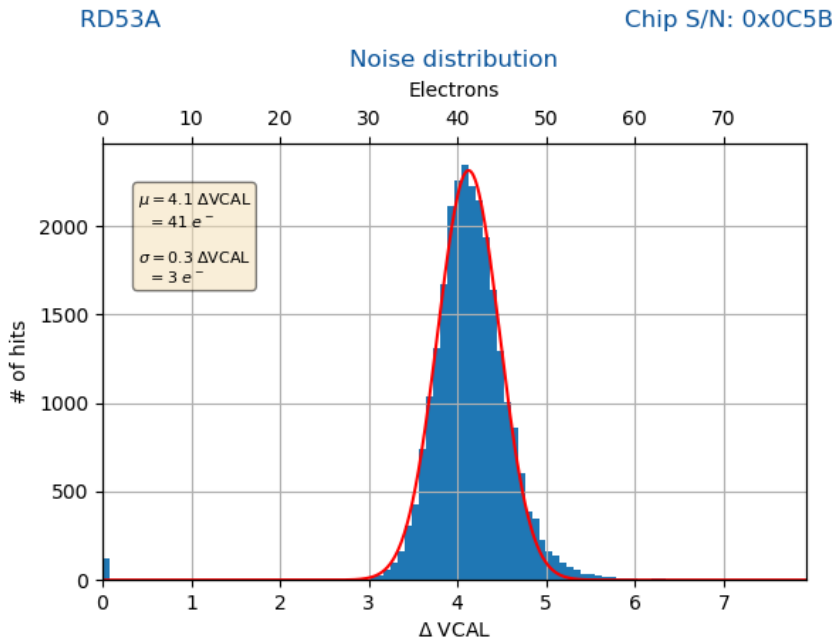




- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation** (not shown) a la FEI4
- **Threshold adjusting** with global 8bit DAC and two per pixel 4bit DACs
- Improved version of the **FE65-P2 FE**
- **Test on-going**

Differential AFE: Baseline/noise tuning



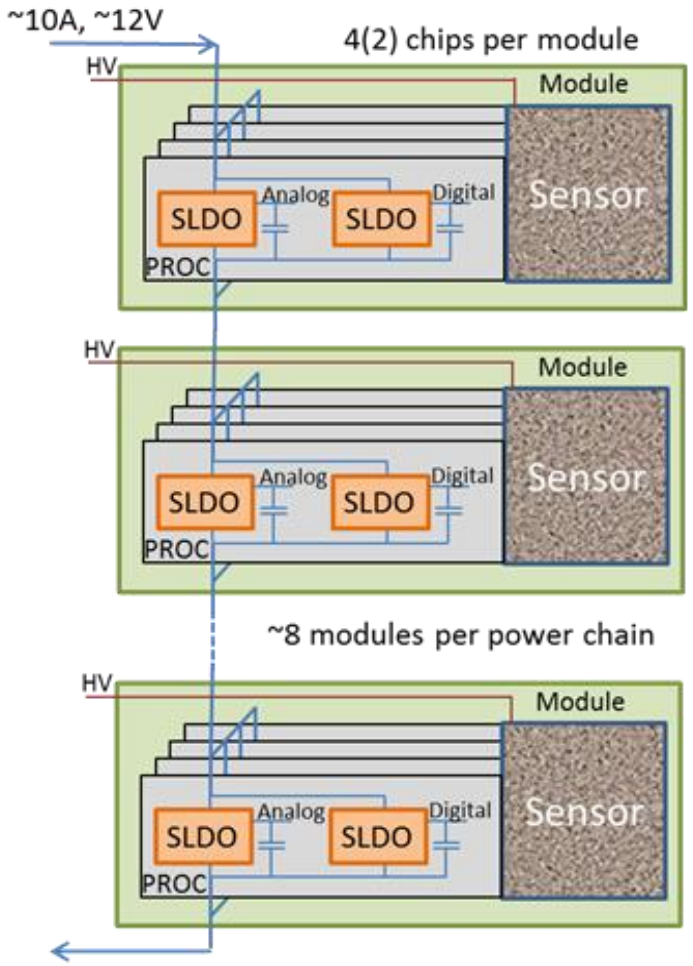


- **Bug in the A/D interface**: missing P&R constraint on the Diff. FE hit output → Varying load capacitance on comparator output → systematic variation of delay and ToT
- **This bug did not prevent the Diff FE full characterization** → Non default parameters to minimize the effect of load capacitance
- **Low threshold** achieved with **35 e- rms** threshold dispersion in **non-default configuration** → (slower wrt nominal)

Serial Powering

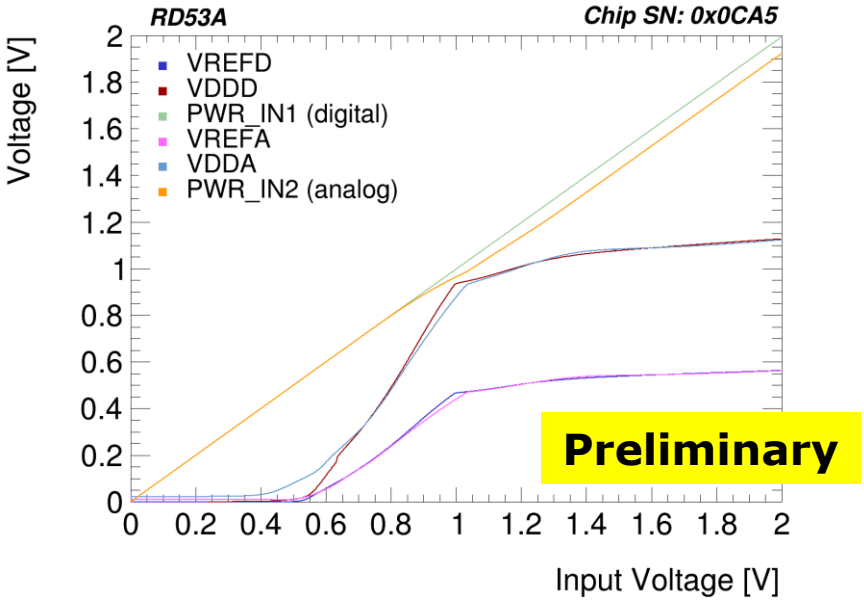
- RD53A is designed to operate with **Serial Powering** → constant current to power chips/modules in series
- Based on ShuntLDO
- Dimensioned for production chip

- **Three operation modes**:
  - ShuntLDO: constant input current Iin → local regulated VDD
  - LDO (Shunt is OFF) : external un-regulated voltage → local regulated VDD
  - External regulated VDD (Shunt-LDO bypassed)

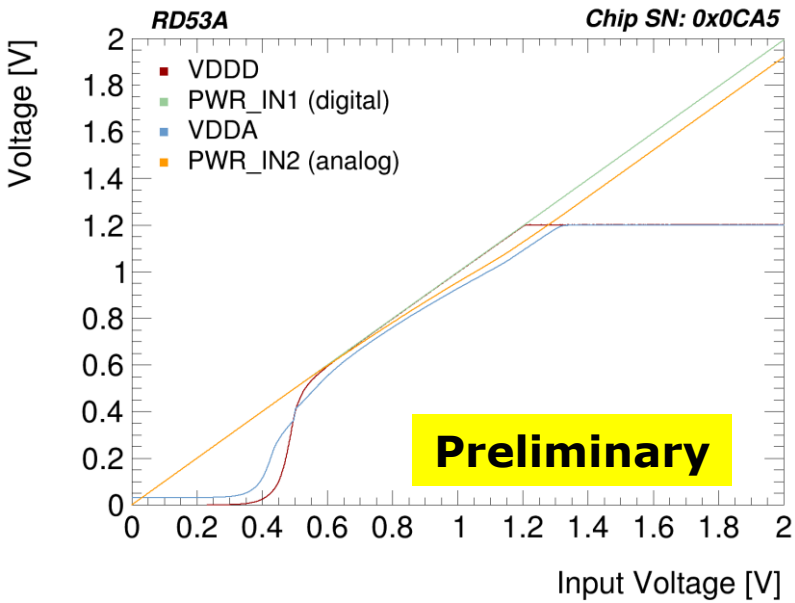


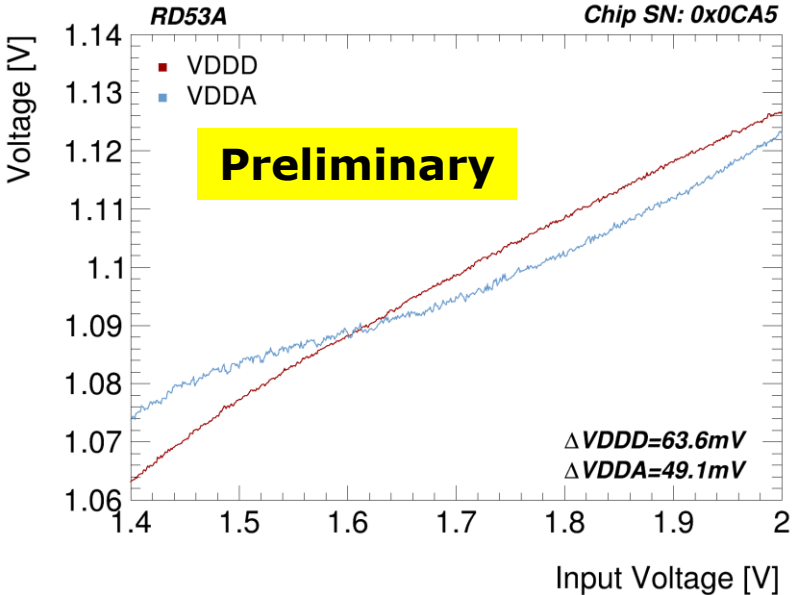
LDO: Line regulation

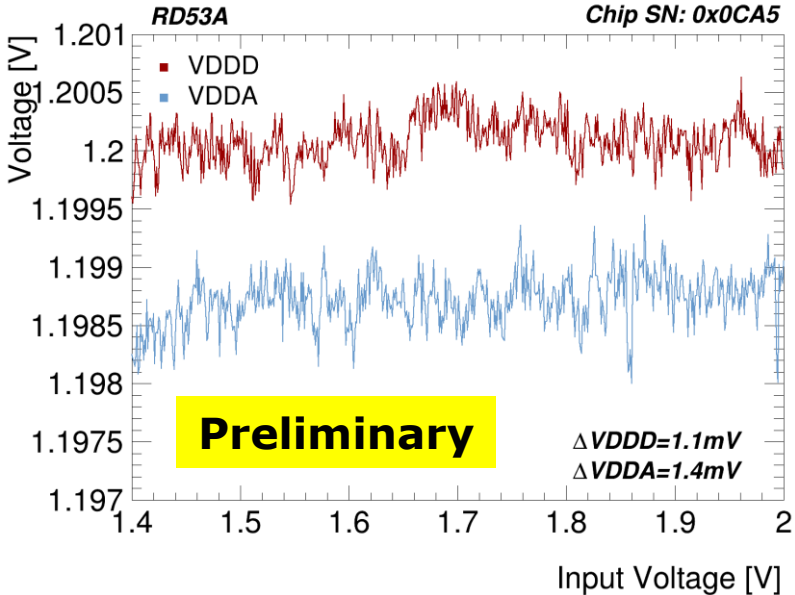
Internal VREF from BGR



External VREF =0.55 V

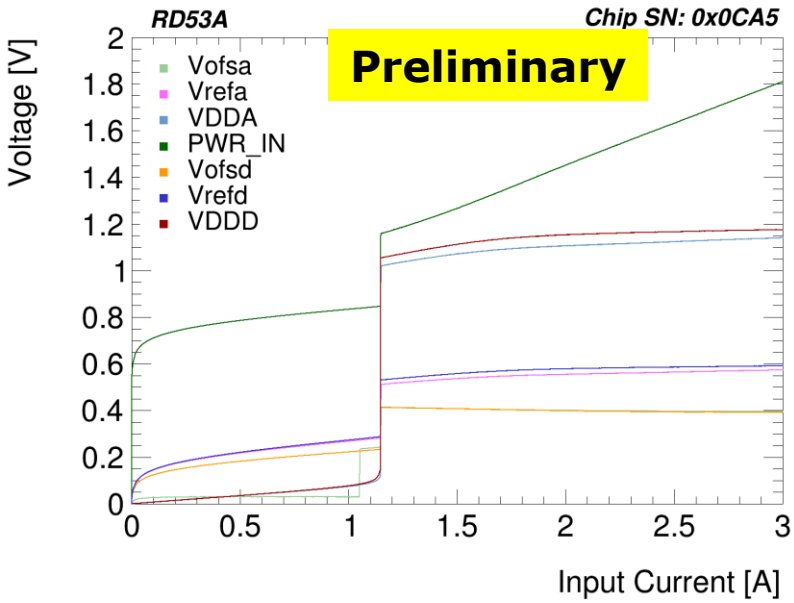




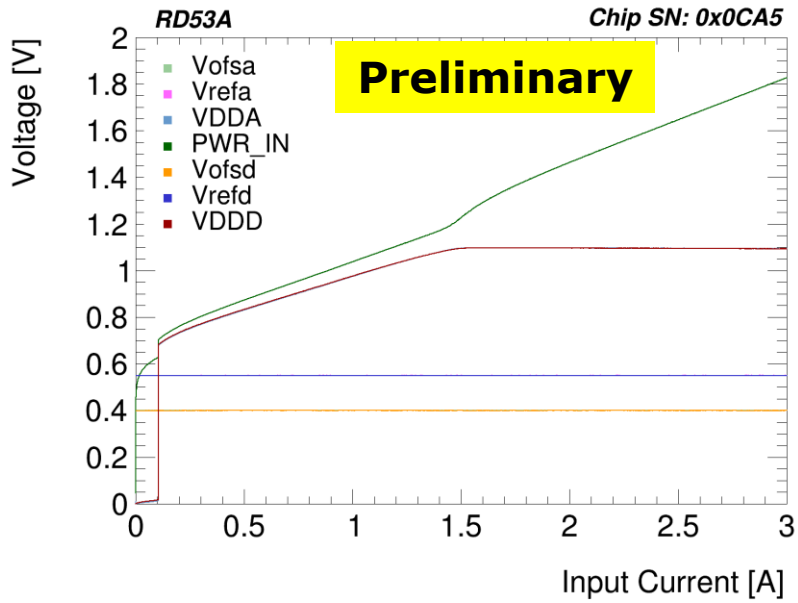


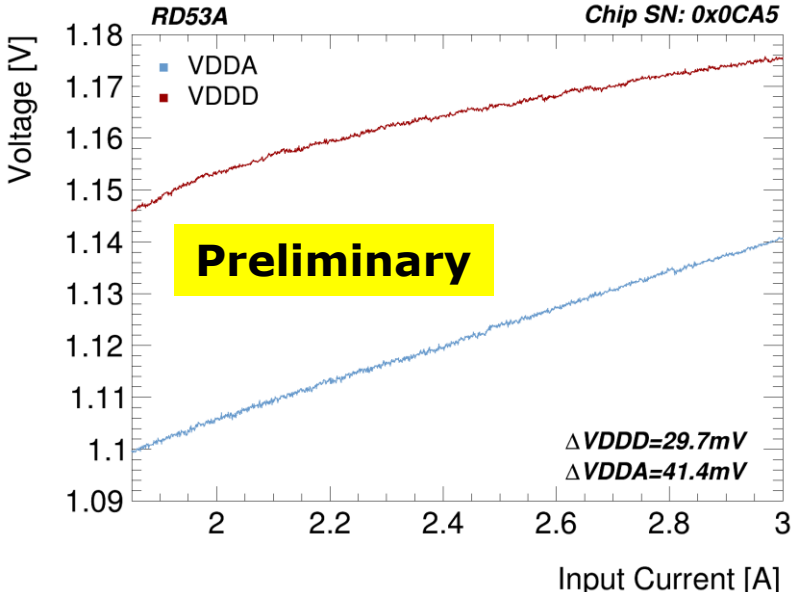
ShuntLDO: Line regulation

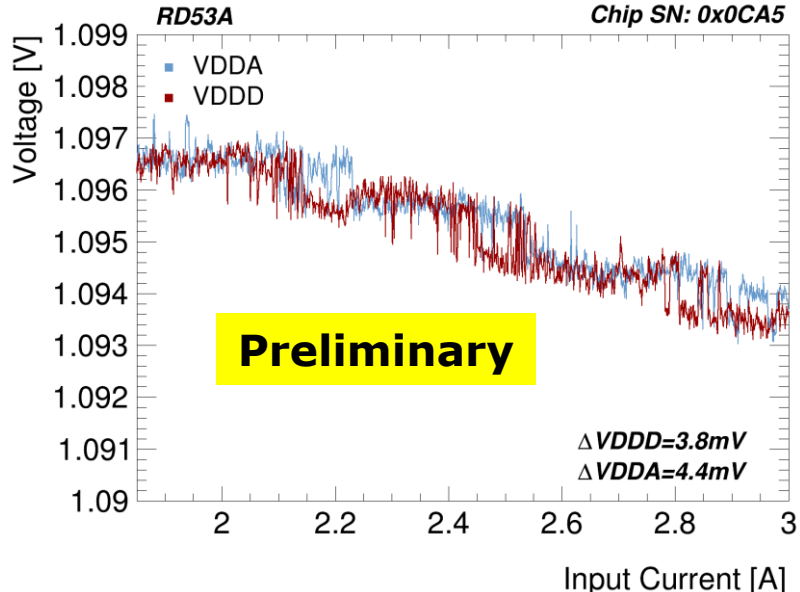
Internal VREF from BGR



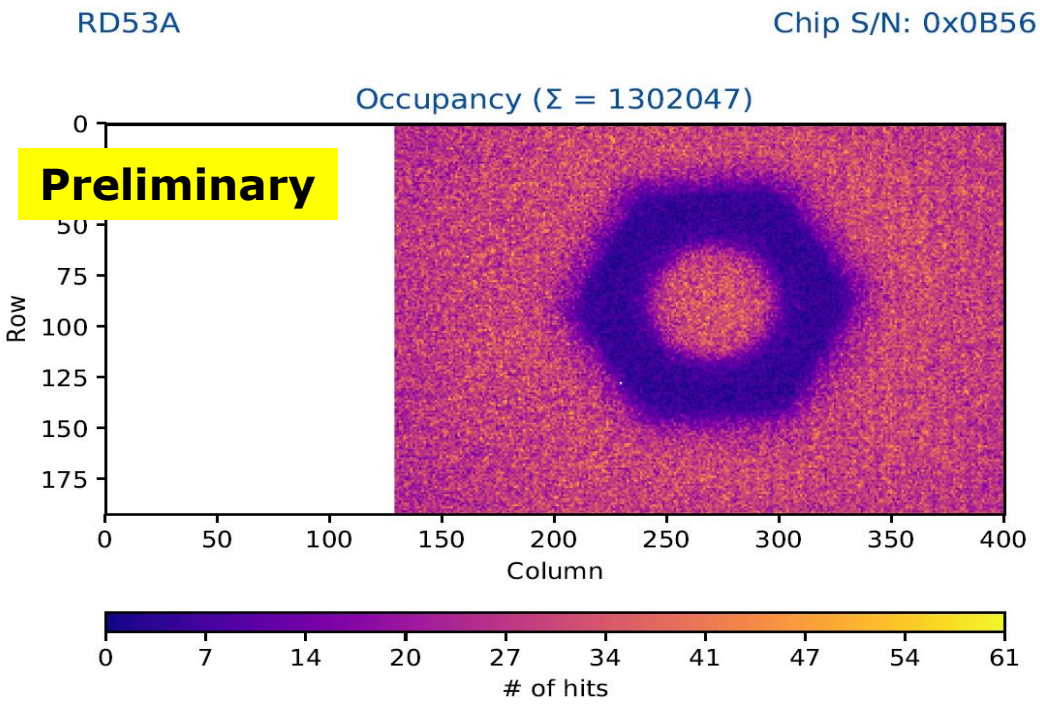
External VREF =0.55 V

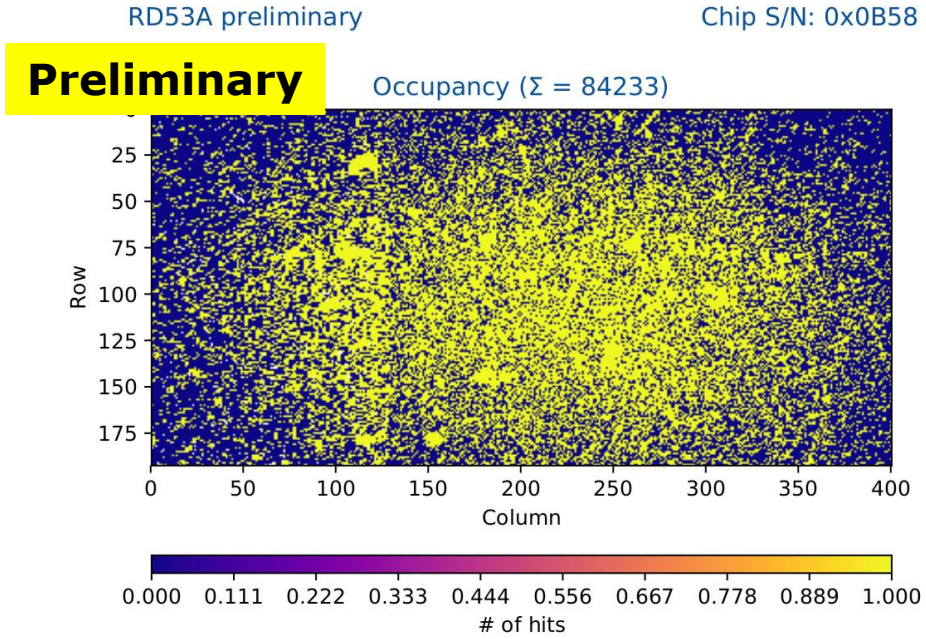






First results of RD53A with sensor





- **4 RD53A chips with sensor** arrived in Bonn on 13 April 2018
- Image of a nut placed on the sensor backside, **illuminated with Am241 source**
- Hit-OR-trigger scan, LIN and DIFF FE, both set to 3 ke- threshold, un-tuned
- Need some more FW/SW development to implement auto-zero sequence for SYNC FE

•Result of the SPS beam test

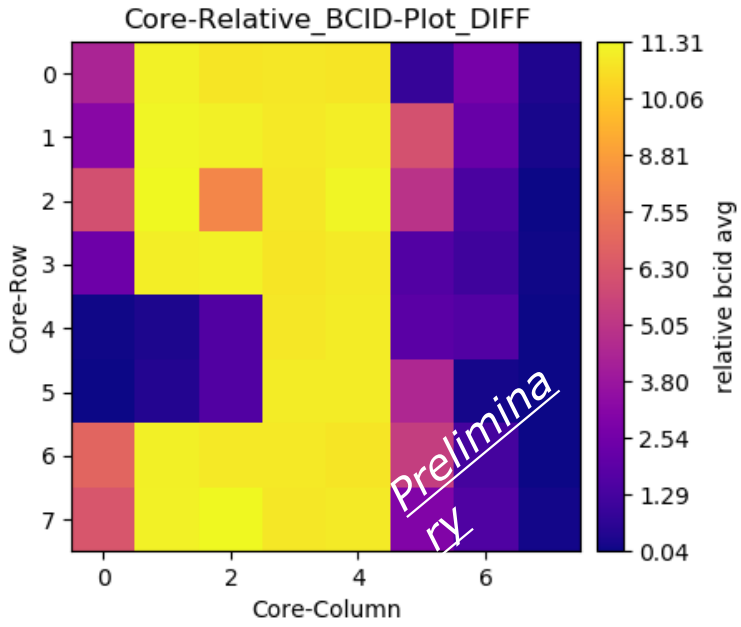
Conclusions

- The **RD53A demonstrator** has been submitted in August 2017 in the framework of the RD53 Collaboration in a **65 nm CMOS technology**
- **RD53A is alive and preliminary test results are very promising**
- **Test systems** will be soon available for the institutes to test sensors with RD53A
- **First production lot** (25 wafers) bought (waiting for confirmation of delivery date)
- **RD53** design team, involving ~ 20 designers, is working to development of final pixel chips to be submitted 2019

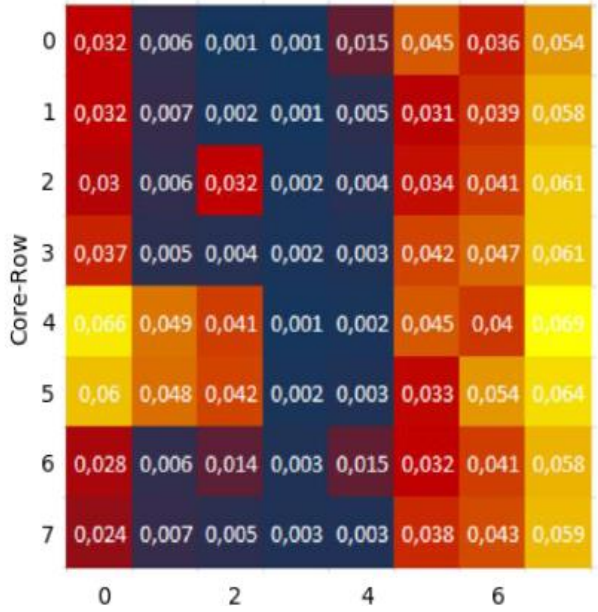
Backup

Differential Analog Front-end: bug

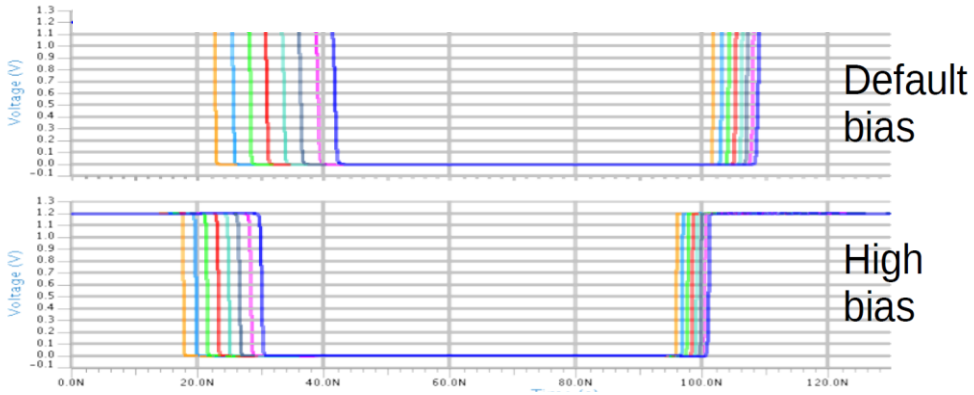
- Bug in the A/D interface: missing P&R constraint on the Diff. FE hit output → Varying load capacitance on comparator output → systematic variation of delay and ToT
- Will improve A/D verification strategy for production chips



Extracted outdisc net load [pF]



- Partially recovered increasing comparator bias current and decreasing preamp discharge current
- **This bug does not prevent the Diff FE full characterization**



RD53A Power consumption

Configuration	VDDD [mA]	VDDA [mA]
No clock in pixel cores (at startup)	124	365
Full chip enabled	442	365

- Direct powering
- Default bias settings
- **Value mostly as expected**

- On average (including Chip Bottom): 5.7 μA/pix (digital) -- 4.7 μA/pix (analog)
- In final chip less contribution from the Chip Bottom
- Further optimizations in both analog/digital pixels under investigation for final chips

RD53A main specifications

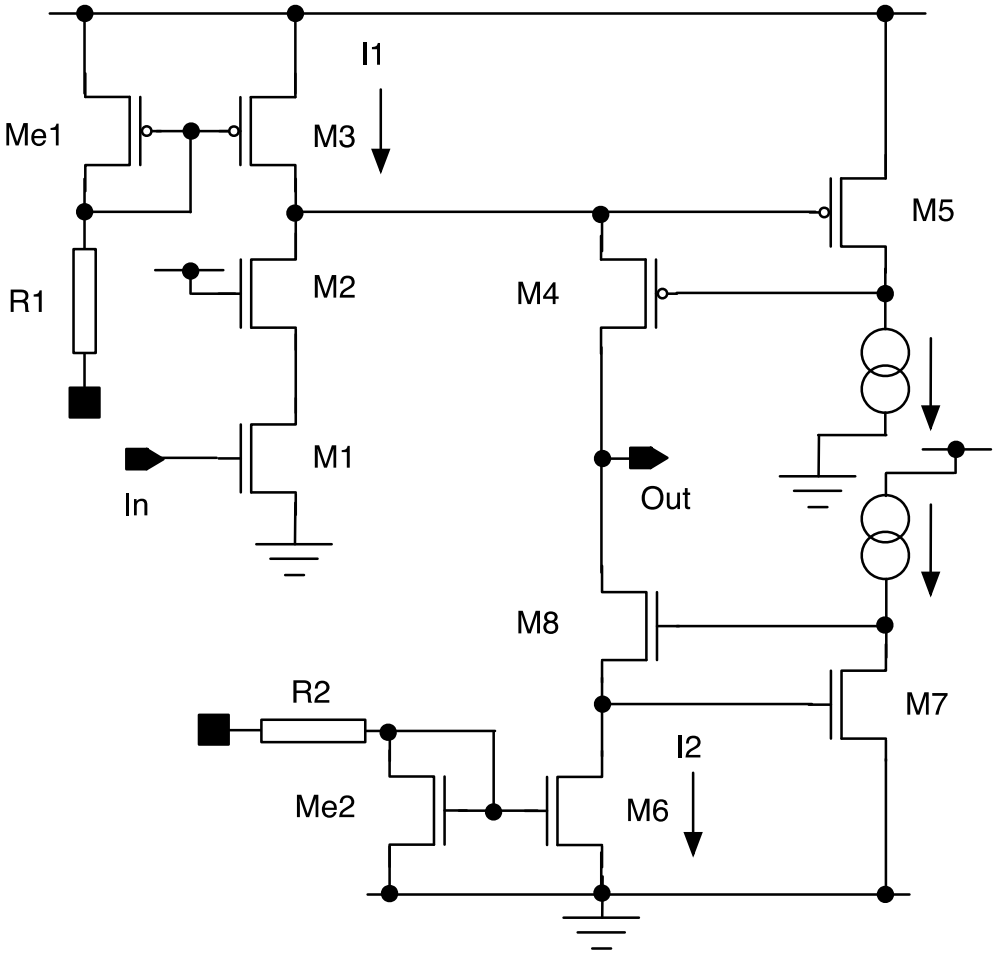
From the Spec. document **http://cds.cern.ch/record/2113263**

- **Hit rate:** up to 3 GHz/cm^2 (75 kHz pixel hit rate)
- **Detector capacitance**: < 100 fF (200 fF for the edge pixels)
- **Detector leakage**: 10 nA (20 nA for the edge pixels)
- **Trigger rate**: max 1 MHz
- **Trigger latency**: 12.5 us
- **Low threshold**: 600 e- → severe requirements on noise and dispersion
- **Min. in-time overdrive**: < 600e-
- **Noise occupancy**: < 10^{-6} (in a 25ns interval)
- **Hit loss @ max hit rate**: 1%
- **Radiation tolerance**: 500 Mrad @ -15° C

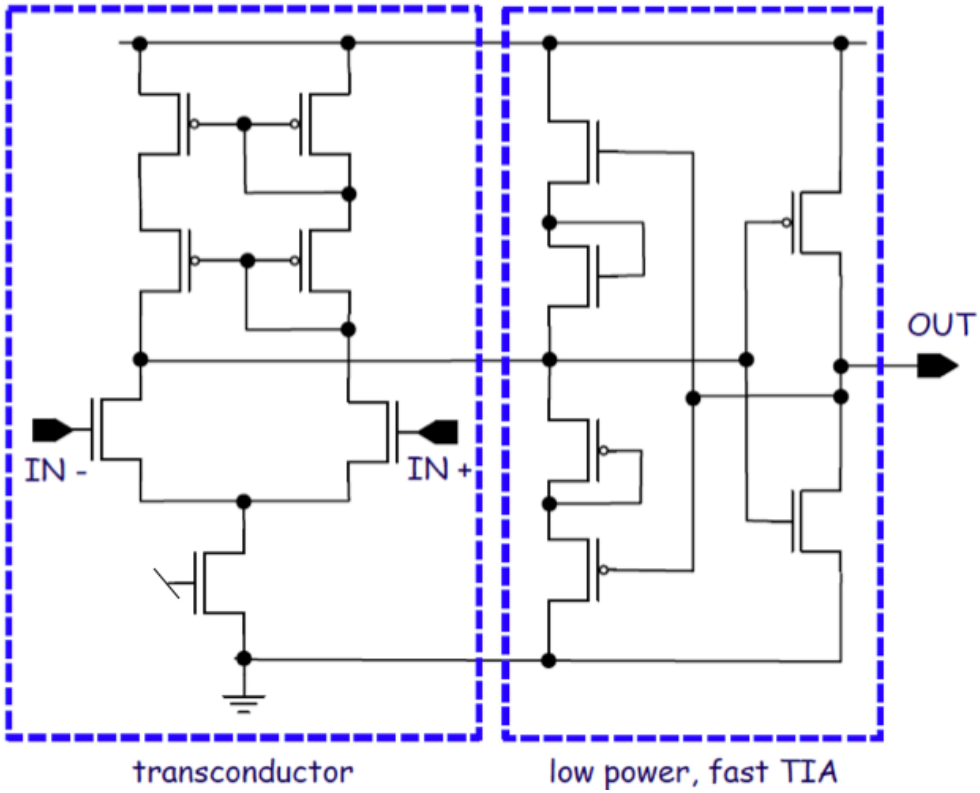
Lin AFE schematic diagrams

RD 53A

Preamplifier



Comparator

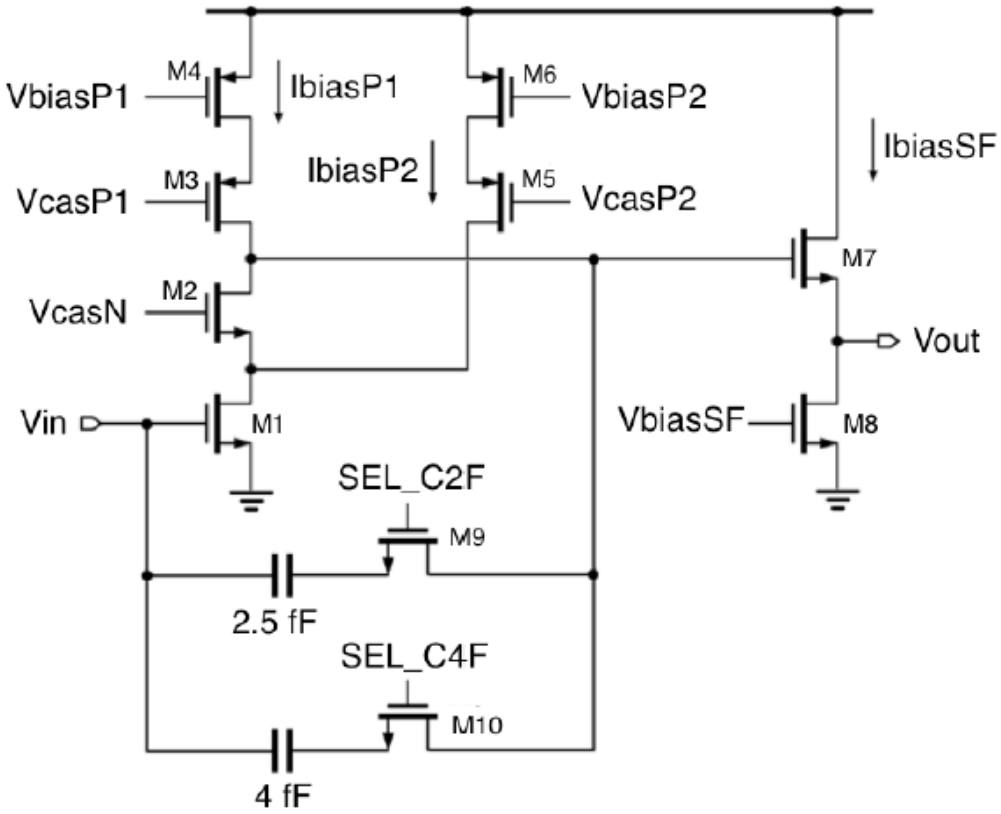


- Gain stage based on a **folded cascode** configuration (~3 uA absorbed current) with a regulated cascode load

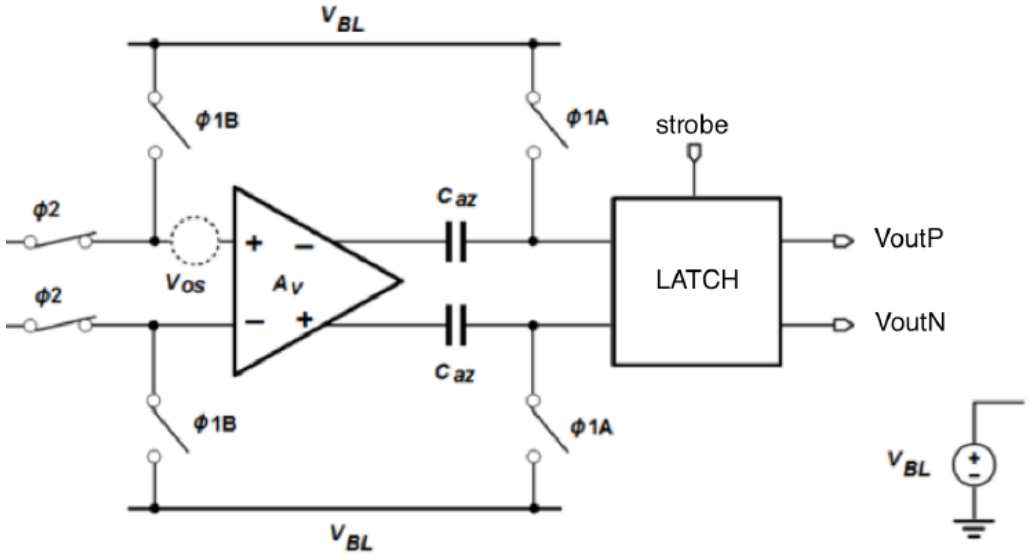
- Low power, **fast discriminator** (~ 1 uA absorbed current) including Gm stage and a transimpedance amplifier providing a low impedance path for fast switching

Sync AFE schematic diagrams

Preamplifier



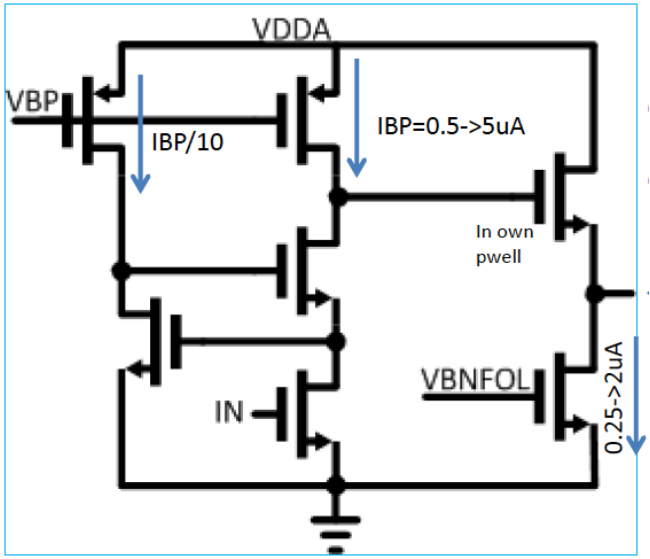
Comparator



- Telescopic cascode with current splitting and source follower
- Two switches controlling the feedback capacitance value

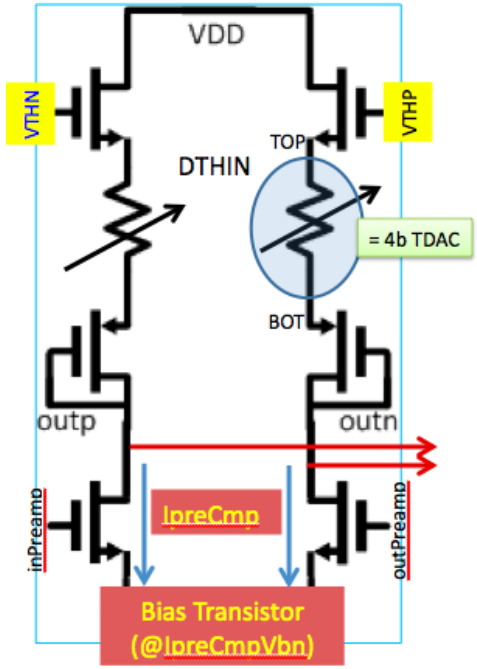
- Offset (and mismatch) cancellation based on **comparator autozero** (store offset on a capacitor, and then subtract it from signal + offset)

Diff AFE schematic diagrams



Preamplifier

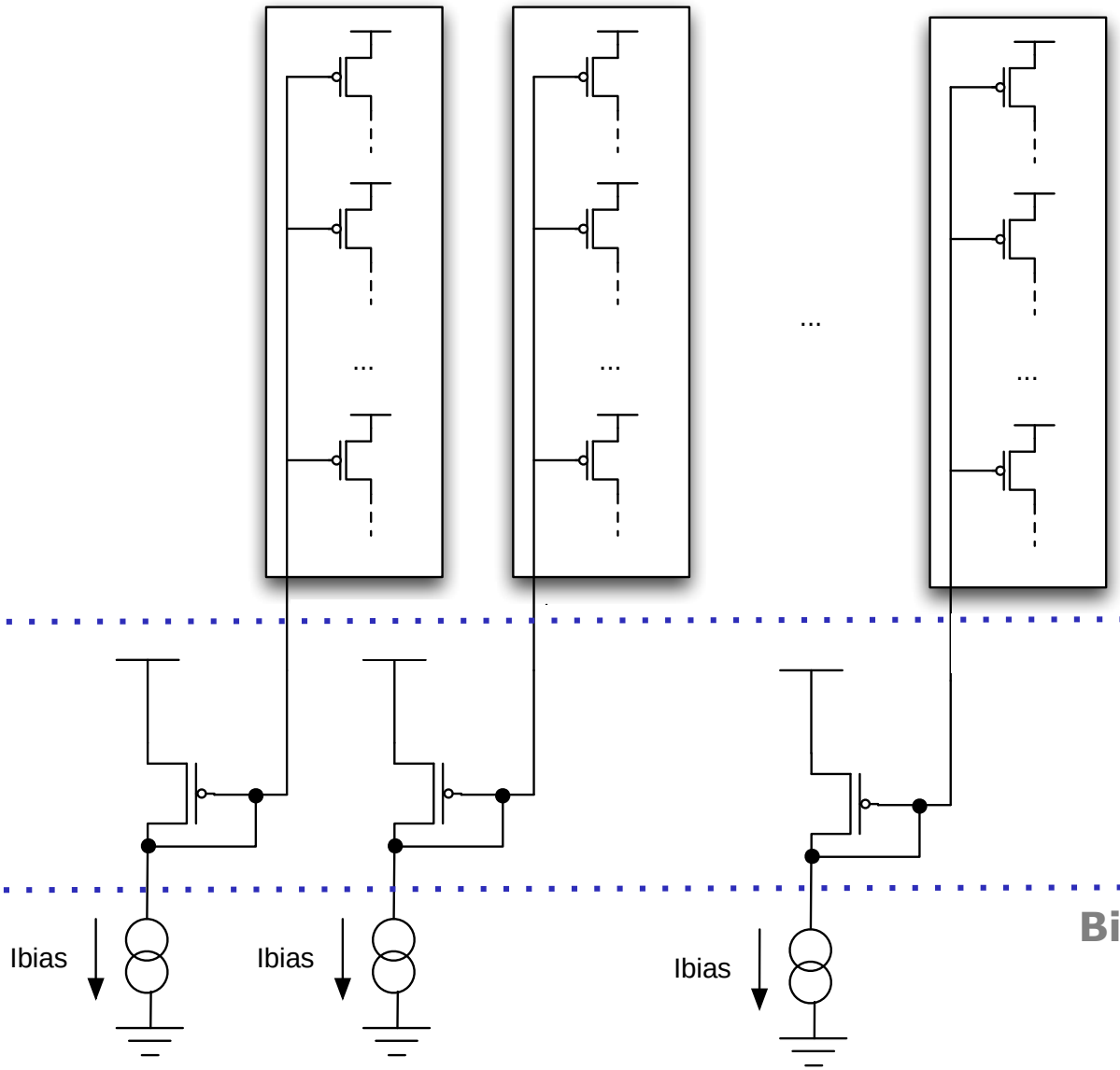
- Gain stage with active cascode
- Simple follower as buffer



Pre-comp

- Fully differential amp w/ resistive load
- Acts as single-to-differential converter
- Global Vth DACs generates effective differential supplies
- Local DTHn trims binary-weighted resistive load
- Sets output CM and differential OP for comp

Analog FE bias scheme



- Robust design
- Not sensitive to leakage
- "Double stage mirroring", biasing DACs and Bandgap refererences **already integrated/tested in CHIPIX65**

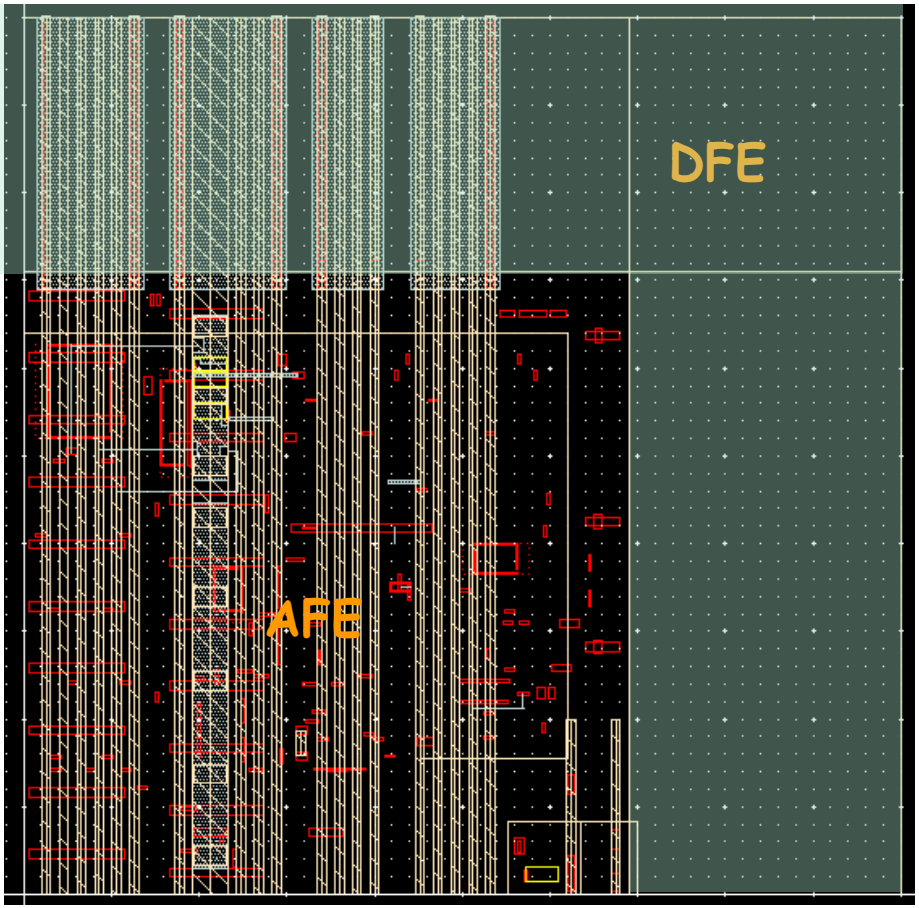
Pixel array

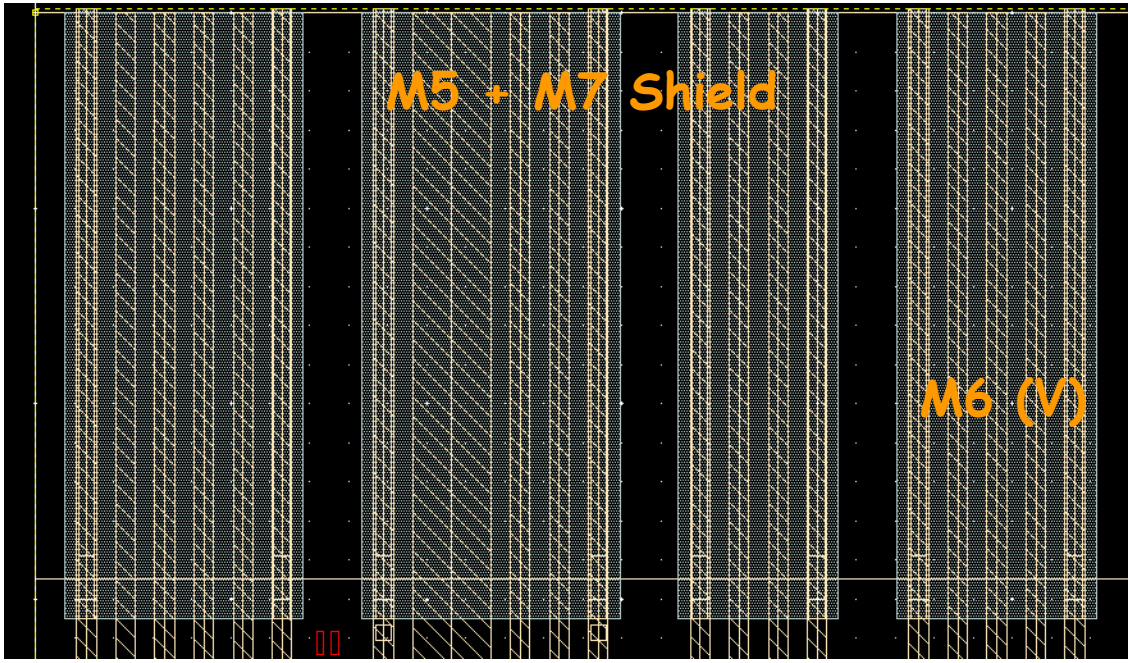
Second stage mirroring (Macrocol bias)

Biasing DACs + first stage mirroring (ACB)

Analog bias

- AFE **area & arrangement** → 35um x 35 um aspect ratio with "analog island" arrangement
- **Same bump PAD structure**
- **Common strategy** for power, bias distribution & shielding

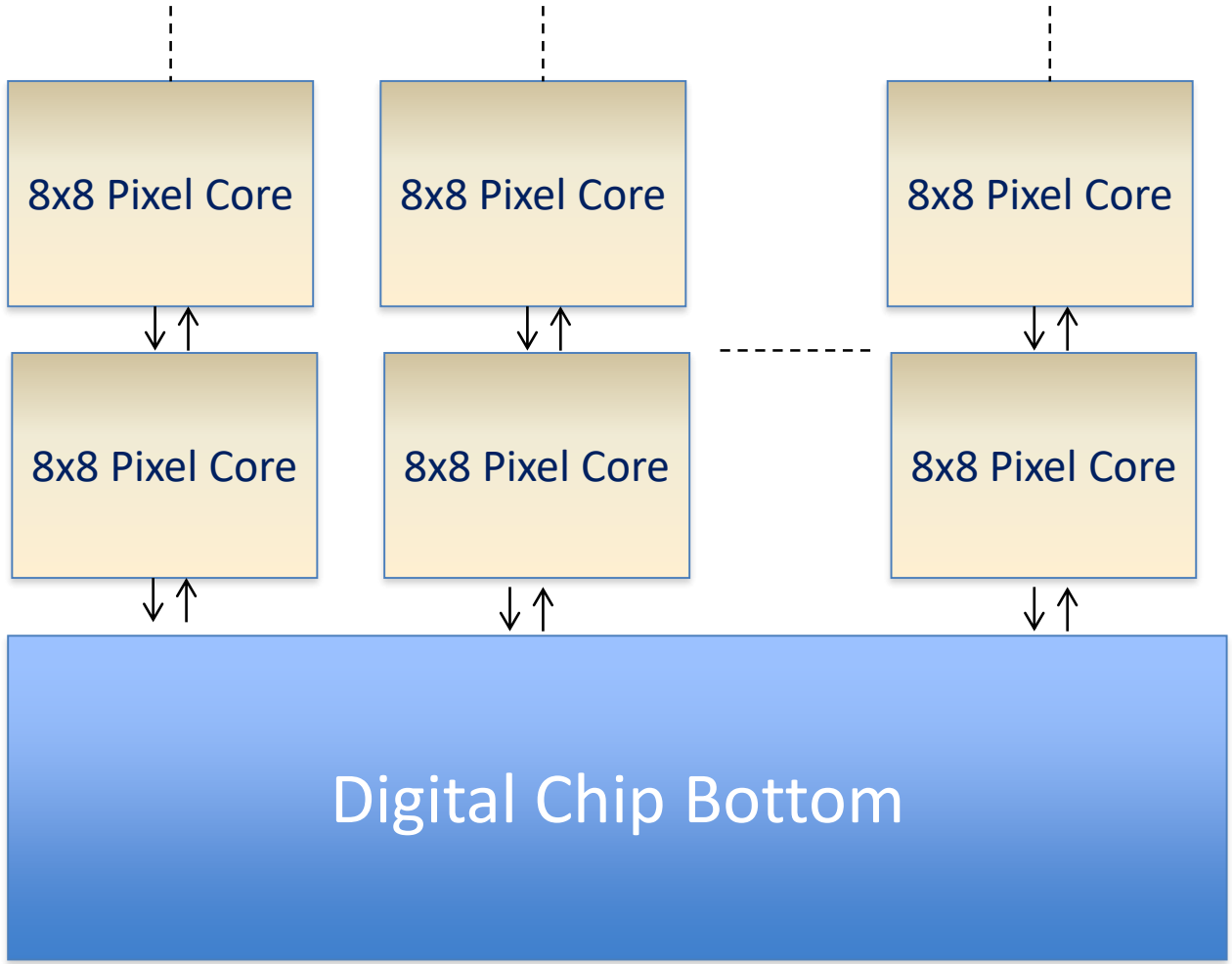




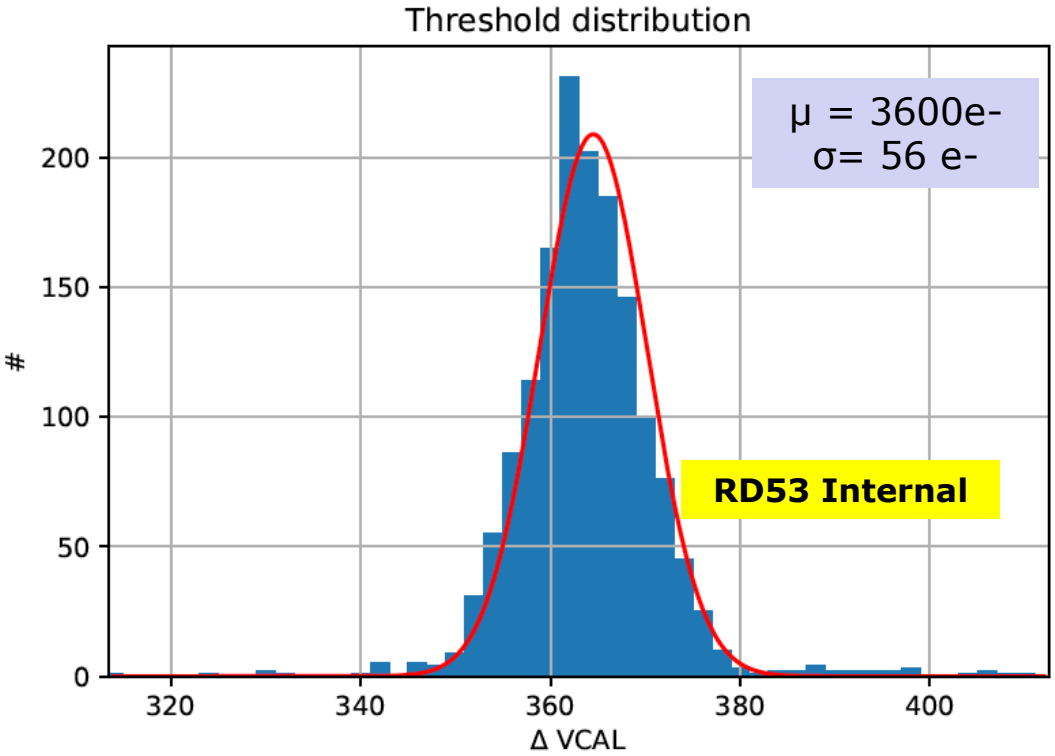
- **M6 V lines** for the analog bias
- **M5/M7 shield** for bias lines in the digital section of the pixel
- **AP/M9/M8** V supplies

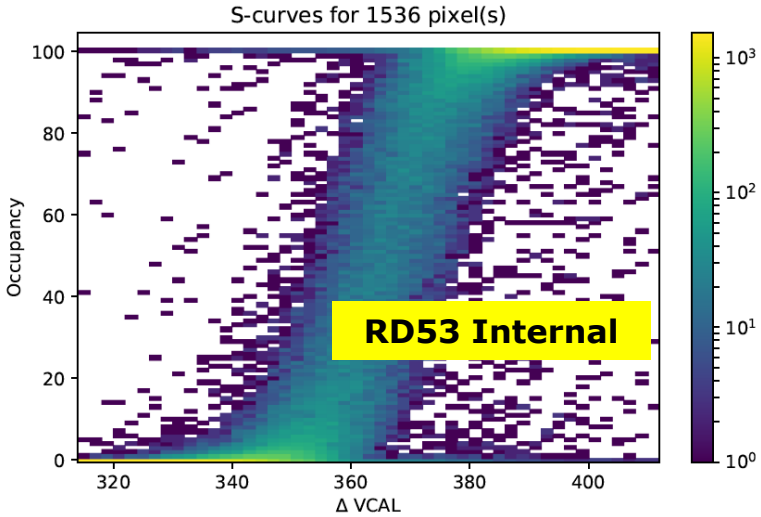
Pixel array logic organization

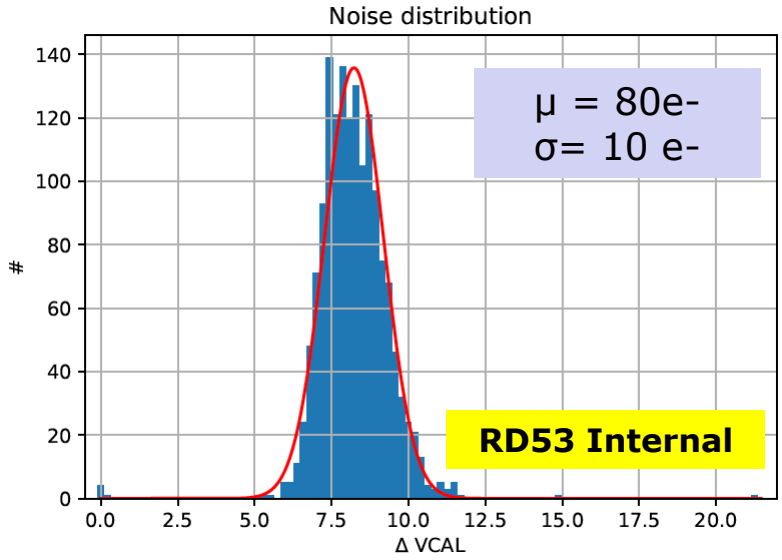
- Each Pixel Core receives all input signal from the previous core (closer to the Digital Chip Bottom)
- Regenerates the signals for the next core.
- The timing critical **clock** and **calibration injection** signals are internally delayed to have a uniform timing (within 1-2 ns)



Linear Analog Front-end - Injection-based tuning







- Linear FE fully functional
- 56 e rms threshold dispersion after tuning @ relatively high th