Integrated Front-End Electronics for Ultra-Low Background Dark Matter Detection

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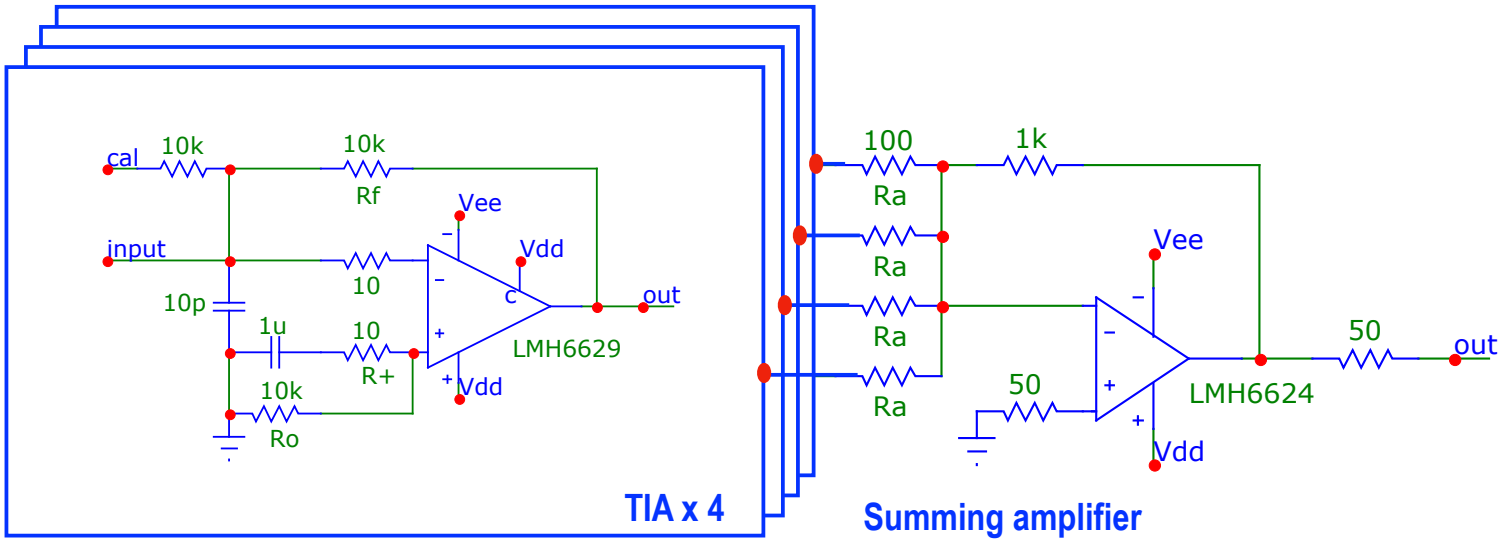
IC FEE for Low-Background LAr DM: opportunities and challenges

- Work developed in the framework of the **Darkside Collaboration**
- Propose and demonstrate solutions for very low background photoelectronics for future massive frontier LAr Dark Matter Experiments
- Need for cost-effective technologies towards the instrumentation of very large areas
- Reduce interconnections to the warm electronics through the use of local signal processing and digital data multiplexing
- Scalable solutions based on a smart sensor network of cold photodetectors and readout electronics
- Starting point: photoelectronics and requirements for **Darkside-20K**, a 20 Tonne Two-Phase LAr TPC for Direct Dark Matter Detection at LNGS

Baseline front-end electronics for Darkside-20K



- Four independent transimpedance amplifiers plus a summing amplifier
- Based on SiGe bipolar operational amplifiers
- Matches and exceeds the key specs
- About 40 discrete components to be mounted on each front-end card
- Two analog output lines per module
- Power consumption 250 mW

IC development roadmap for DarkSide

- **Level 1: Single channel front-ends**
  - Easier compatibility with the discrete solutions
  - Fast design time
- **Level 2: Front-end ASICs with on-chip event digitisation**
  - Custom multi-channel FE+ADC ASIC in CMOS technology
  - Use data multiplexing to reduce the number of fibers
  - Daisy-chain readout, 1 Data Link per Motherboard
  - Photoelectronics assembly on a Silicon Active Interposer
- **Level 3: Multi-pixel front-end ASIC towards single-photon counting**
  - Target pixel size for single-photon time-tagging on Dark-matter experiments could be 1.25 mm x 1.25 mm
  - SiPM sensor 1 cm^2 on a 8x8 pixel arrangement
  - 64 channels per cm^2, 150 μW per pixel
  - Hybrid approach for independent optimisation of sensor and CMOS FEE
  - Target Time resolution O(1 ns)
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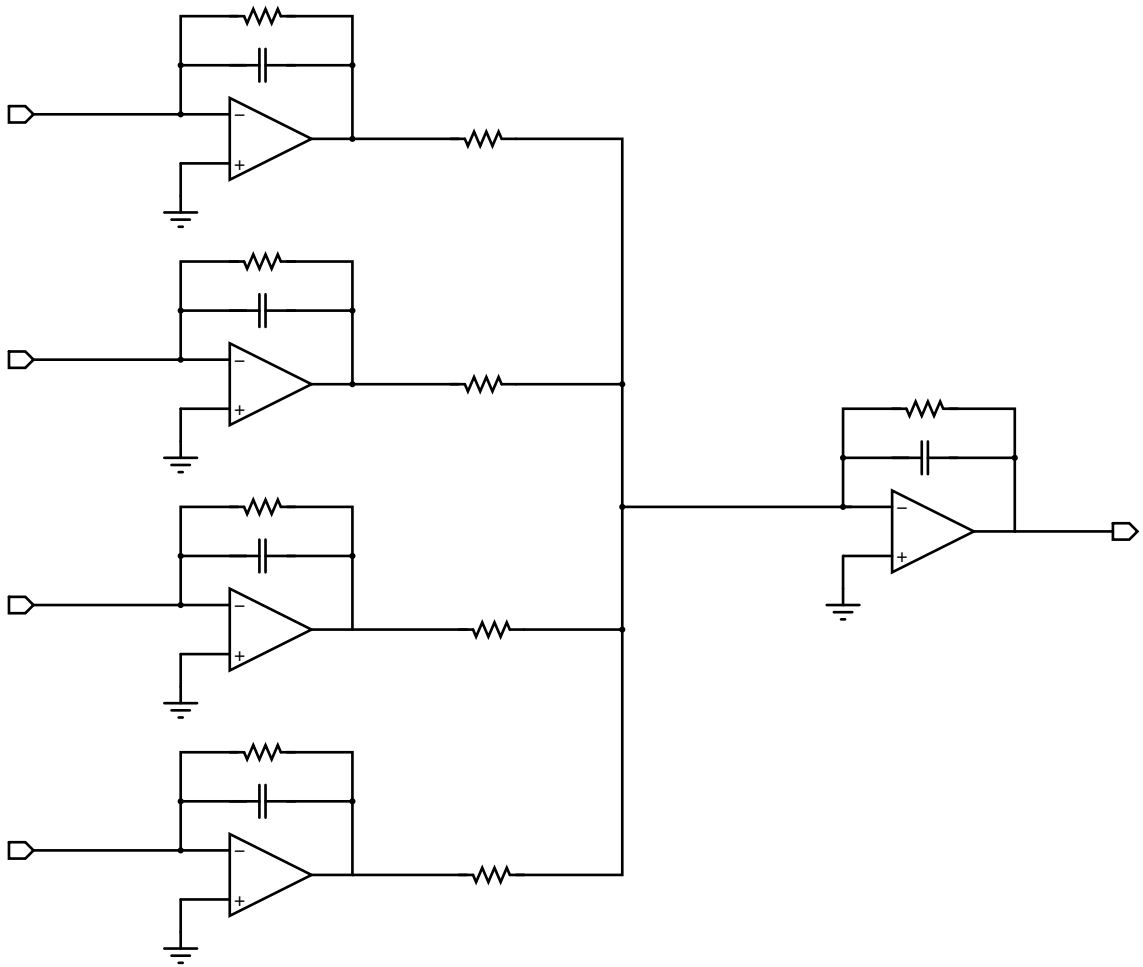
Op-amp based single channel front-end

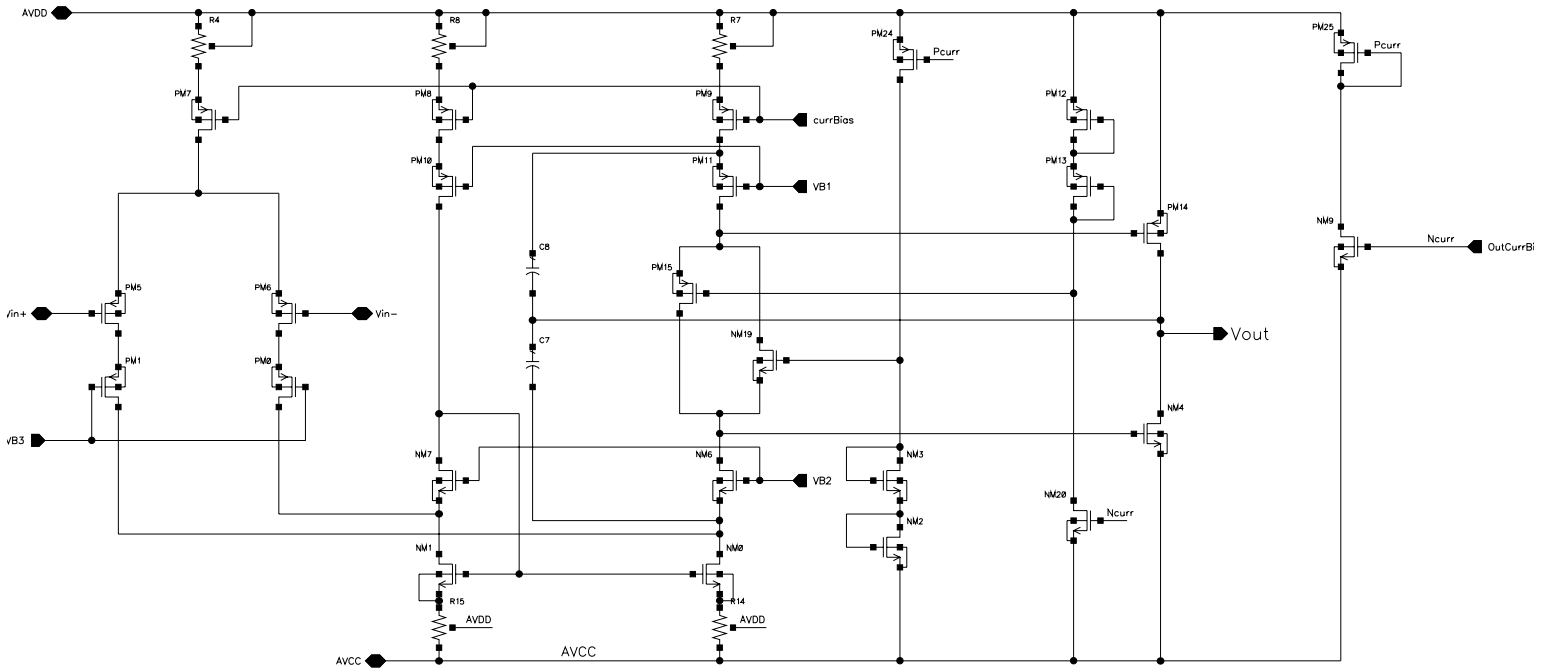
- Straightforward integration of the discrete front-end for DS-20K
- Four transimpedance amplifiers and a summing amplifier

- Two poles for noise filtering
- Simple DC coupling among stages ☺
- Higher noise for a given power ☹



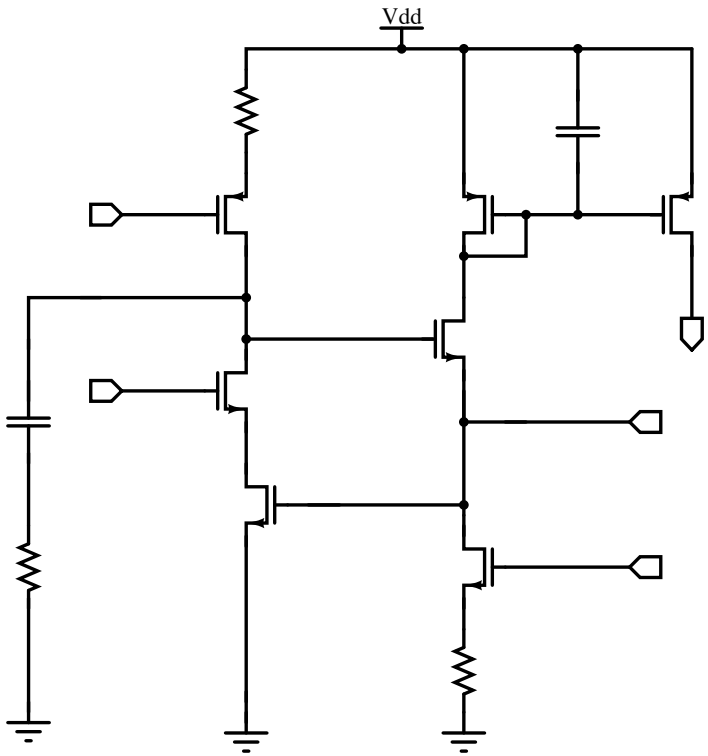
Cryogenic CMOS op-amp

- Thin oxide input transistors for better transconductance and lower noise
- Cascode input transistors to reduce voltage
- Thick oxide transistors to support 2.5 V operation
- Class AB output stage for low power and high drive capability



Alternative front-end

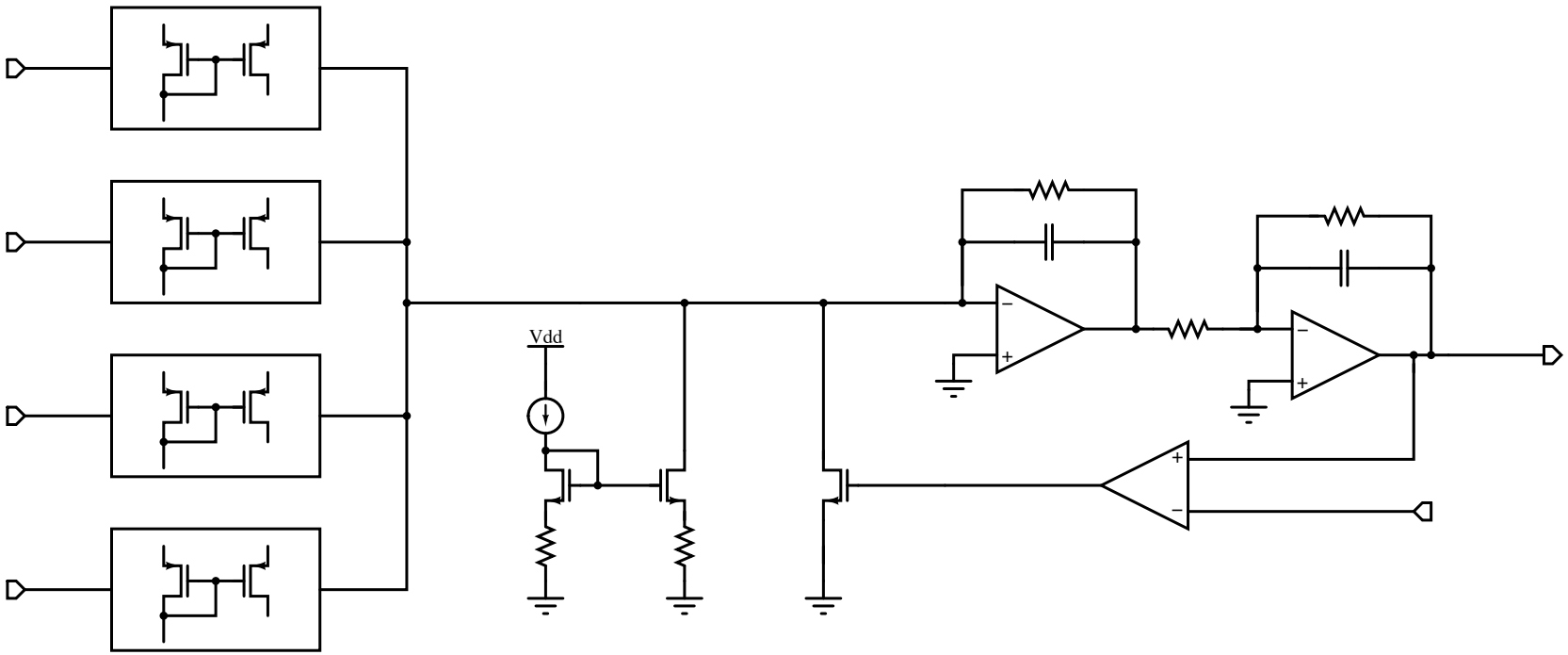
- Single-ended input stages have better noise vs power figure
- Can be exploited to have smaller power or higher speed



- Common gate with local feedback loop to decrease input impedance
- Noise dominated by input transistor in the feedback loop
- Thin oxide input transistor with protection cascode
- 4 mA of bias current
- Transconductance: 80 mS at 300 K and (estimated) 200 mS at 77 K

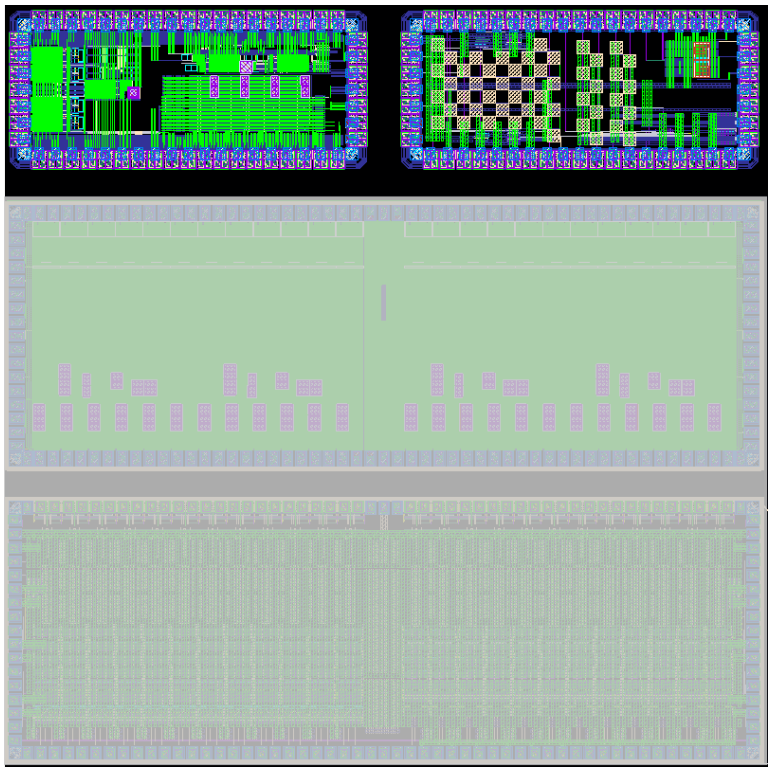
Full channel

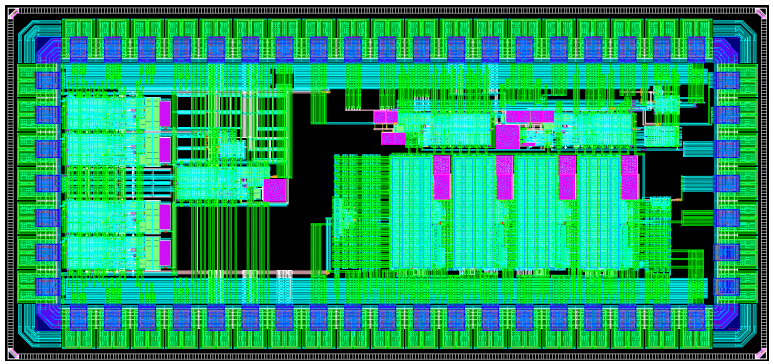
- Four channels are combined into a single output
- Op-amp in the second stage have the same topology as the ones used in the OTA-based front-end
- Baseline restorer needed to compensate the DC current from the first stage

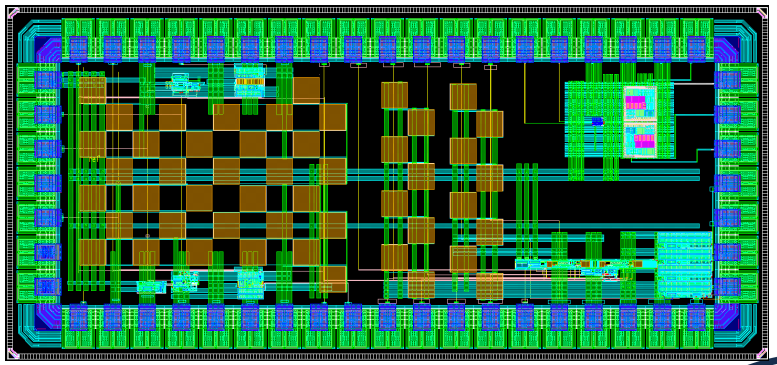


Submission status

- Two test chips submitted in January, delivery mid-June
  - Full channel for 24 cm^2 SiPMs based on TIAs
  - Full channel for 24 cm^2 SiPMs based on common gate input
  - DC and AC-coupled RGC VFEs for ALCOR[1], bandgap, LVDS Tx, digital test structures
  - shared 5x5 mm^2 MPW, each test-chip 2.3 x 1.1 mm^2







[1] covered in next slides

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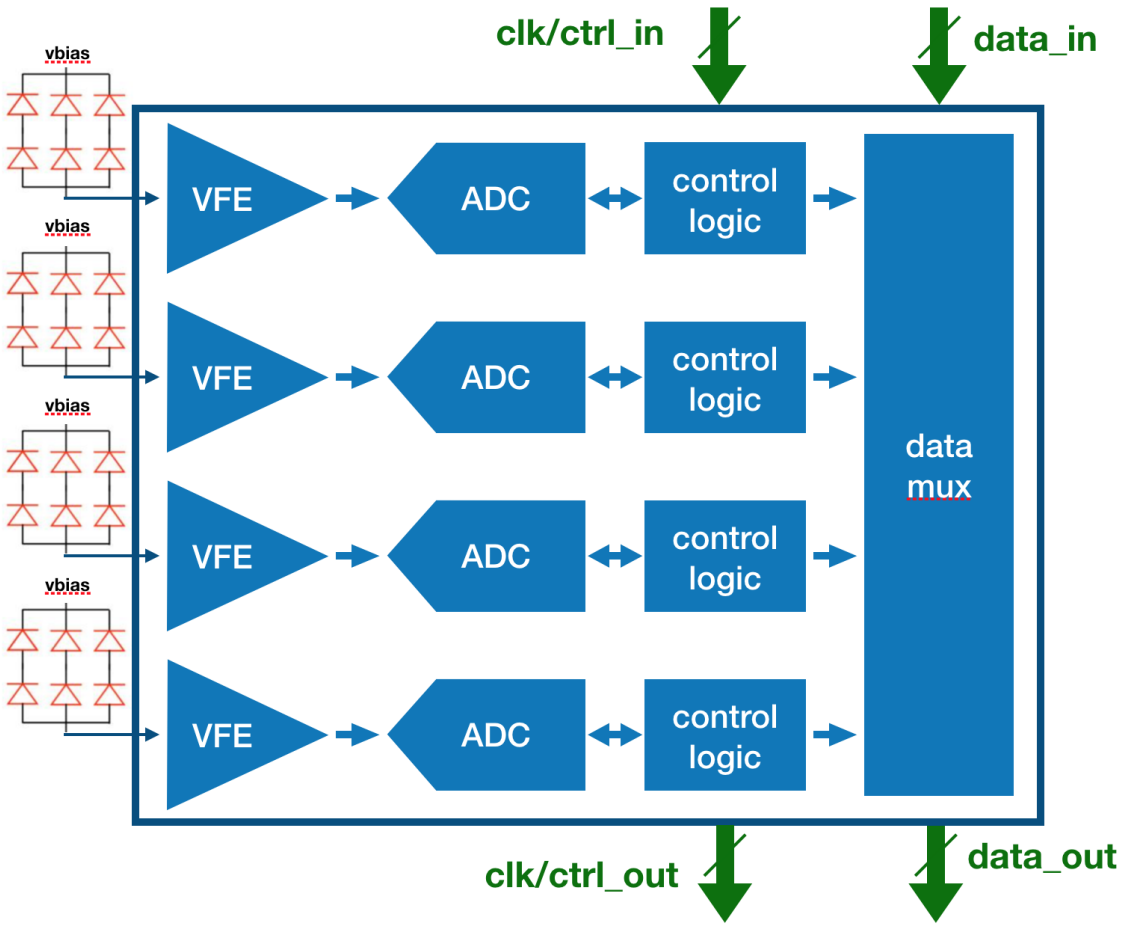
Short term possibility towards a mixed-signal ASIC for DS-20K



- quad-channel ASIC with front-end and digitisation circuitry
- each channel reads a 6 cm^2 2s3p SiPM
- signal digitised by a full-sampling ADC
- noise reduction by a factor of 2, with respect to an analogue multiplexing scheme
- on-chip data multiplexing, daisy-chain readout, faulty chips overriden

- A dual-TPC LAr DM detector would eventually need few bits for ADC or even simpler charge measurement schemes
- Would significantly decrease the number of data links towards the warm DAQ

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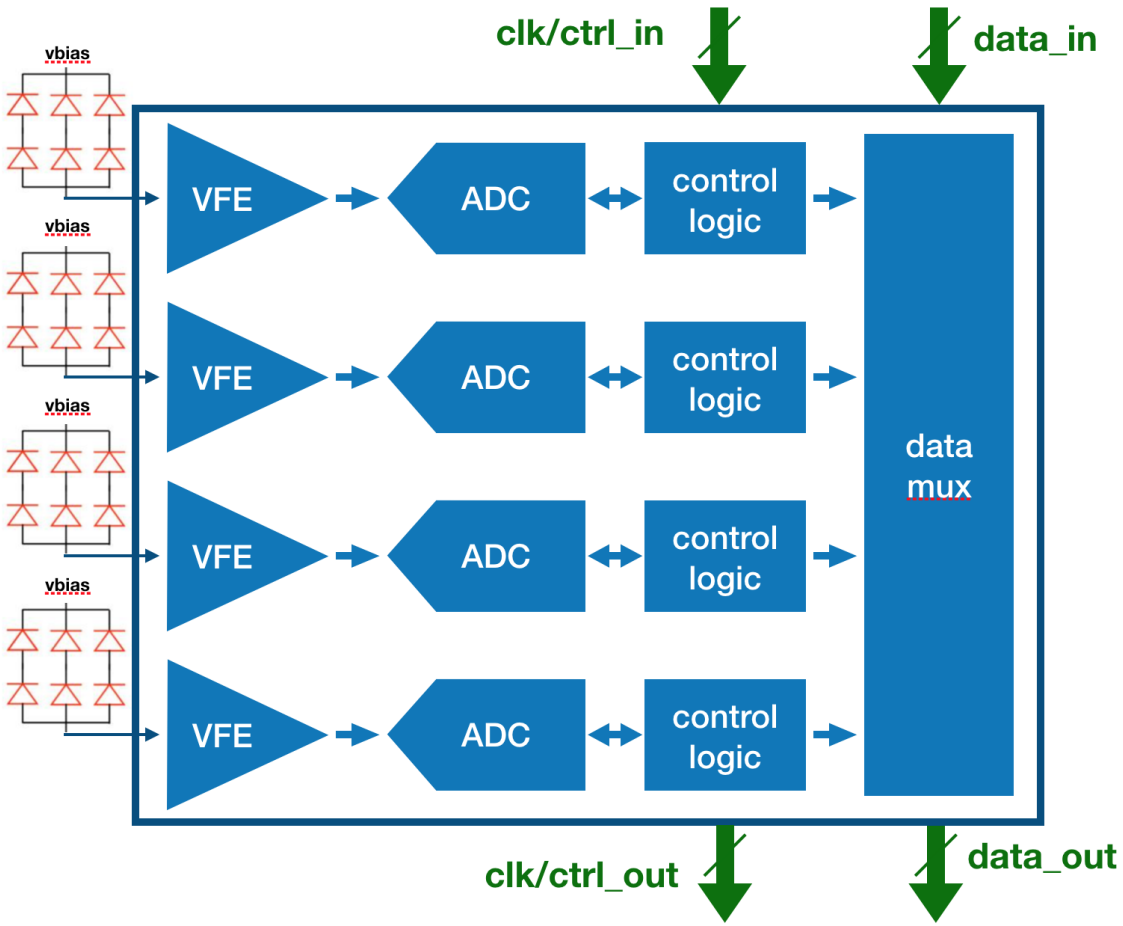

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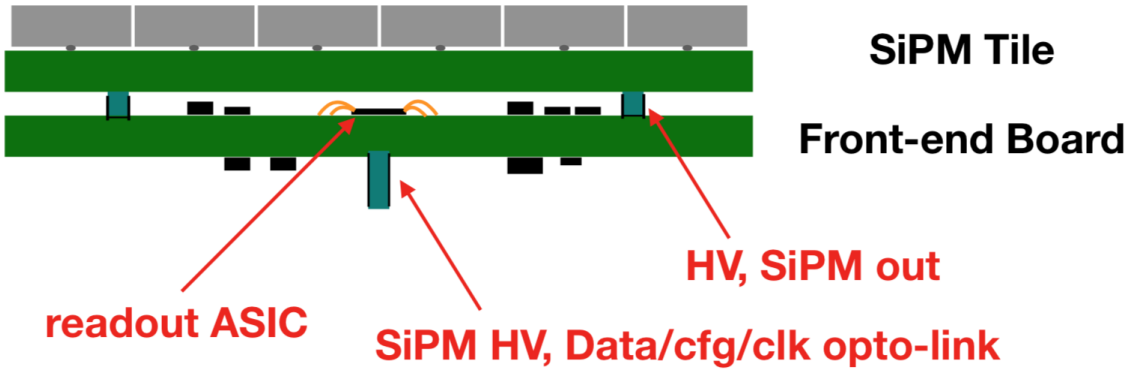
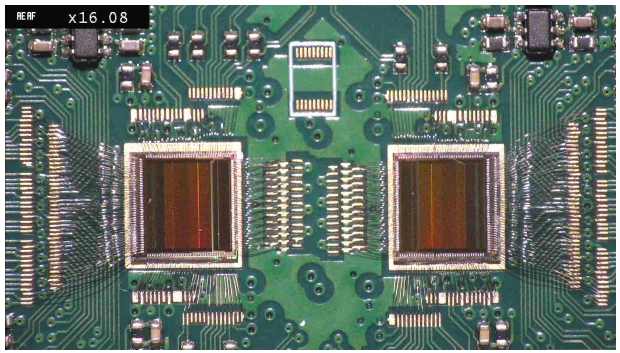
Possibilities for Front-end Electronics and SiPM assembly

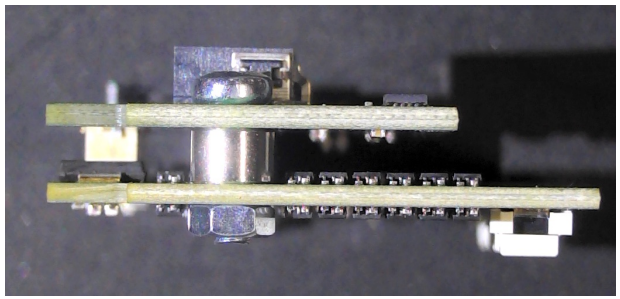
- possible sketch of a stack-up with SiPM and FEB
- FEB hosting ASIC, LDOs, connectors, optical driver (could be on-chip) and LED



- Chip-on-board, wire-bonding or flip-chip mounting
- Smaller substrate volume in respect to a discrete solution, but residual system-level gain

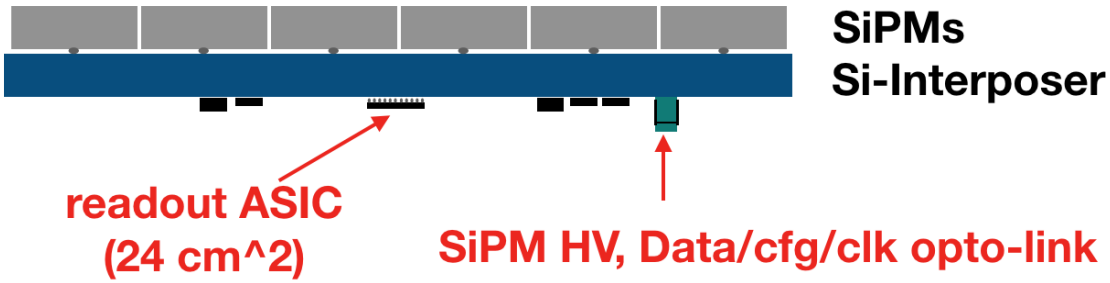
Example of a 128-channel 50 mm^2 integrated electronics front-end module for sensor readout (INFN-TO)





Possibilities for Hybrid Photoelectronics assembly on DM detectors

The need for a very-low background on LAr dark matter detectors calls for the use of a **silicon substrate** for background reduction



- **passive silicon interposer** as a re-distribution layer
- wire-bonding or flip-chip mounting of readout ASIC
- SiPMs and readout ASIC tested before assembly
- reduced number of masks for RDL → low NRE costs for interposer
- cost dominated by CMOS wafer production and post-processing (TSV)

- ⋆ simpler solutions (fused silica + polyimide?) could be more cost effective than CMOS
- ⋆ Routing of the output signal from SiPM on 5 cm long CMOS BEOL traces could be challenging
- ⋆ Optimisation: read and digitise 1 cm^2 SiPM
- ⋆ Data transmission on the sensor node network managed with token

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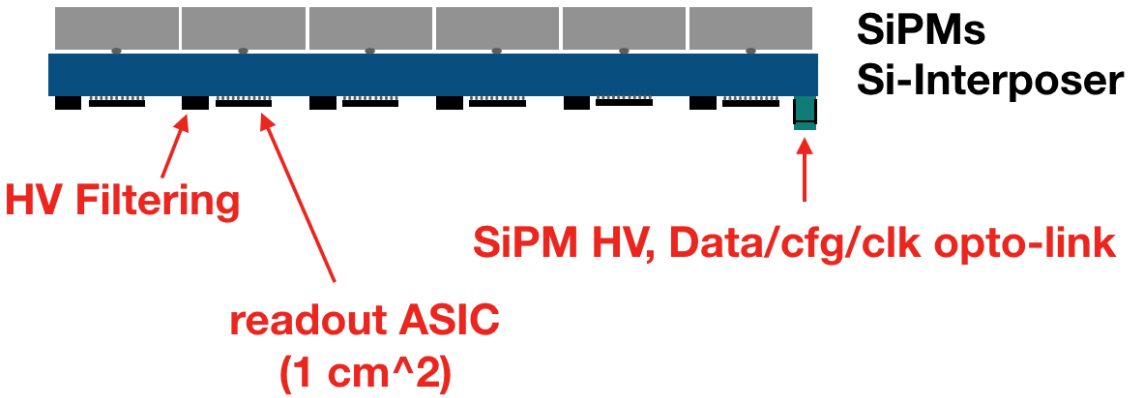

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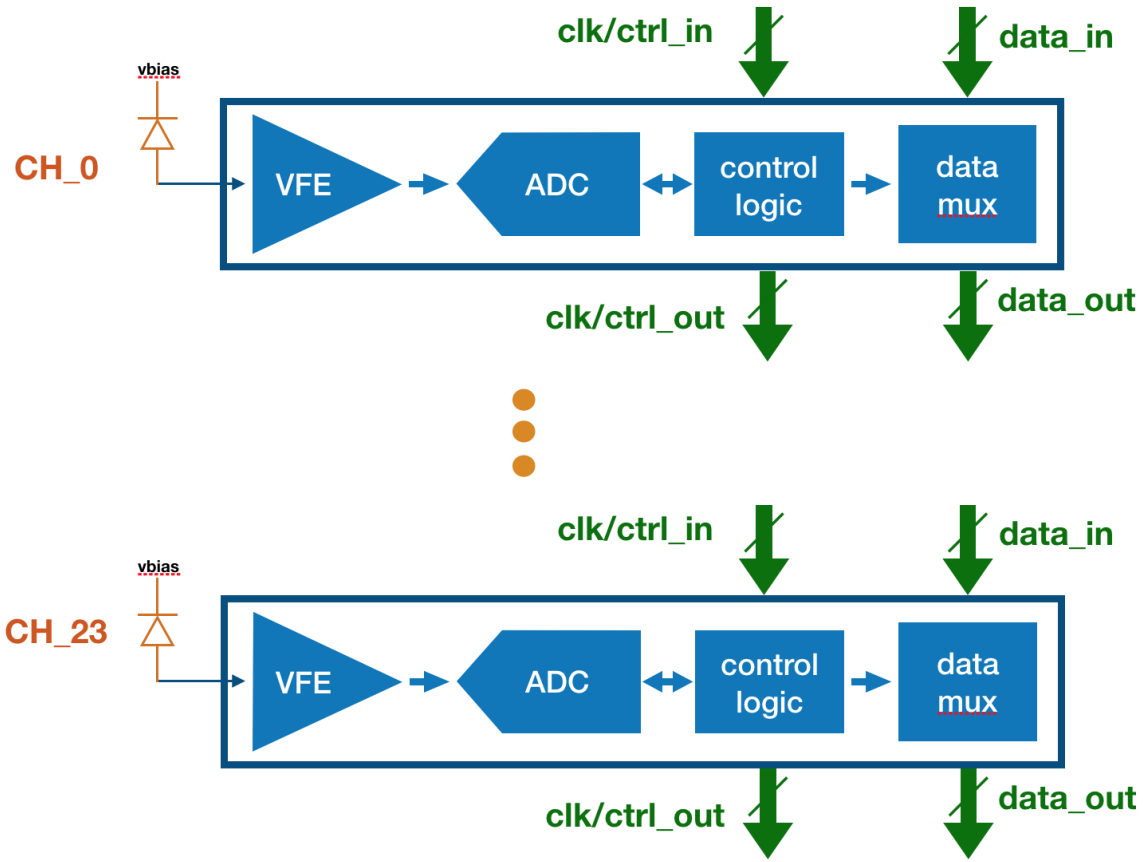

- Each node amplifies, digitises and multiplexes data
- Redundancy or e-fuse allow to override faulty nodes; characterisation phase or during operation (configuration)
- Current mode differential signalling (CML, SLVS) for clock/reset, configuration and data transmission
- SiPMs and readout ASIC tested before assembly
- each ASIC node is about 4 mm^2, large-scale cost dominated by Si-Interposer (CMOS or fused silica)

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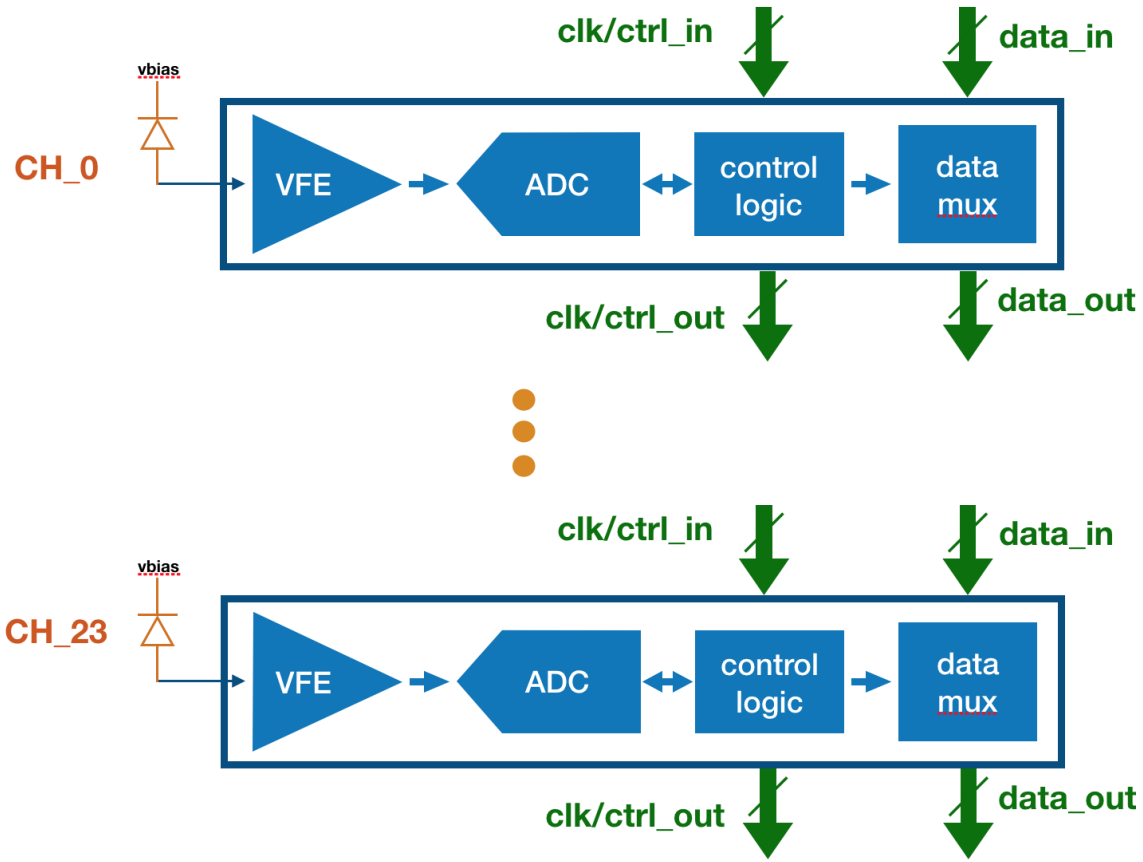

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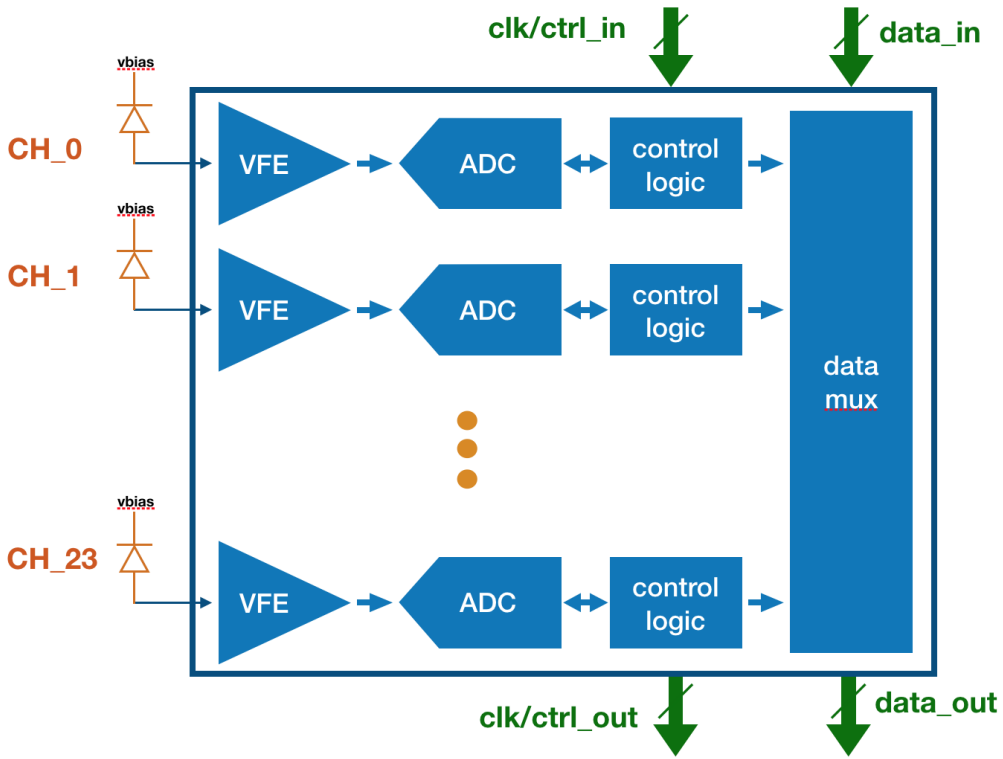
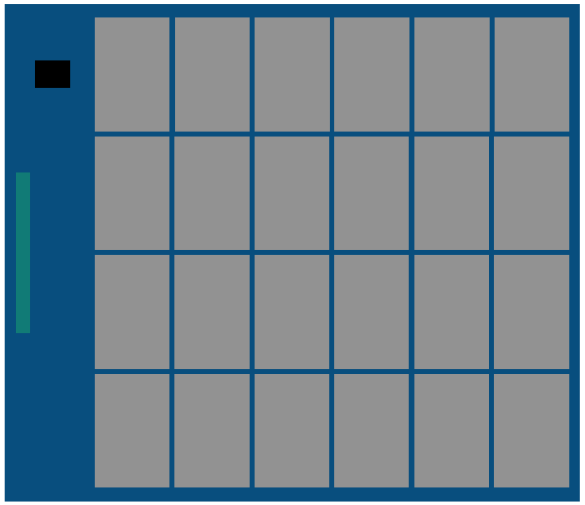
Towards the development of active CMOS interposers





- ⋆ first prototype on standard CMOS pilot-line (no TSV) to qualify mixed-signal electronics and data transmission scheme
- ⋆ thick BEOL metalisation for signal and data transmission
- ⋆ Current mode differential signalling for clock/RST, configuration and data transmission
- ↪ Stitching of 2 reticle-size chips (max reticle 26x32 mm)

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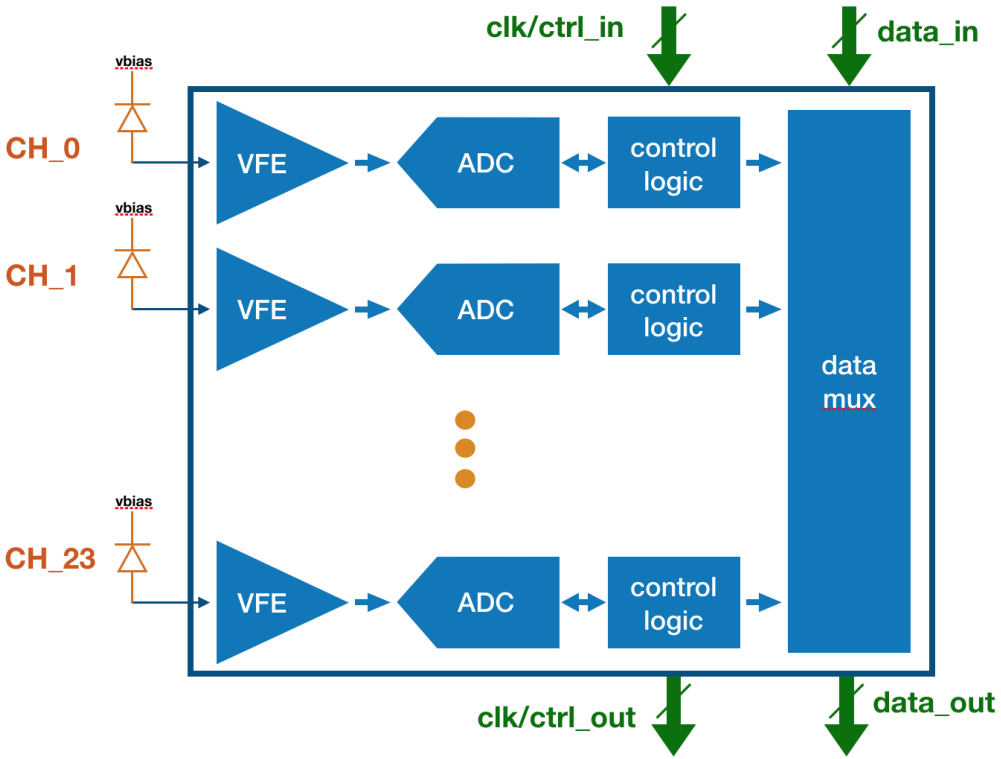

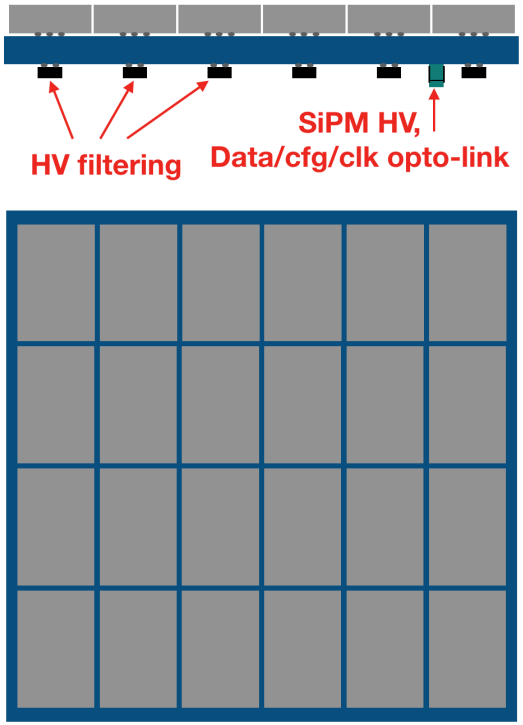

- ⋆ second prototype: re-spin of a subset of BEOL masks
- ⋆ TSV post-processing: use of aSiPMs allows for relaxed TSV pitch
- ⋆ better PSRR and common-mode noise rejection with optimal HV filtering
- ⋆ tap bonding and kapton strip for electrical link, or
- ⋆ on-chip transceiver and off-chip LED and optical link

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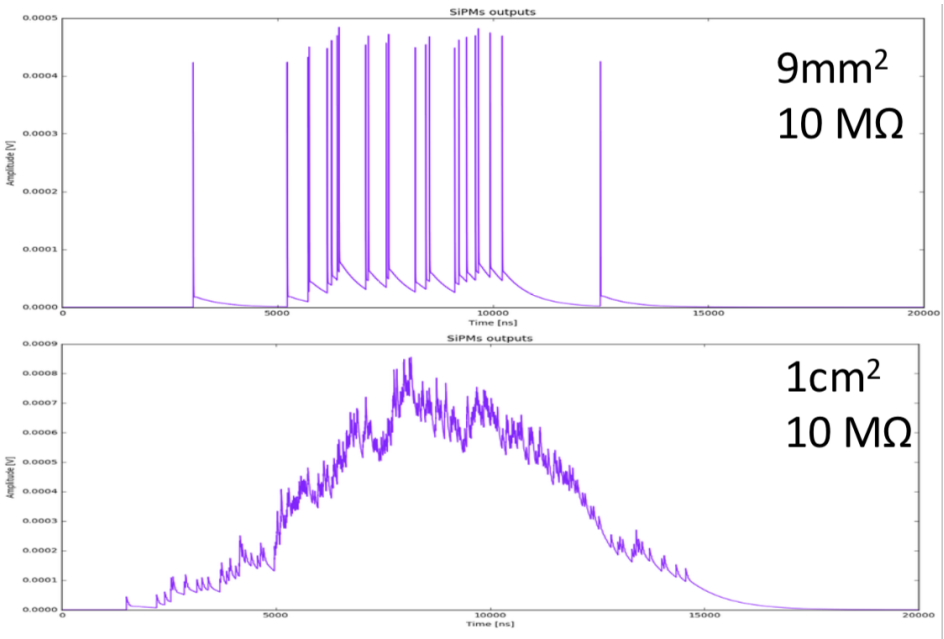
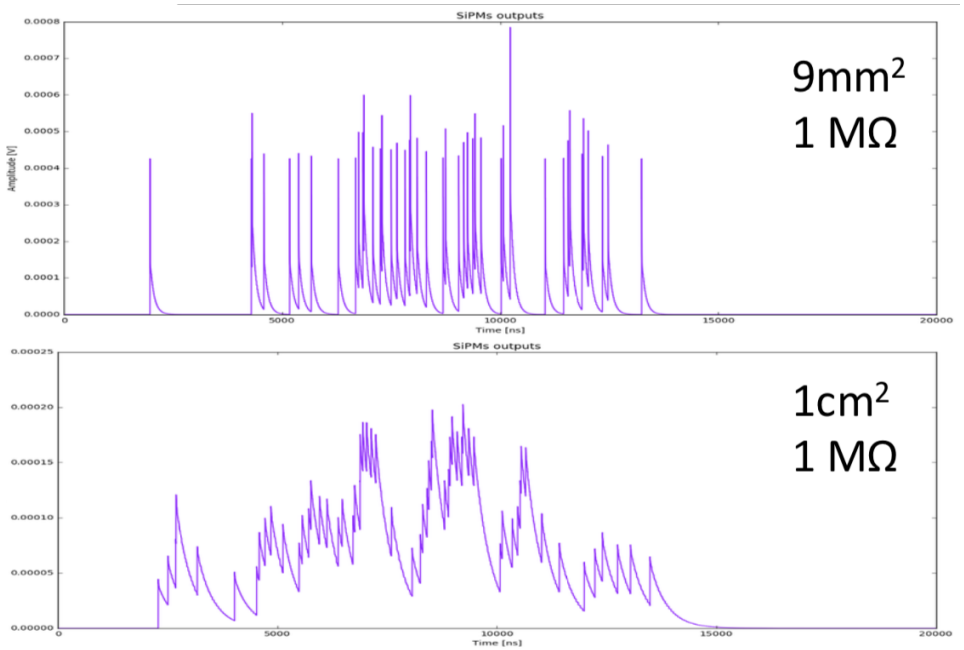
Motivation for a single-photon readout

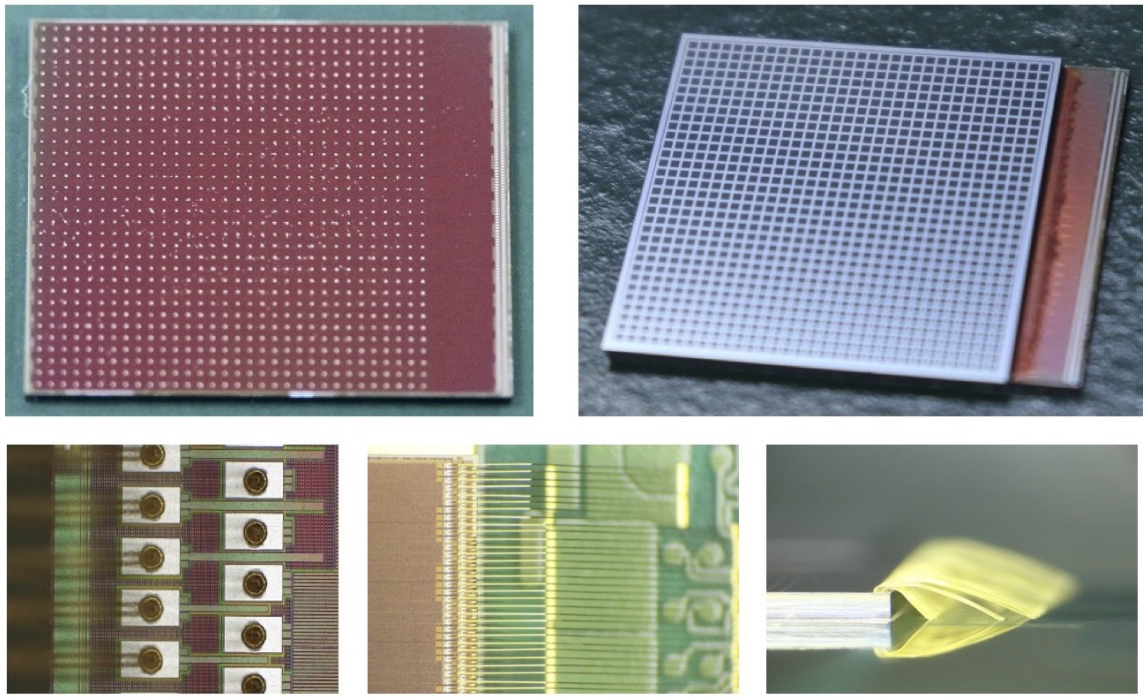
- High-level simulations (R. Kugathasan, A. Cocco) on Ar39, Ar40 S2
- aggressive pixelisation could allow for a single-photon tagging, even on S2
- SiPM parameter tuning (Rq) already implemented on new FBK R&D pilot run
- A SiPM pixel size of few mm^2 would be suitable for dark matter detectors and other applications





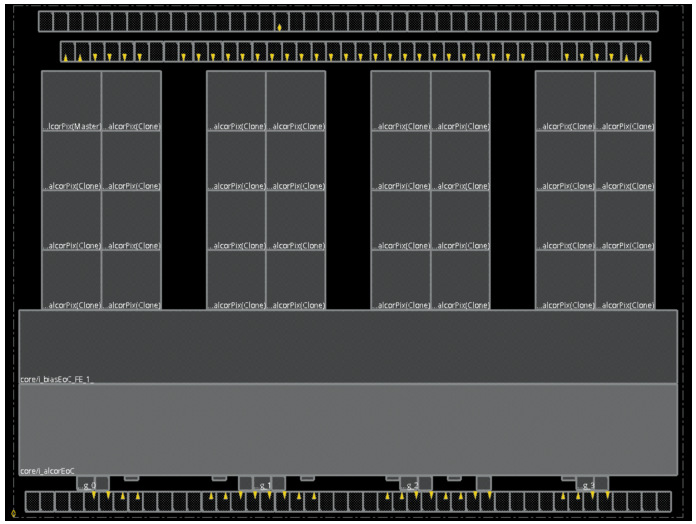
Starting point for a single-photon readout

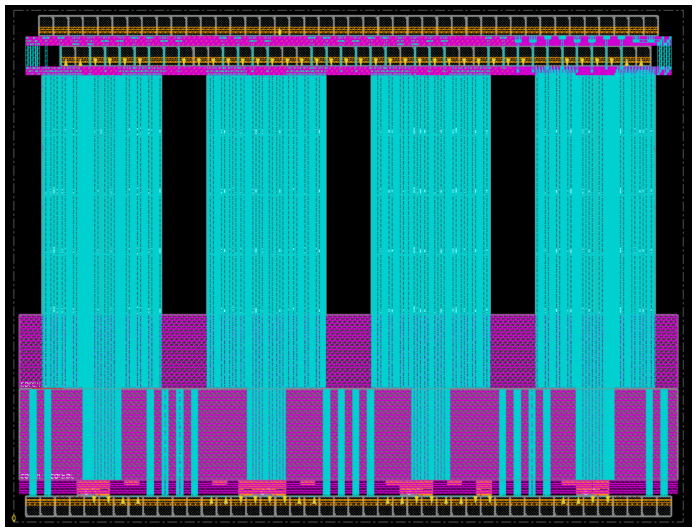
- CMOS 1024-pixel readout ASIC for fast timing applications developed by INFN-TO
- UMC 110nm technology
- Pixel size 400 μm, 32x32 pixel matrix, approx 250 mm^2



- flip-chip mounted to a photosensor (*top right*). Detail of bonding pads (*bottom*) and bonding scheme for data and power
- The first-silicon ASIC performs single-photon time-tagging with a 30 ps r.m.s. time resolution, up to 200 kHz per pixel

ALCOR - A Low Power Chip for Optical Sensor Readout





- 32-pixel matrix mixed signal ASIC
- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O.
- each pixel reads an SiPM (up to 1 cm^2, compatible with smaller pixels)
- Pixel hosts SiPM VFE, leading-edge discriminator, 4 TDCs, charge integrator, digital control and interface
- Single-photon time tagging mode or time and charge measurement
- 64-bit (32-bit on time tagging mode) event and status data is generated on-pixel and propagated down the column
- Up to 4 LVDS TX data links used, SPI configuration
- operation from 10 MHz up to 320 MHz (TDC binning down to 50 ps)
- 10 MHz clock, 500 ps r.m.s. time resolution on single photon

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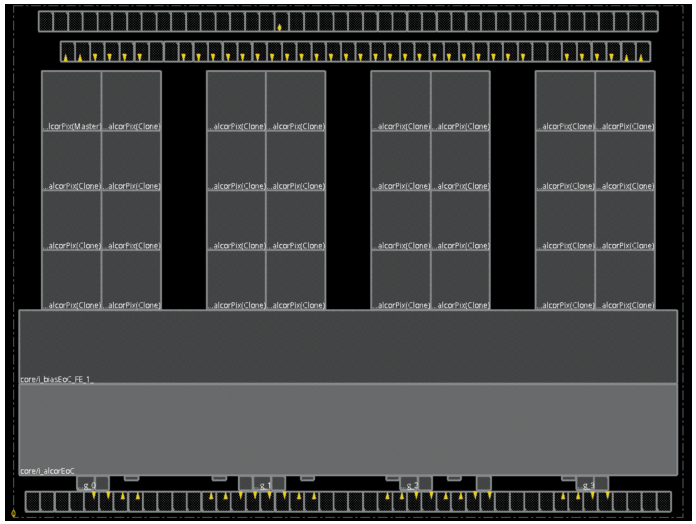

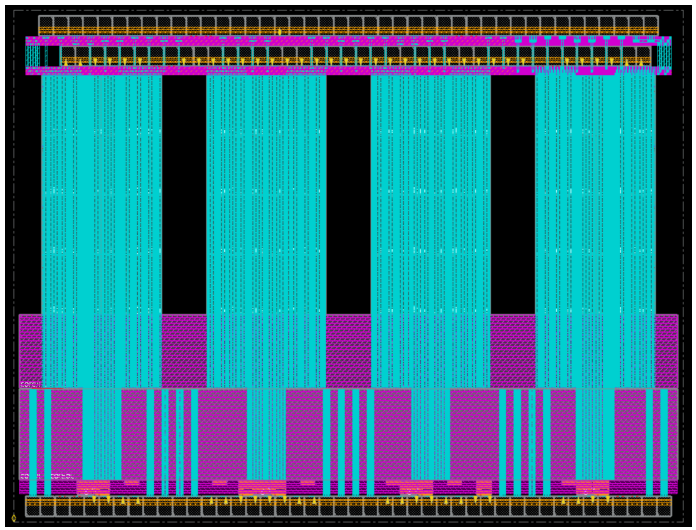

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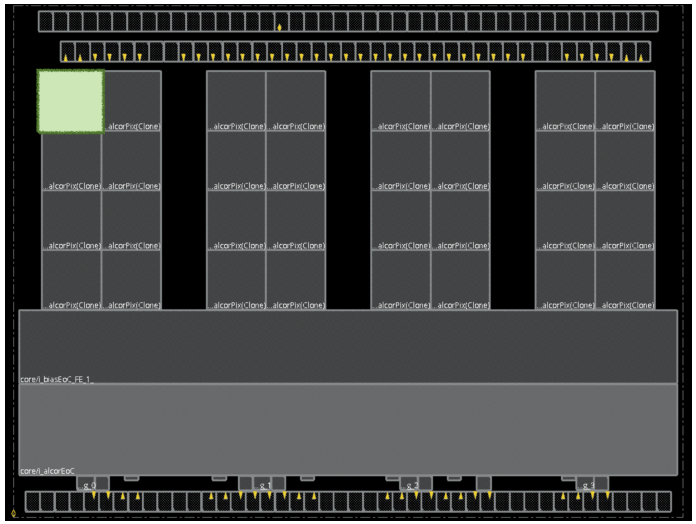
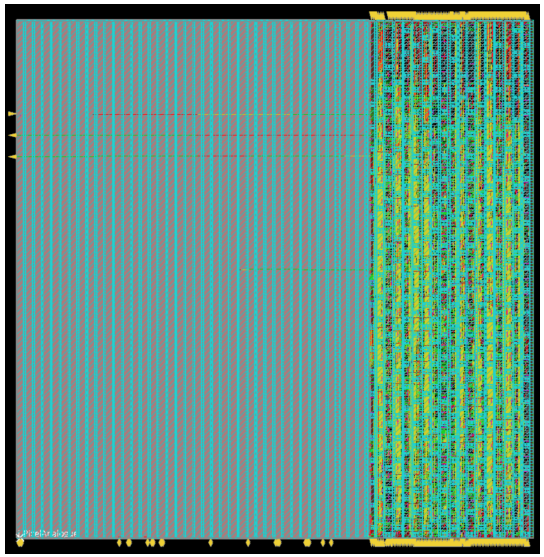
- 10 MHz clock, 500 ps r.m.s. time resolution on single photon

ALCOR - A Low Power Chip for Optical Sensor Readout





- 32-pixel matrix mixed signal ASIC
- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O.
- each pixel reads an SiPM (up to 1 cm^2, compatible with smaller pixels)
- Pixel hosts SiPM VFE, leading-edge discriminator, 4 TDCs, charge integrator, digital control and interface
- Single-photon time tagging mode or time and charge measurement
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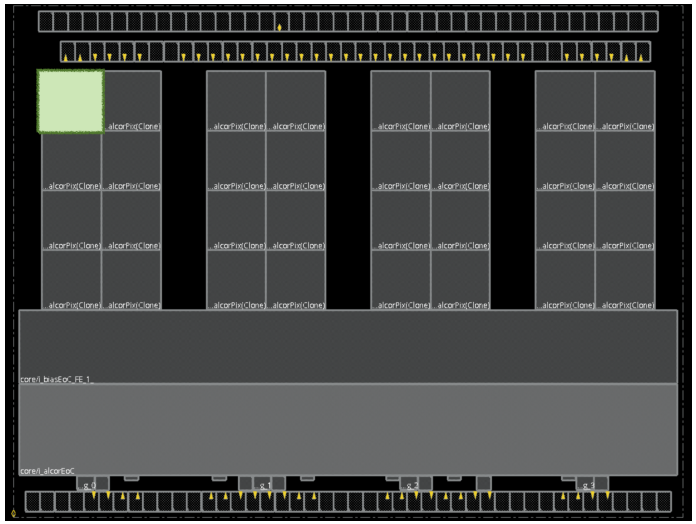

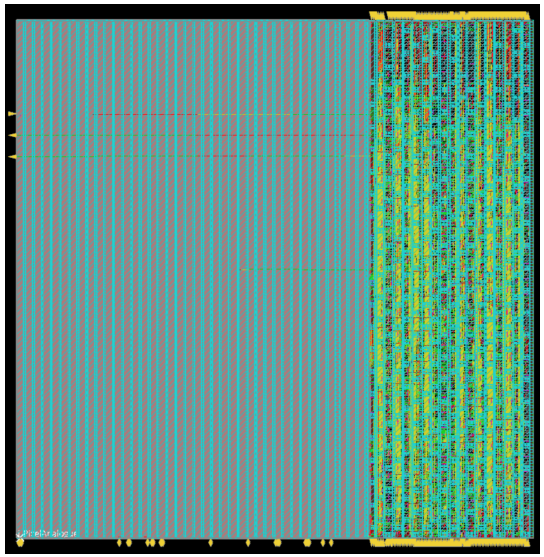

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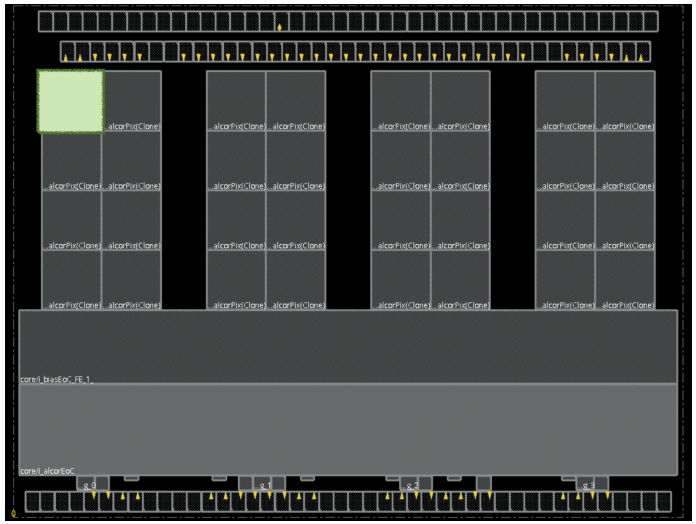

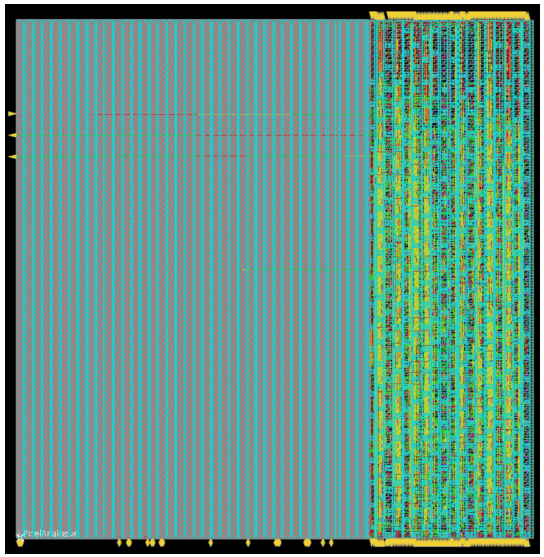

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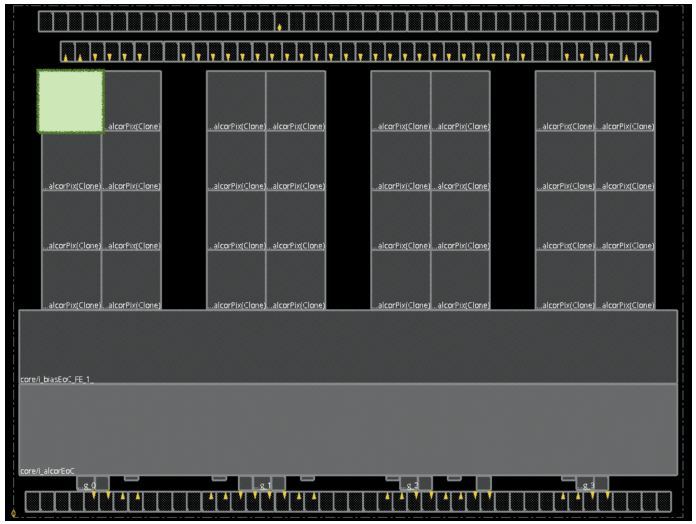

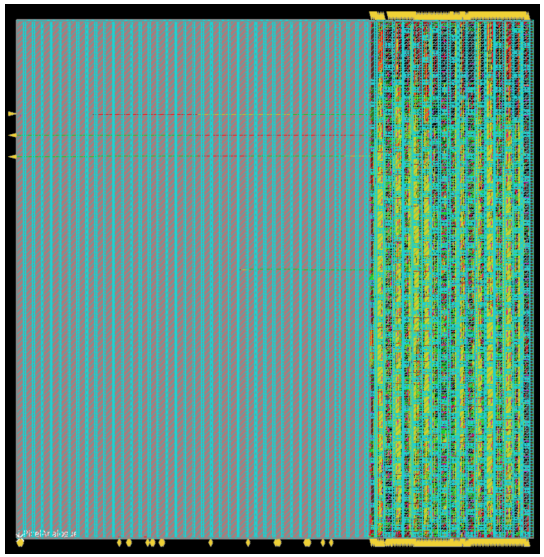

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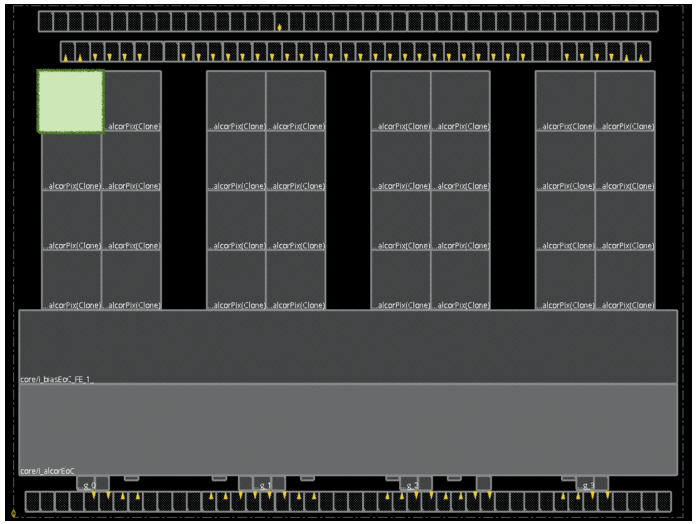

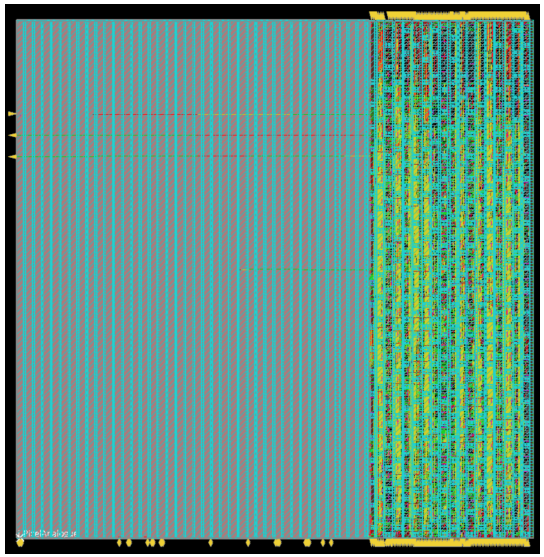

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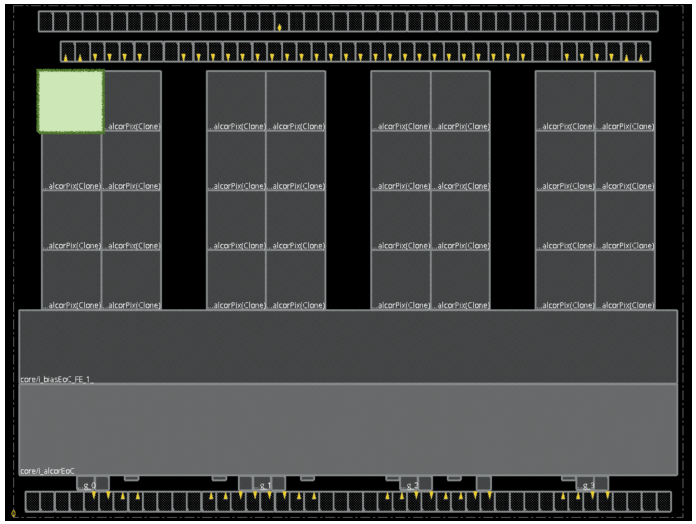

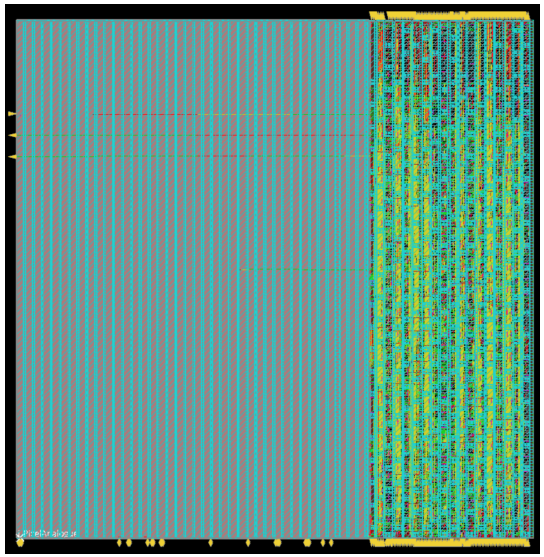

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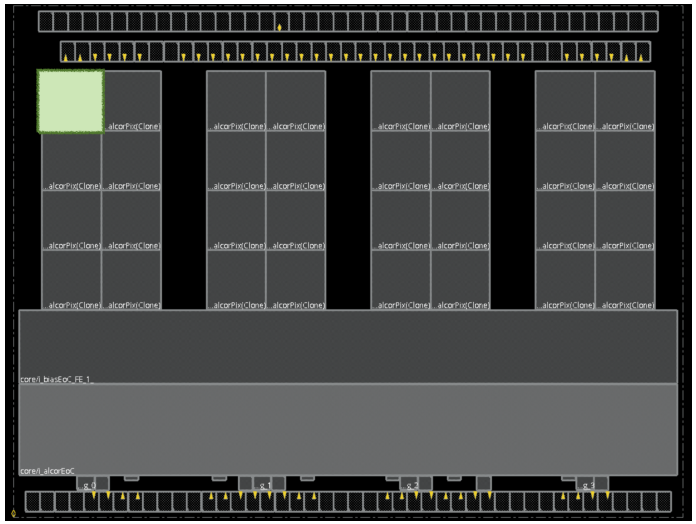

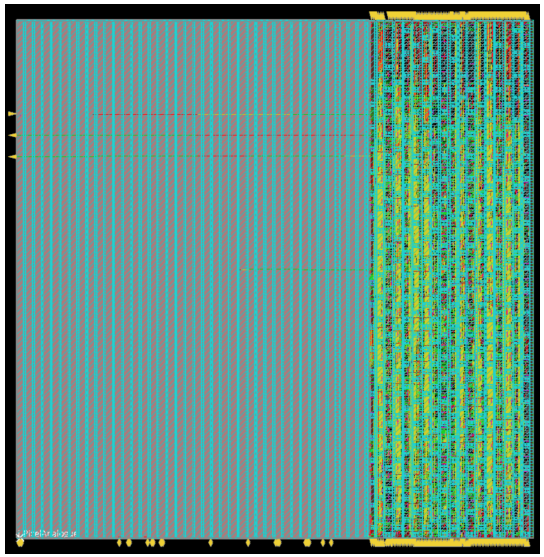

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Towards a Low Background Cold Digital SiPM tile, in a nutshell

- Explore integration solutions towards the development of an active silicon interposer for LAr DM detectors
- Effort on the reduction of radioactive background of the photoelectronics
- Short-term validation target: Exploring fully compatible solutions with existing module design for DS-20K
- What's Next: mixed-signal prototypes will include event digitisation and data multiplexing
- Data-driven very low-power architecture and data multiplexing used on networks of smart photosensors future massive detectors
- Single-photon time-tagging with smaller sensor pixels could be a strong candidate for **frontier dark-matter and neutrino experiments**
- A first version of the ALCOR chip ready for submission by Fall 2018
- A reference foundry was selected by INFN, started technical assessment for advanced sensor integration and development of large active silicon interposers using stitching

INFN TORINO

Weishuai Cheng, Fabio Cossio, Manuel Da Rocha Rolo, Giulio Dellacasa, Raffaele Aaron Giampaolo, Ramshan Kugathasan, Alejandro Martinez, Marco Mignone, Alessandro Razeto, Angelo Rivetti, Richard Wheadon