AMAC chip

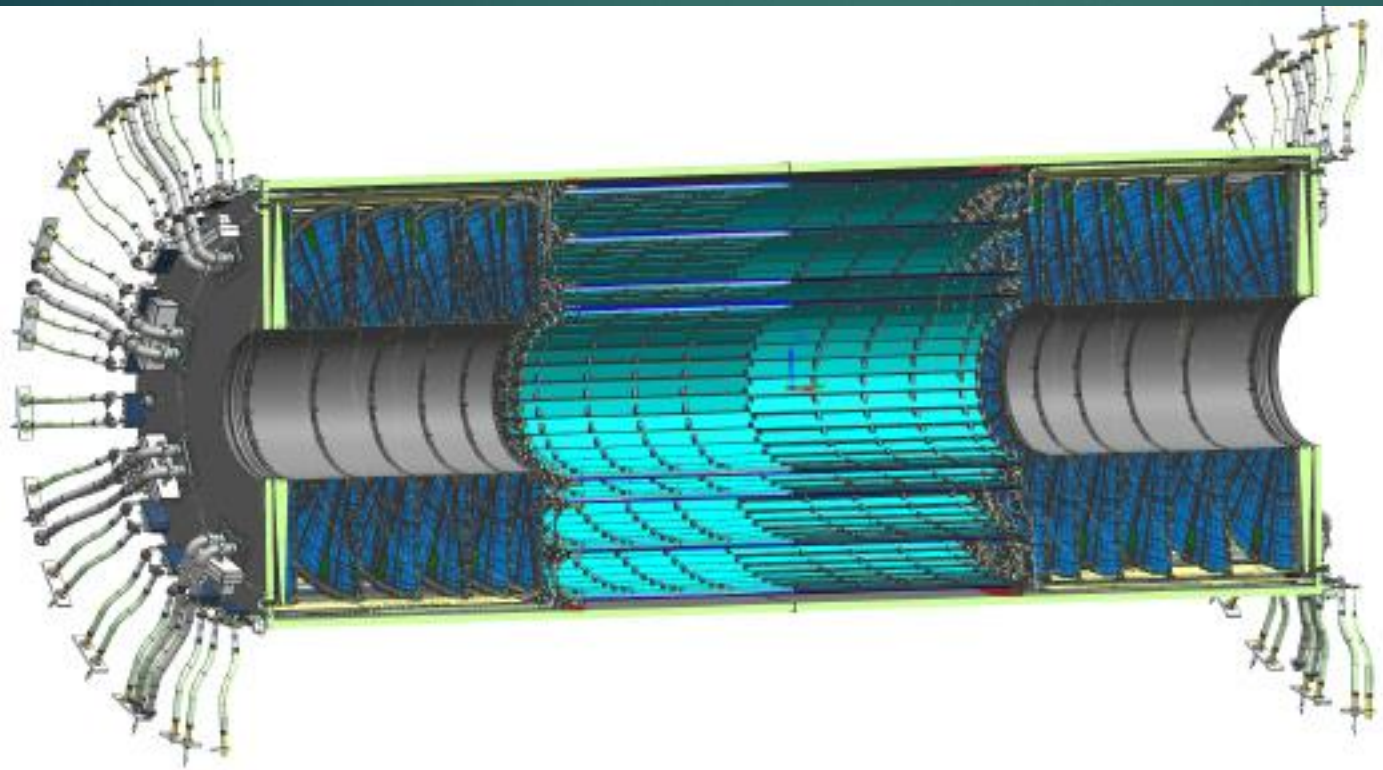
Autonomous Monitor And Control

Design Team: *BILL ASHMANSKAS. NANDOR DRESSNANDT, PAUL KEENER, MITCH NEWCOMER, ADRIAN NIKOLICA*

FOR THE ATLAS STRIPS COLLABORATION

ATLAS ITK Strips Structure & Environment

Low power, low mass rad hard environmental measurements(V, I, temp) at the module level with granular supply control is Essential to the Strips system design

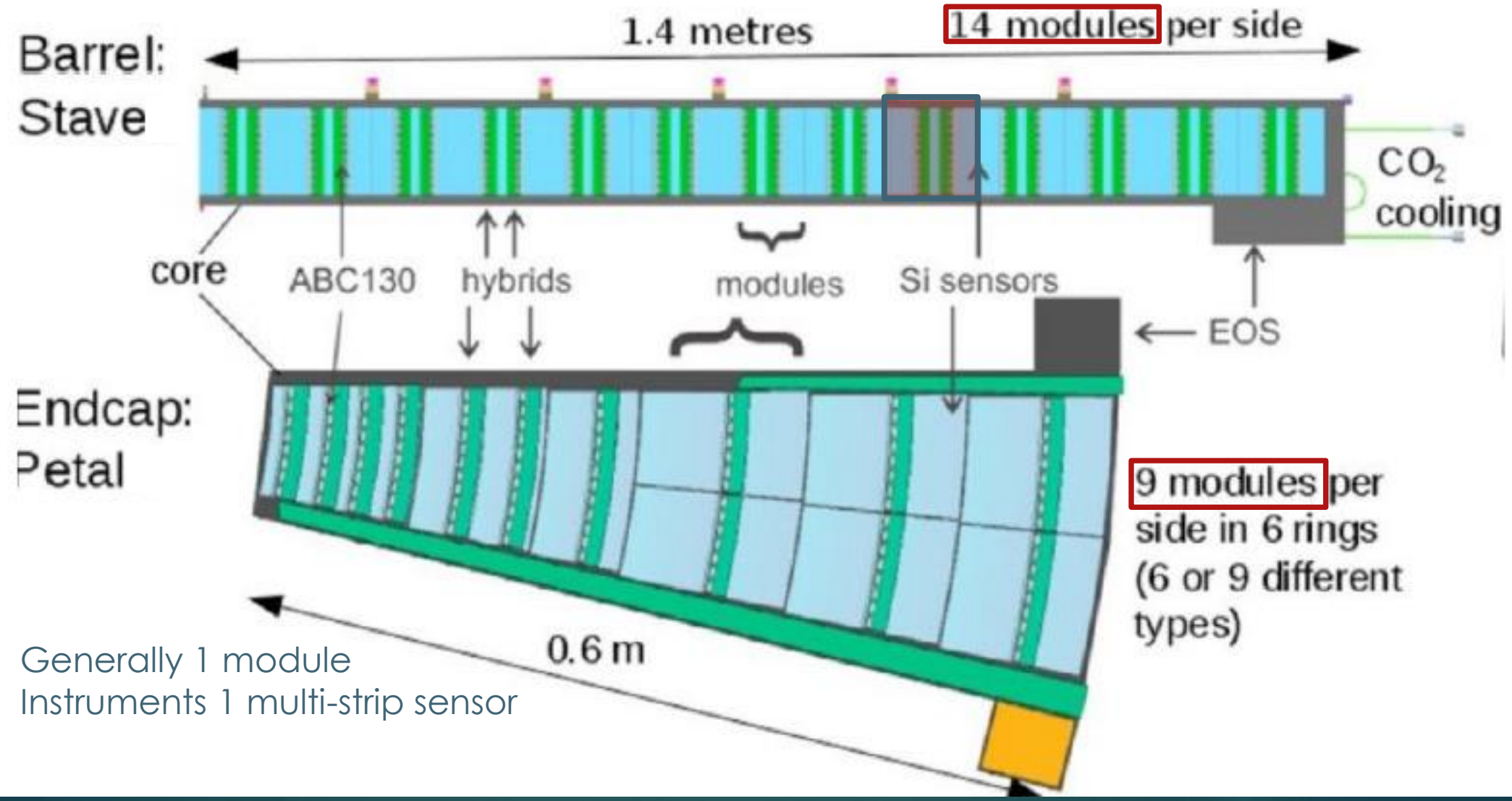


60M Strips
18k modules
@ -20C

~ 66MRad (500KGy) TID
~ $2*10^{15}$ (1MeV eq.) n/cm^2

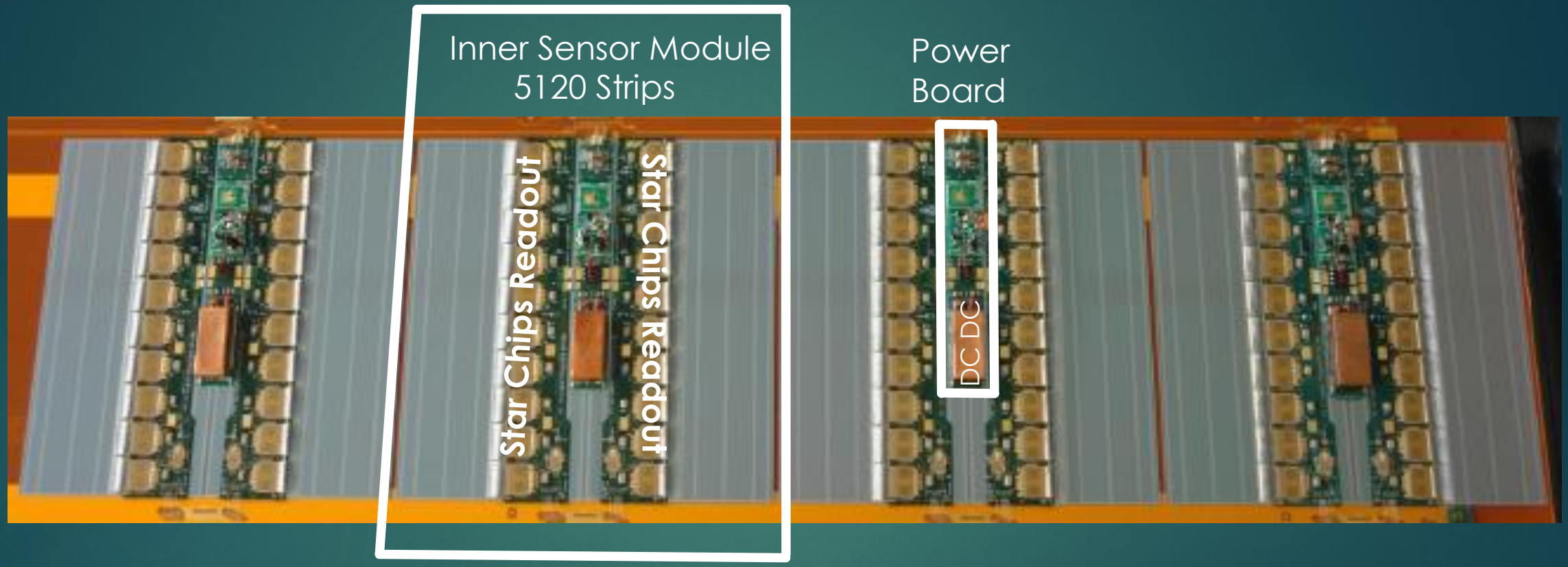
A new strips tracker for the upgraded ATLAS ITK Detector.
Jinst, 11th International Conference on Position Sensitive Detectors

Barrel Staves and End Cap Modules



Generally 1 module
Instruments 1 multi-strip sensor

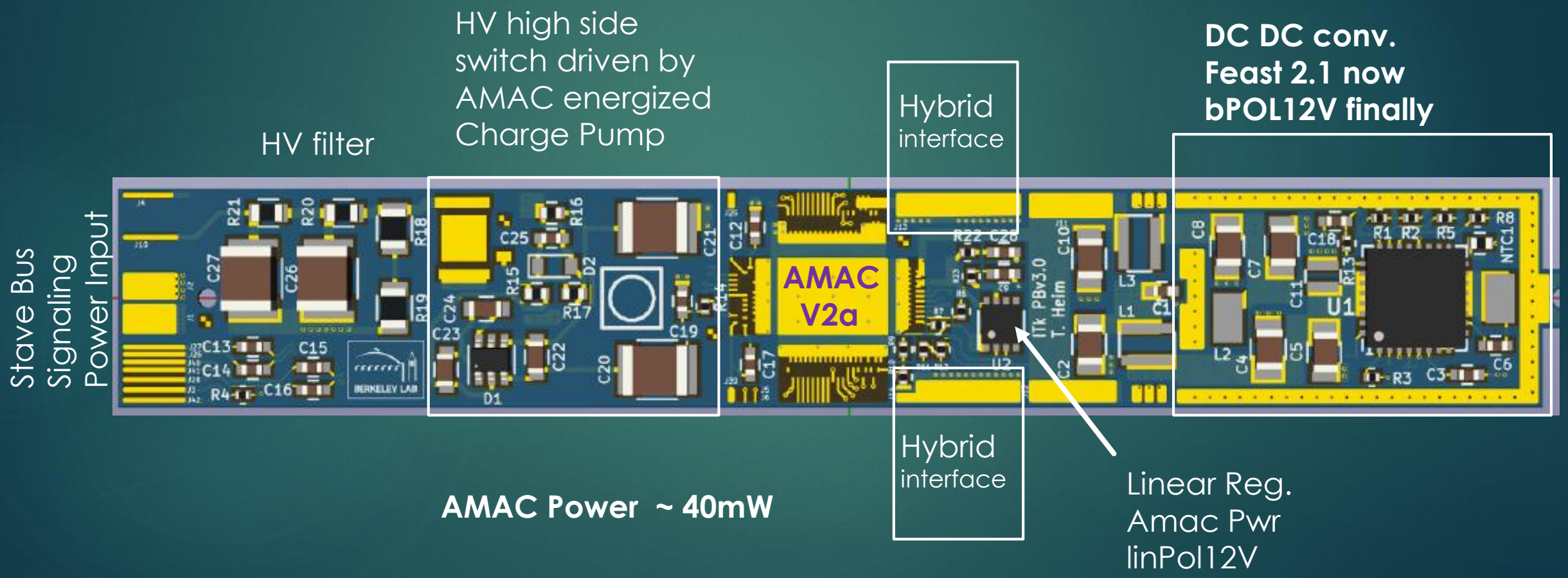
Barrel Module example



Module Power ~ 7.5 to 9.5 Watts from DCDC converter
Sensor Bias Voltage Locally switched off up to 700V (500V baseline)
Operational Temperature -30C unpowered to -10C powered

Barrel Power Board* (9x72mm)

*End Cap Power Boards are different in physical form factor



AMAC functions/requirements

- **Control**: DCDC output power, set Low and High Power mode for star chips
  Switch off sensor HV (500V baseline). Improves HV granularity 4X.
- **Failsafe**
  - Provide alternative communication path to force reset HCC and ABC chip.
  - Reset power on next power board through its AMAC. First PB can be reset from EOS.
  - Respond to communications Reset signal from HCC.
- **Monitoring:** (10bit ADC) ~ 5% or better accuracy
  > 10 parameters simultaneously within less than 1 second.
  - Voltages: DCDC input / output, Internal Regulated Supply/bandgap.
  - Temperatures: 3 external NTC's, Internal CTAT, bandgap PTAT.
  - Currents: Sensor Bias return, DC DC input/output.
- **Limits**
  - Programmable Window warning with optional interlock.
- **Calibration:** 2 calibration for ABC's (also 2 current shunt references) 8 bit D/A's.
  Can switch internal power from Linear Regulator to DCDC converter.

AMAC_V2 Low BW communication

I2C dropped in AMAC V2 in favor of Differential communications.

- Bussed unidirectional lines: CMDin and CMD/Data out differential pairs

Single LPGBT elink transmits to all AMACs (max 14) on a stave or petal.

Single LPGBT elink receives data/status from all AMACs. stave or petal.

- ***AMAC does not depend on the system clock. Uses its internal ~ 40MHz clock***
- Communication protocol *Endeavor, uses long and short pulses for 1's and zero's*
  Local Clock Pulse Counting: Hi=6<n<22, Lo=29<n<128 Bit Interval 11<SP<75
- Each Command sent to AMAC elicits a handshake AMAC response.

→ up to 14 AMACs on RX and TX differential pairs.

AMAC **Receivers** AC coupled with hysteresis memory / deglitched

AMAC **Drivers** DC coupled /BWL on bus with Tri-State outputs.

AMAC V2 Design Environment

Design Flow -

130nm CMOS Process PDK

Digital On Top with analog macros

Design environment

Cadence Innovus / Genus / Virtuoso

Analog Design / Simulation ADE - XL

Digital Verification Framework

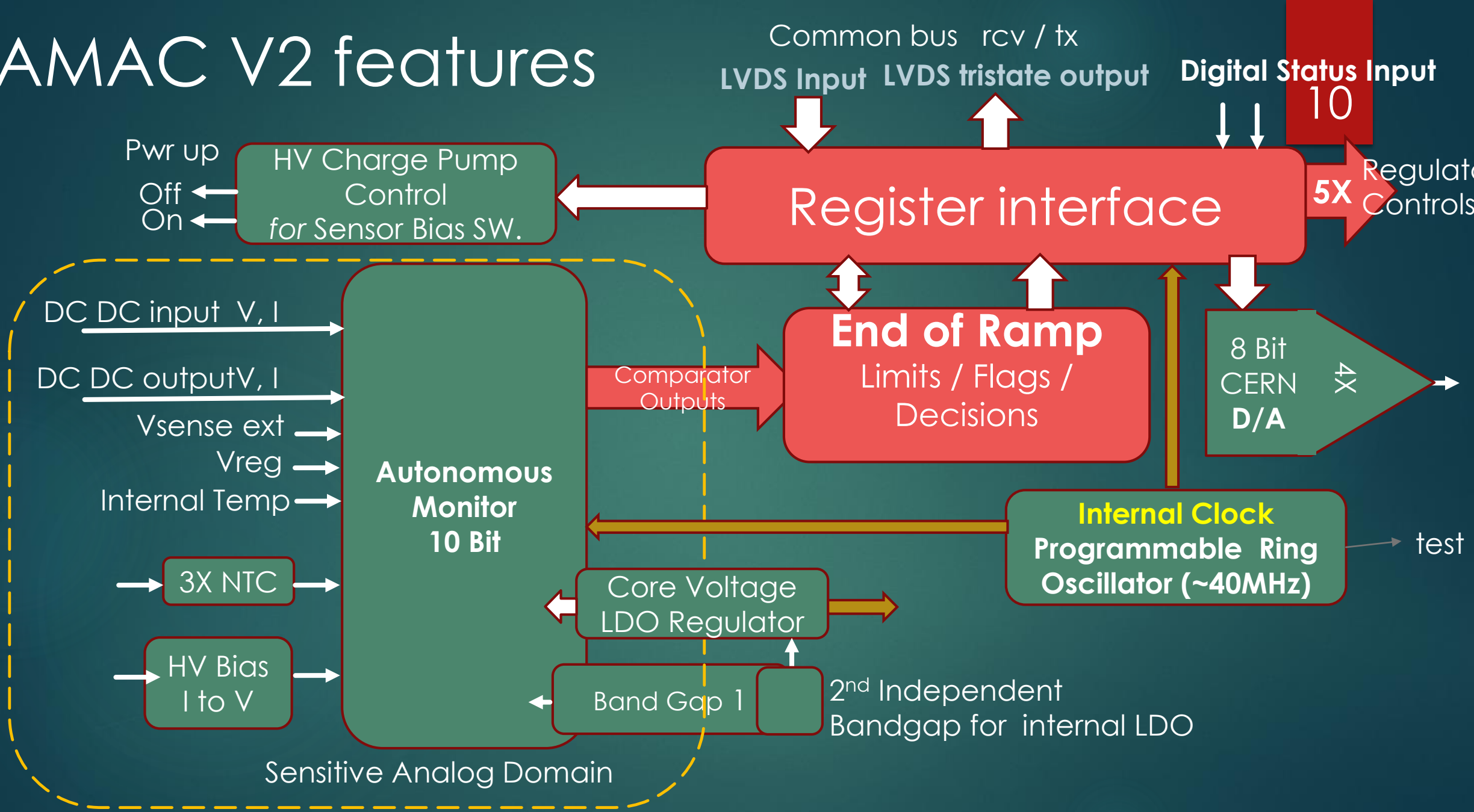
- Top-level testbench is written using cocotb*
  - Allows test vectors to be manipulated using Python
- Testbench code yields control to the Cadence simulator, where stimulus is injected or results are read back.
- Refer to http://potential.ventures/cocotb
  http://cocotb.readthedoxs.io/en/latest/introduction.html#how-does-cocotb-work

This verification is also used for the Star Chipset including multi-ASIC simulations.

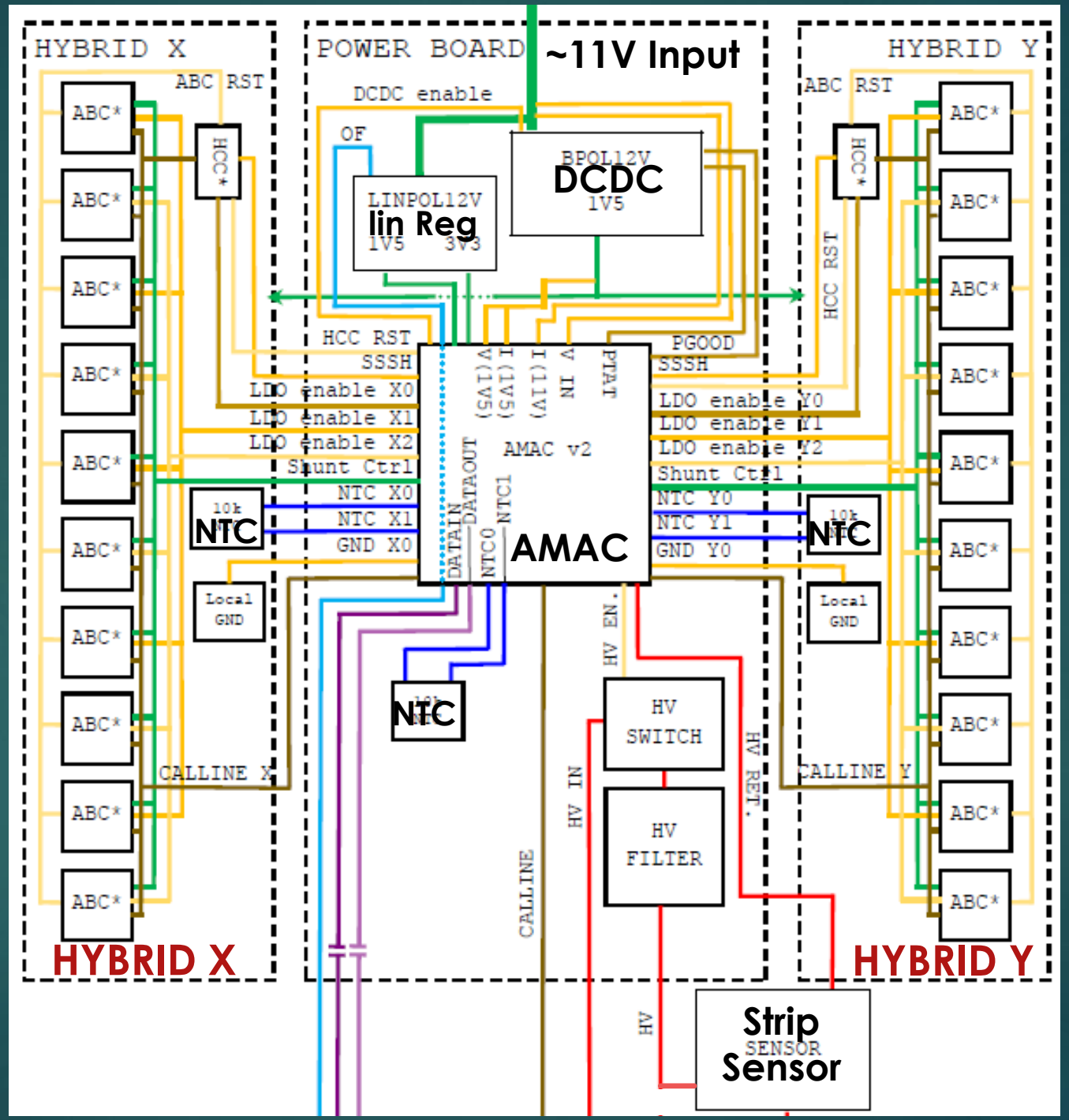
Basic Functional control connectivity including polarity checks among AMAC, HCC and ABC have also been implemented and tested by Verilog simulation.

* Implemented at Penn by Bill Ashmanskas, Ben Rosser, Adrian Nikolica

AMAC V2 features

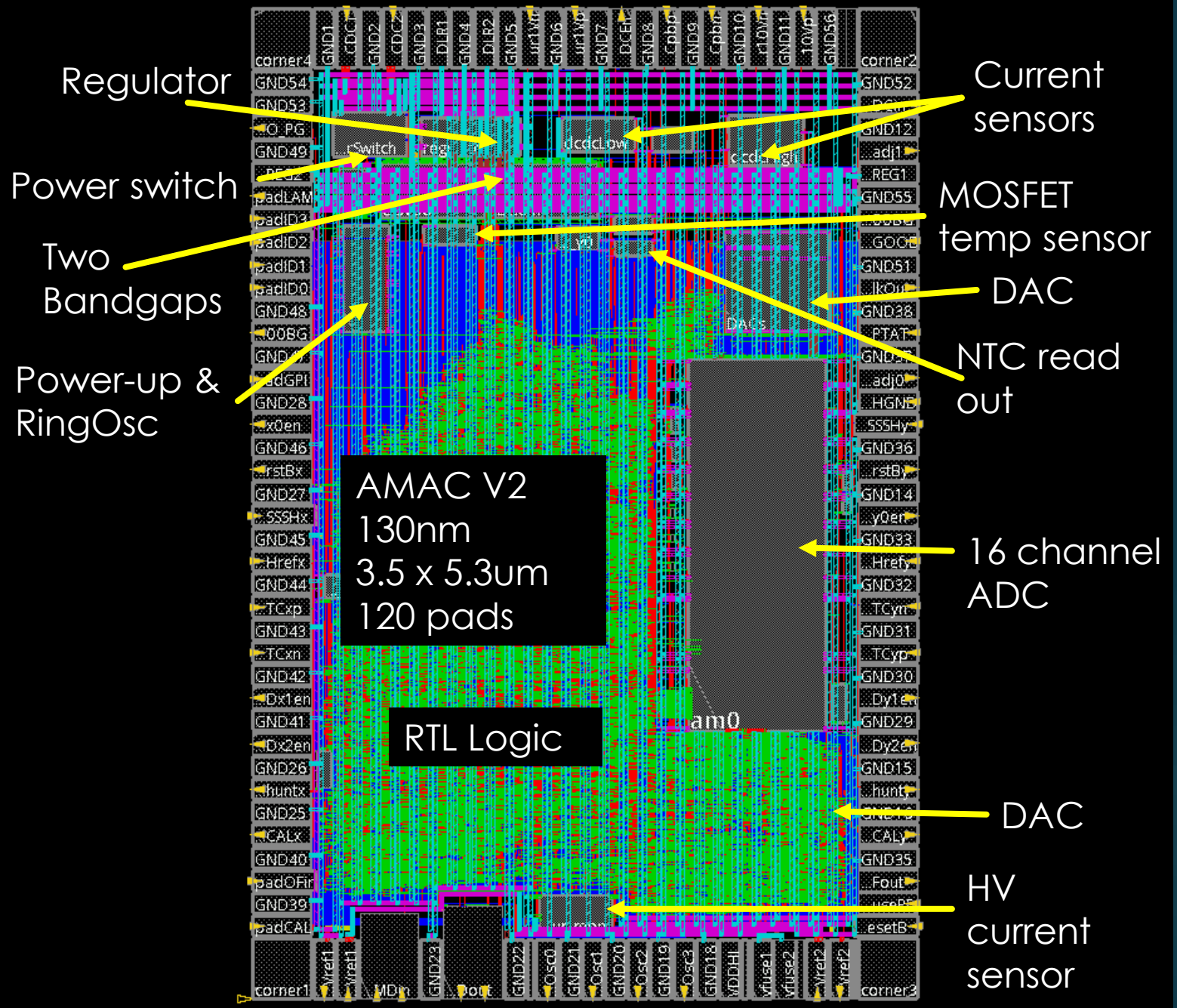


Module hookup



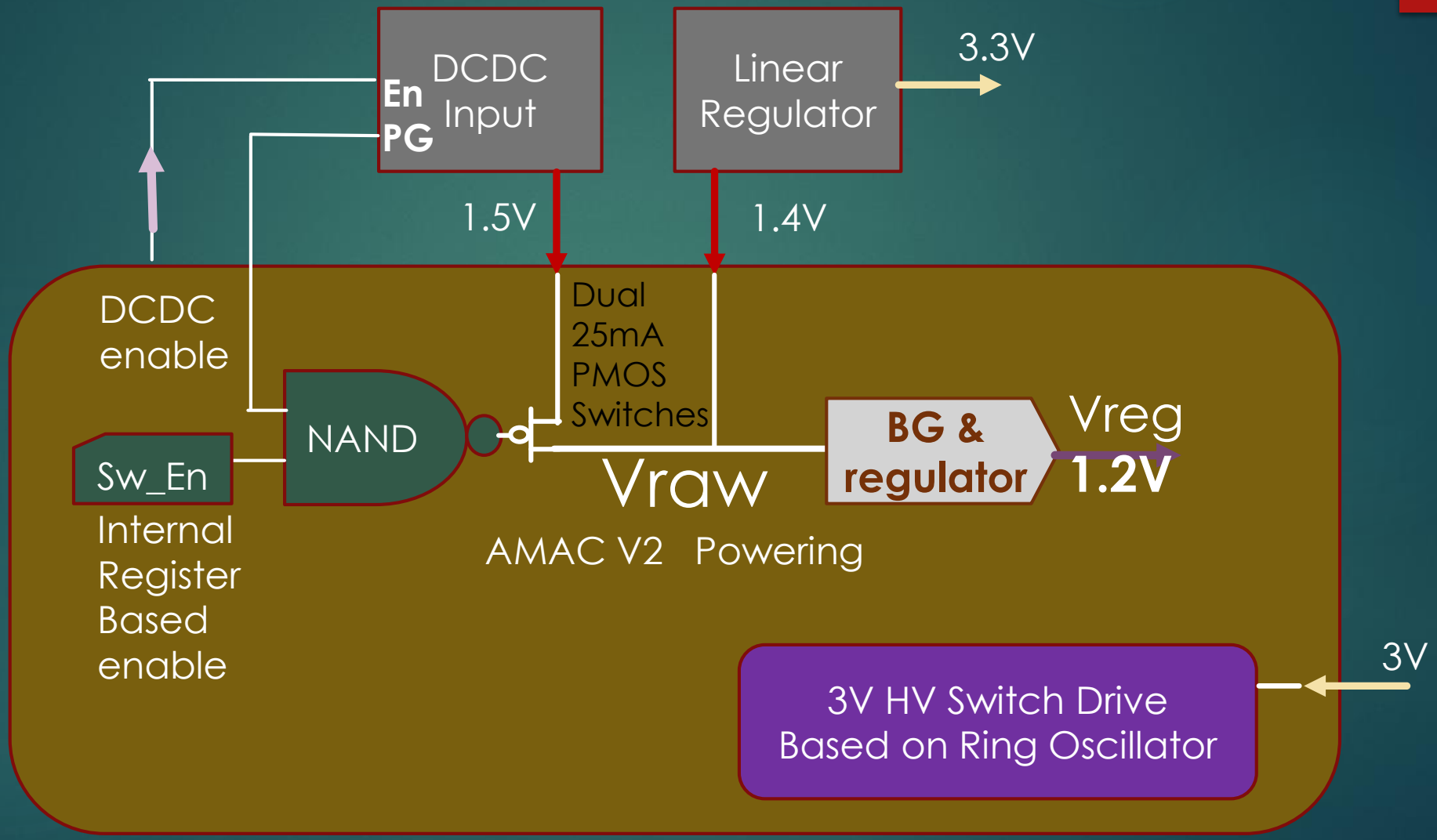
Analog Blocks

- Voltage Regulator & Bandgaps
- Ring Oscillator (with Power Good Output)
- Analog Monitor
  - Integrating DAC
  - Comparator
- Voltage Measurements
- Temperature Measurements
- Sensor Bias Current Measurement
- DCDC Current Measurements
  - Input (@ 10-14V)
  - Output (@ ~ 1.5V)
- CERN DACs
- LVDS (like) I/O - sub 10MHz
  - Receiver
  - Driver
- Power Switch



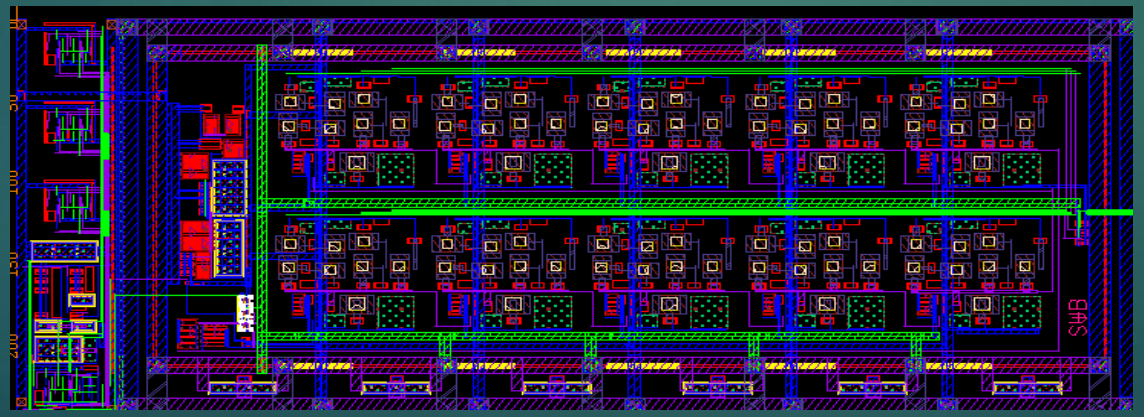
Powering AMAC

This approach allows a variety
Wire options Including DCDC only.



Ring Oscillator with *Power Good* Signal

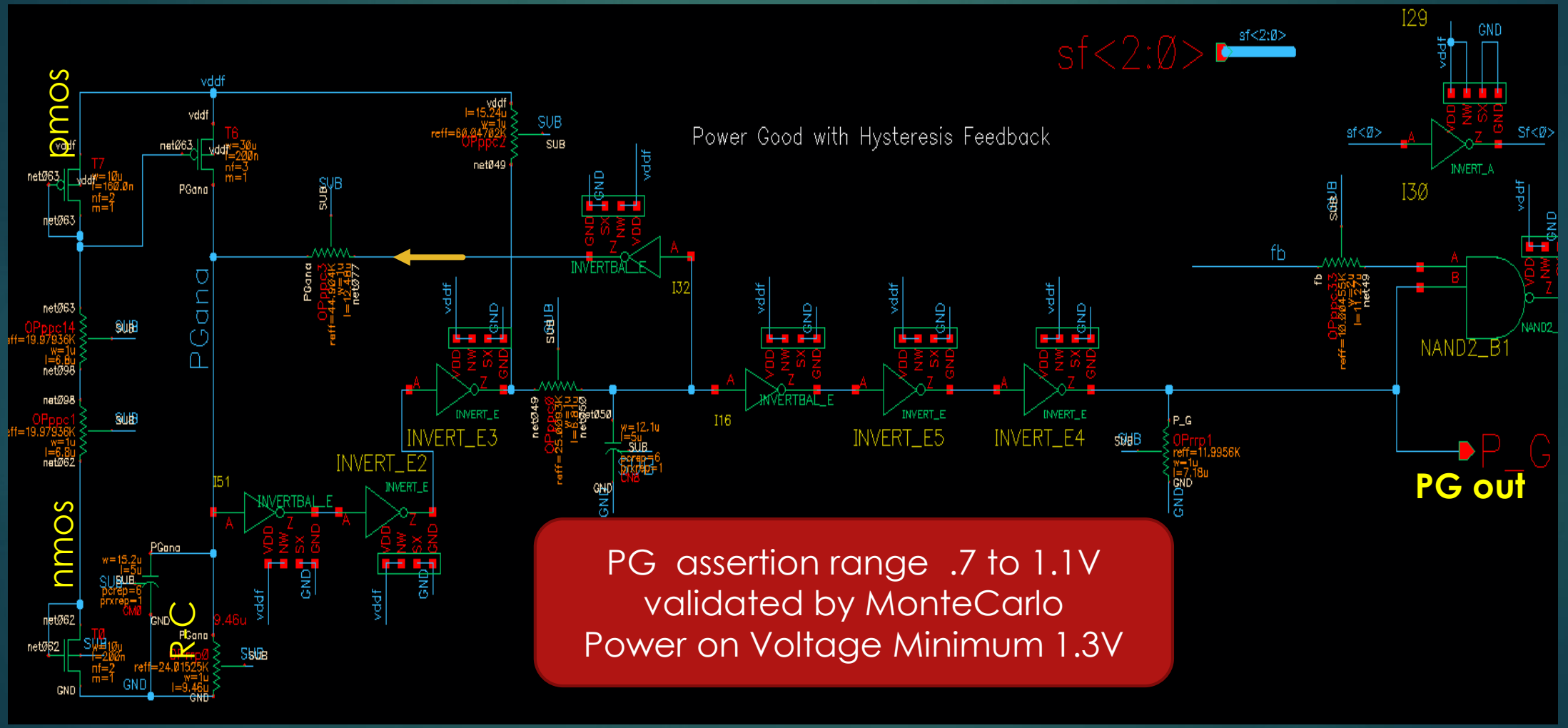
Ring Oscillator Characteristics	
Supply Voltage	1.2V±.1 @ 210µA
Area	243X507µm
Target frequency	40MHz
Programming Range	32 – 47MHz
Outputs	PGood and CLKout (CMOS logic)
Inputs	Sf(0:2) (CMOS logic)



Power Good requires NMOS & PMOS mirror

Functionality + multiple Inverter response.

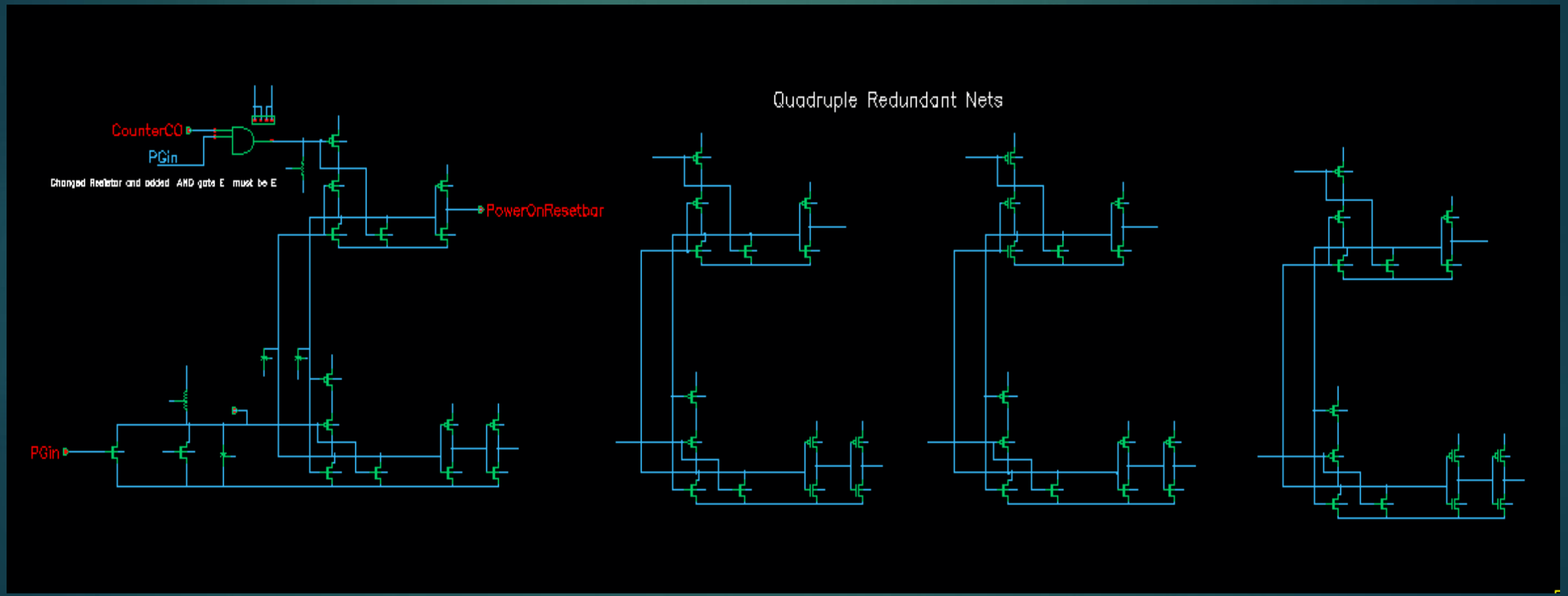
Hysteresis FB ensures 200mV drop before changing state



PG assertion range .7 to 1.1V
validated by MonteCarlo
Power on Voltage Minimum 1.3V

Quadruple parallel wired nor Latch Block

manual layout separation > 25um provides SEU protection.

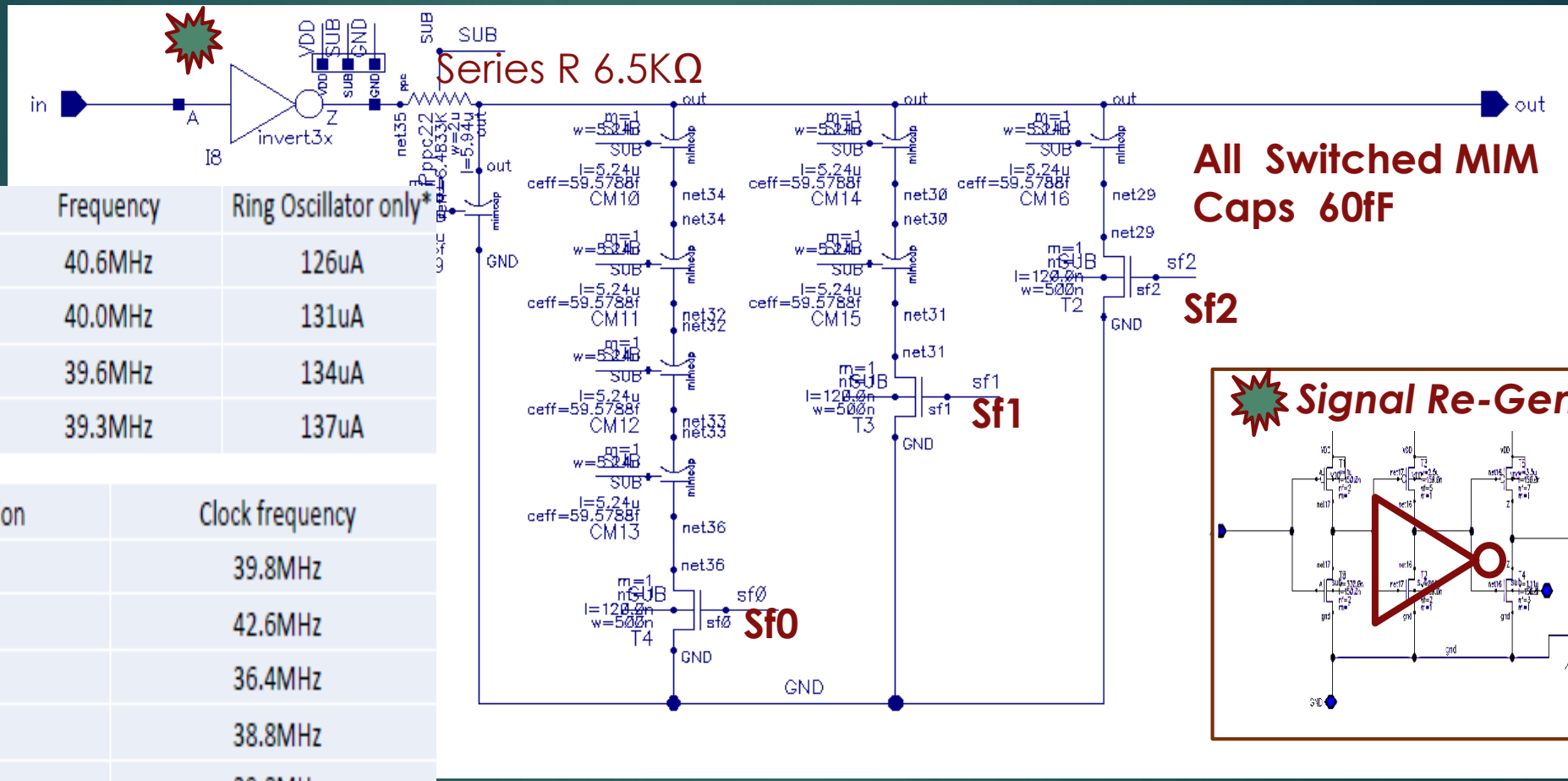


One of 10 Ring oscillator Delay Elements

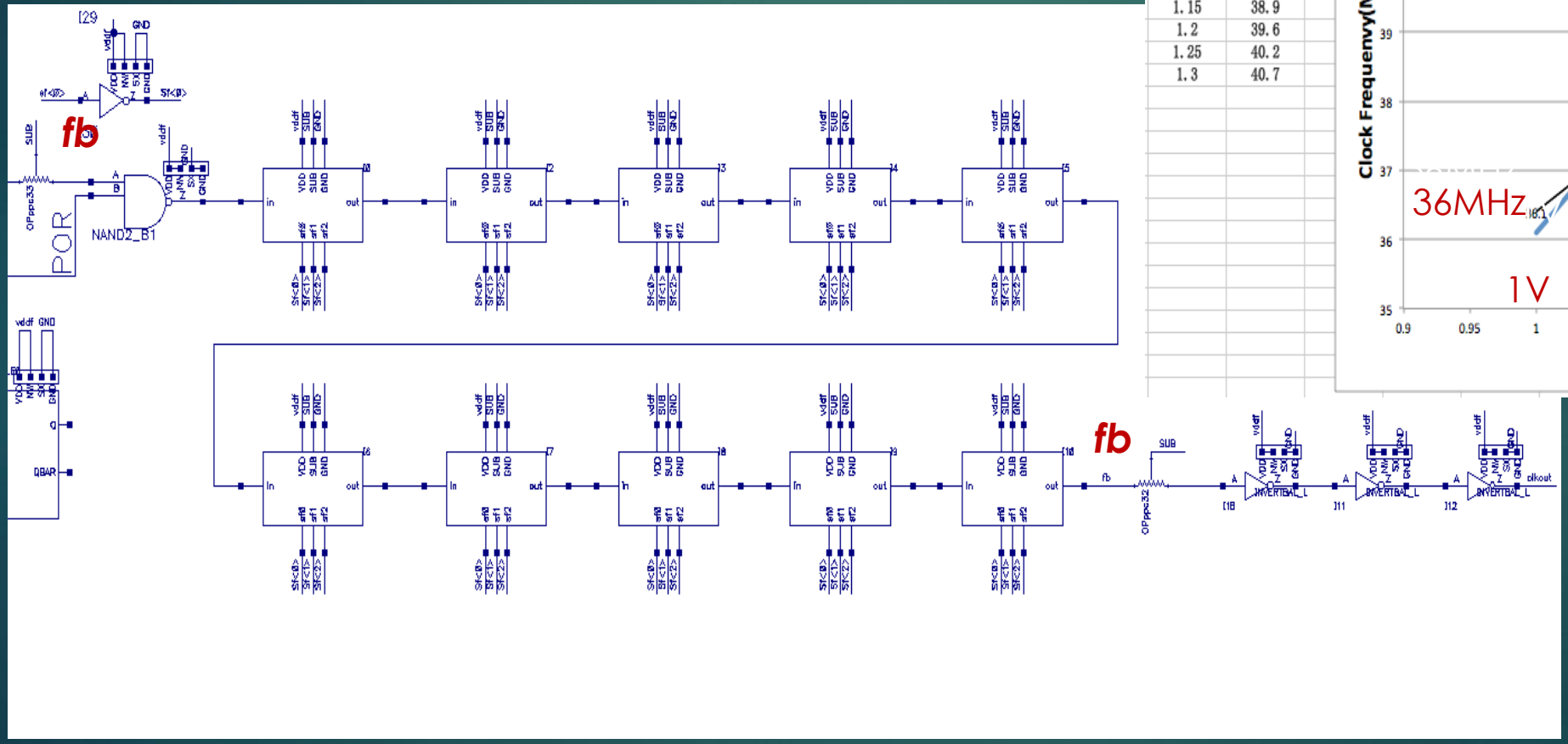
Communications Requirement +/-25% freq.

Temperature	Frequency	Ring Oscillator only*
-40C	40.6MHz	126uA
0C	40.0MHz	131uA
25C	39.6MHz	134uA
50C	39.3MHz	137uA

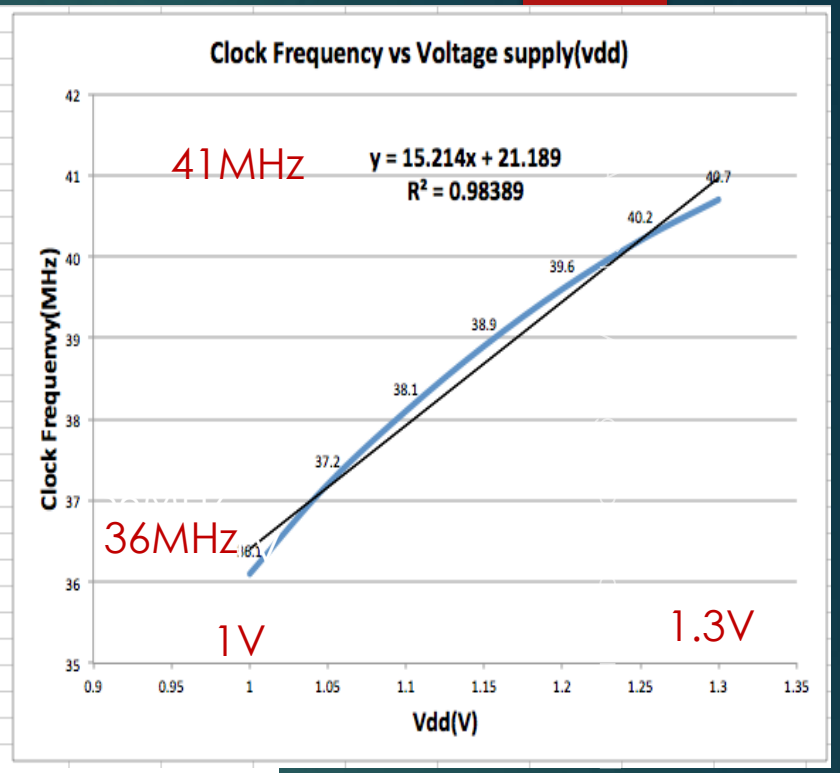
Process variation	Clock frequency
tt	39.8MHz
ff	42.6MHz
ss	36.4MHz
fs	38.8MHz
sf	39.8MHz



Ring Oscillator



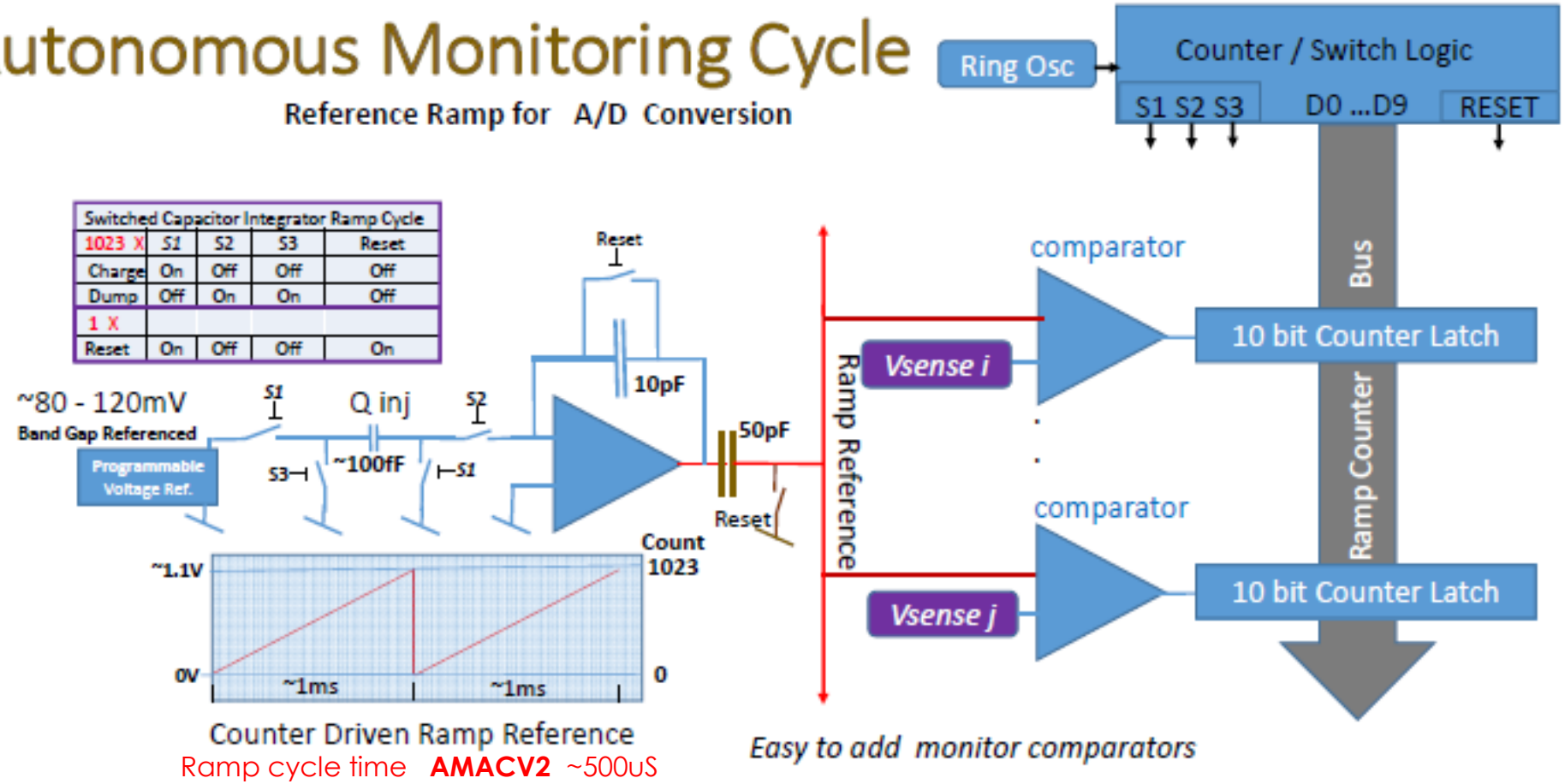
Vdd (V)	Freq (MHz)
1	36.1
1.05	37.2
1.1	38.1
1.15	38.9
1.2	39.6
1.25	40.2
1.3	40.7



Wilkinson Ramp Generator (ADC)

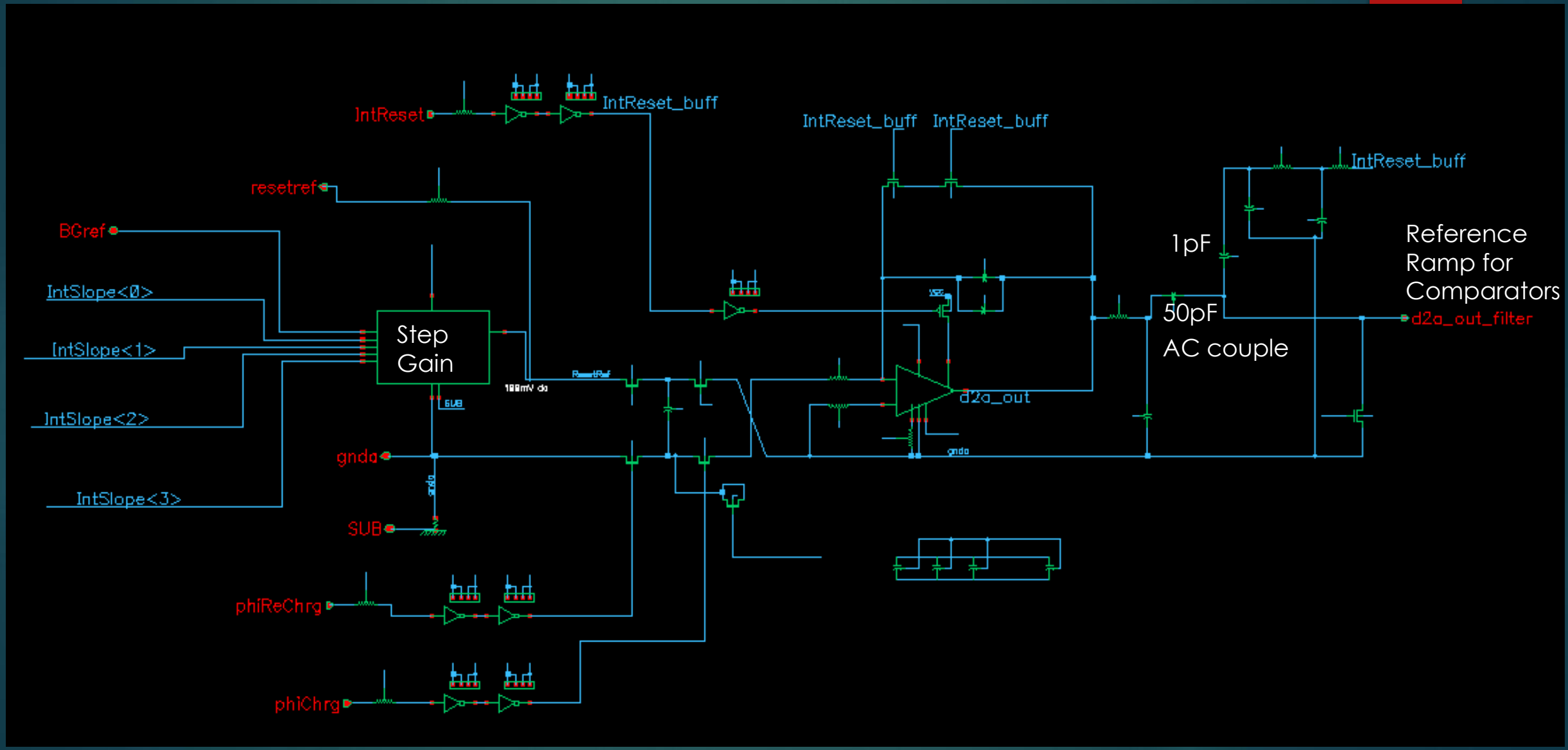
Autonomous Monitoring Cycle

Reference Ramp for A/D Conversion

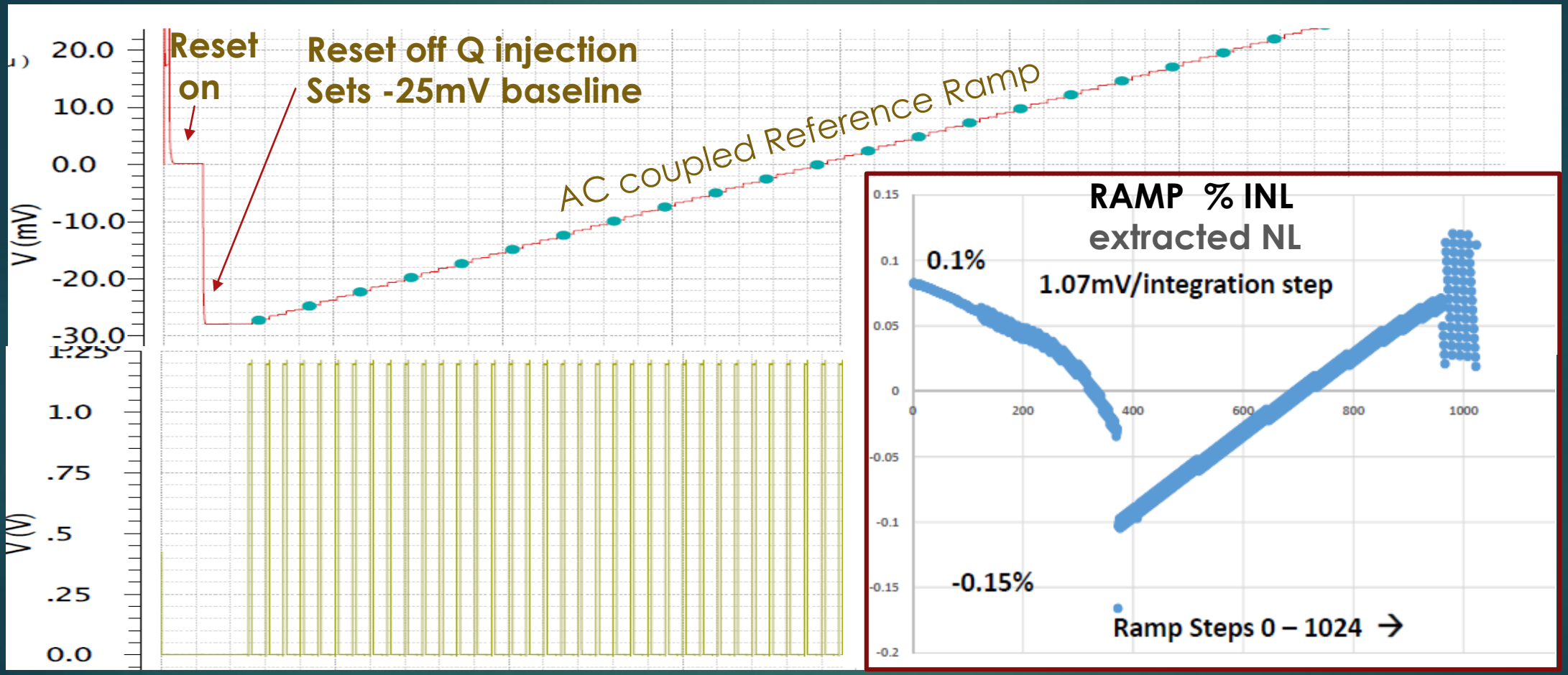


Tuning capability- the programmable Voltage reference 80 to 120mV allows the unit step to be set to ~ 1mV/cnt.

Integrating DAC Implementation



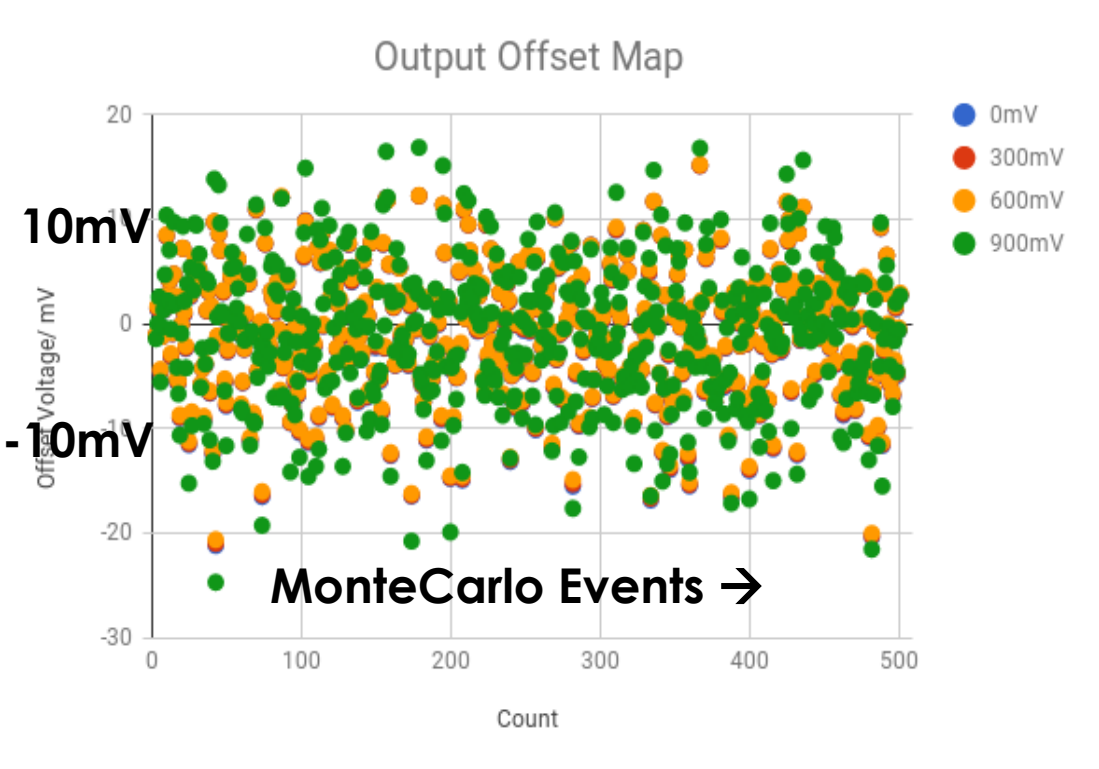
Ramp Characteristics



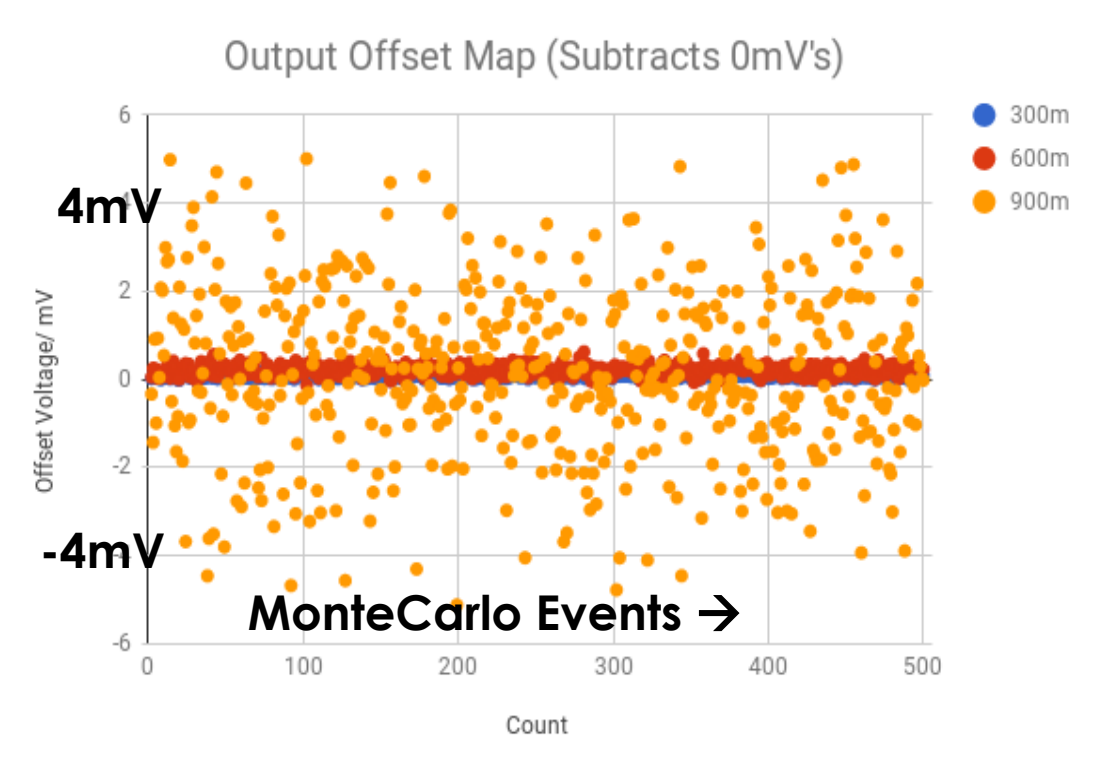
Calibration Mode

Switch Comparator input to 0V & calibrate 0V then subtrace 0 calib from Measured parameter value.

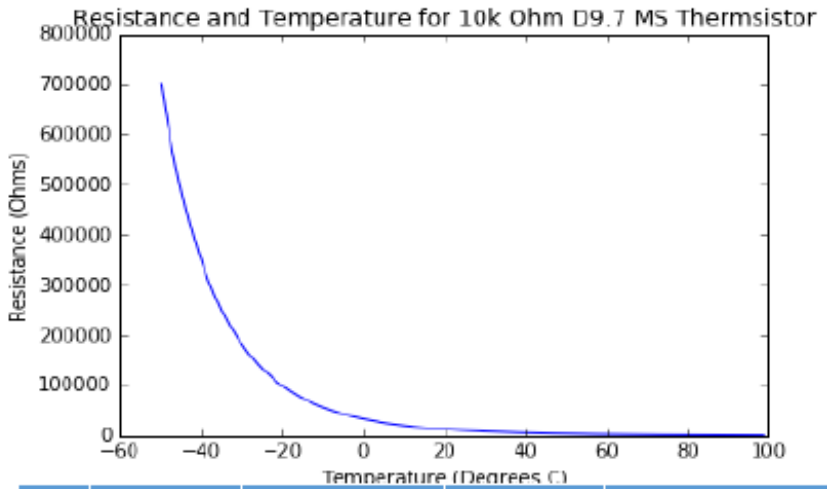
RAW Measurement



Calibration Measurement



NTC Temperature Measurement

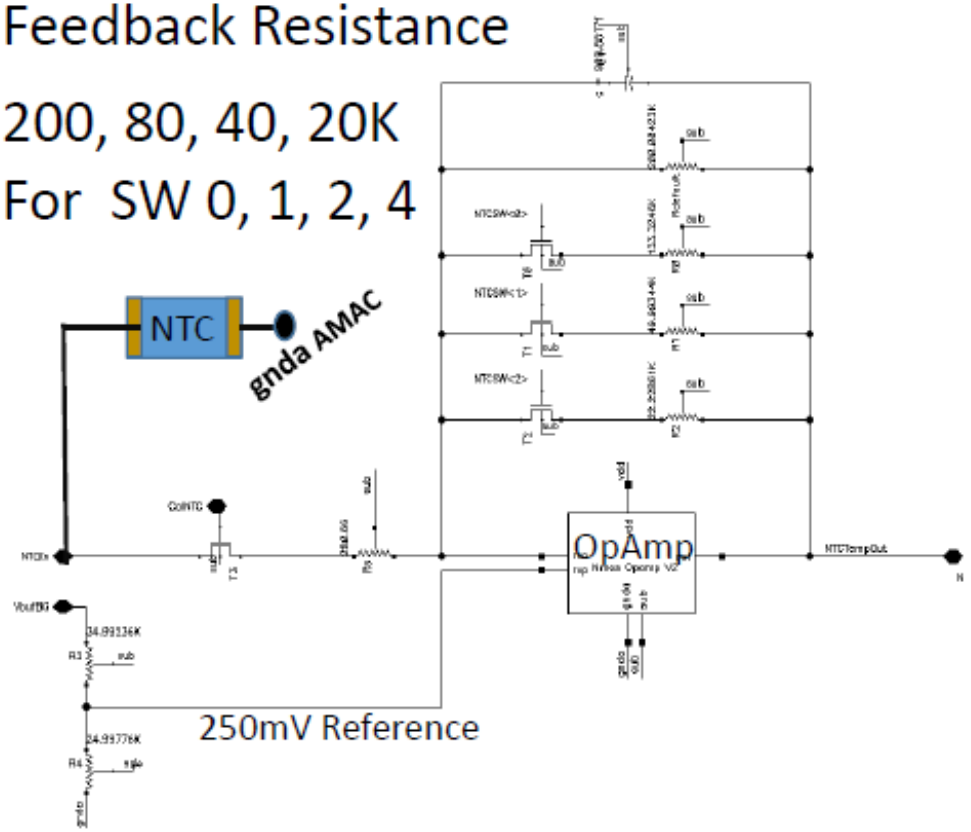


Sl no.	ON	OFF	NTC resistance	Temperature range
1	-	All	67K to 700KΩ	-45 ˚C to -18 ˚C
2	NTCSW<0>	NTCSW<1> NTCSW<2>	27k to 400 K	-40 ˚C to 0 ˚C
3	NTCSW<1>	NTCSW<1> NTCSW<2>	13.5 to 226K	-35˚C to +20 ˚C
4	NTCSW<2>	NTCSW<1> NTCSW<2>	7.5K to 115K	-22 ˚C to +30 ˚C
5	NTCSW<2> NTCSW<1>	NTCSW<0>	3.6k to 80k	-10 ˚C to +55 ˚C

Feedback Resistance

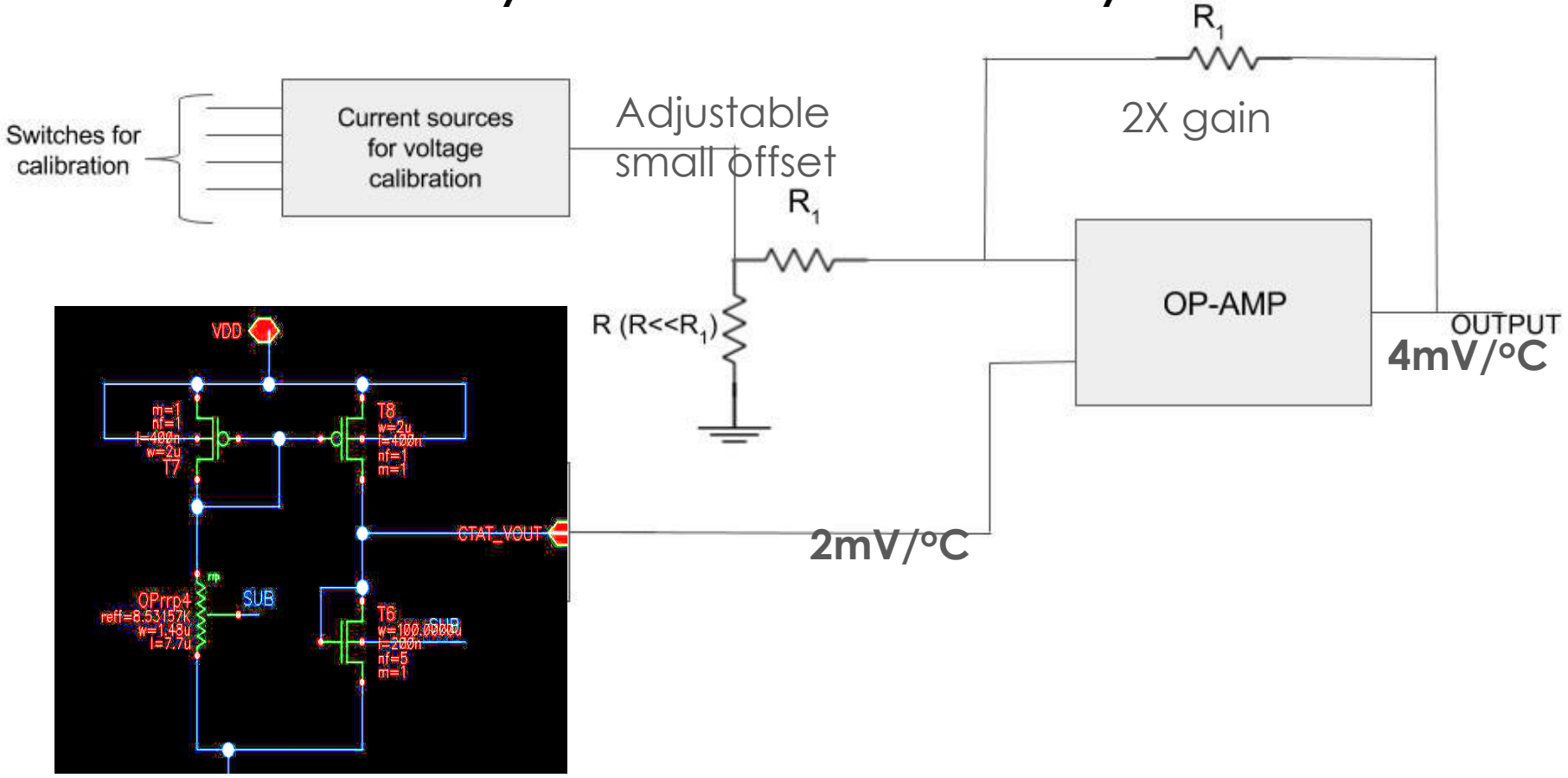
200, 80, 40, 20K

For SW 0, 1, 2, 4



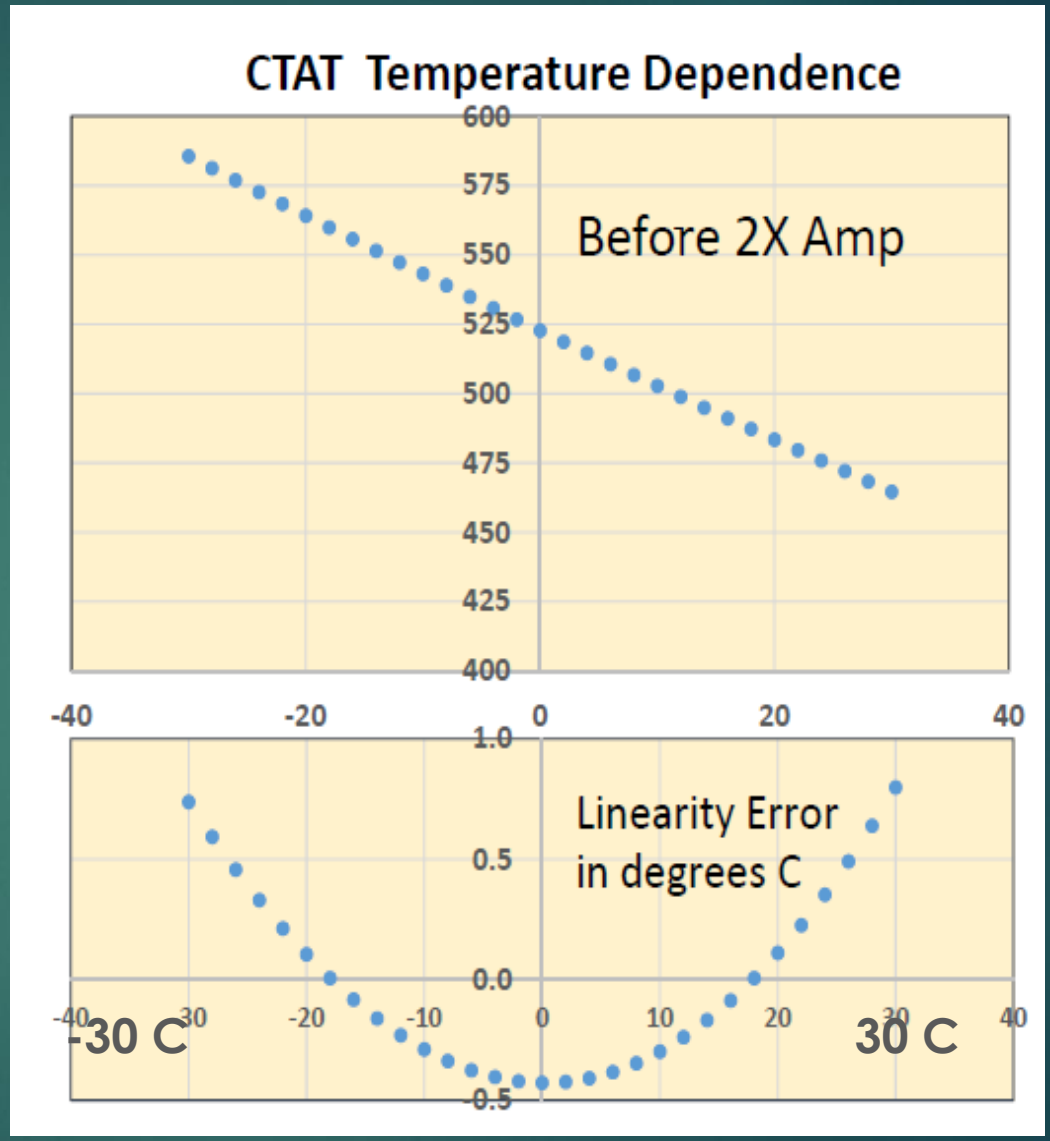
On Chip NMOS Temperature Sensor

Newly Added On AMAC V2a only



MOSFET temp sensor

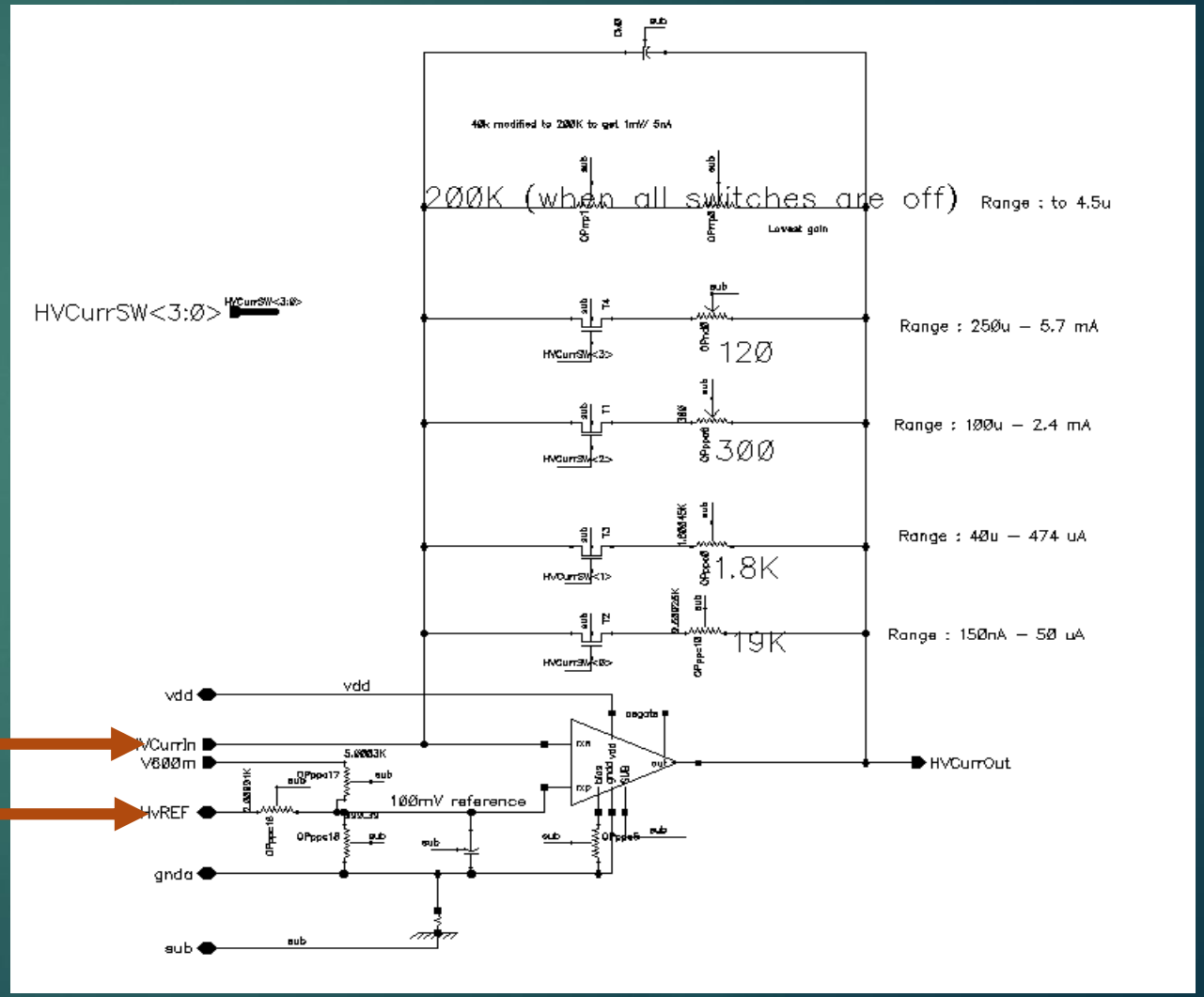
Slope 2mV/°C
Linearity error < 1°C
Supply Variation 2.5°C/100mV
Process Variation: < 10% in slope
~150mV in offset



Sensor Bias Current Measurement

Range 20nA to 10mA

- OpAmp Designed for up to 10mA sustained (sensor current)
- 5 ohm output impedance
- Input reference is 100mV
- AMAC Input protection will source sensor bias current in the event the op amp fails.



DCDC high side Input and output current measurements

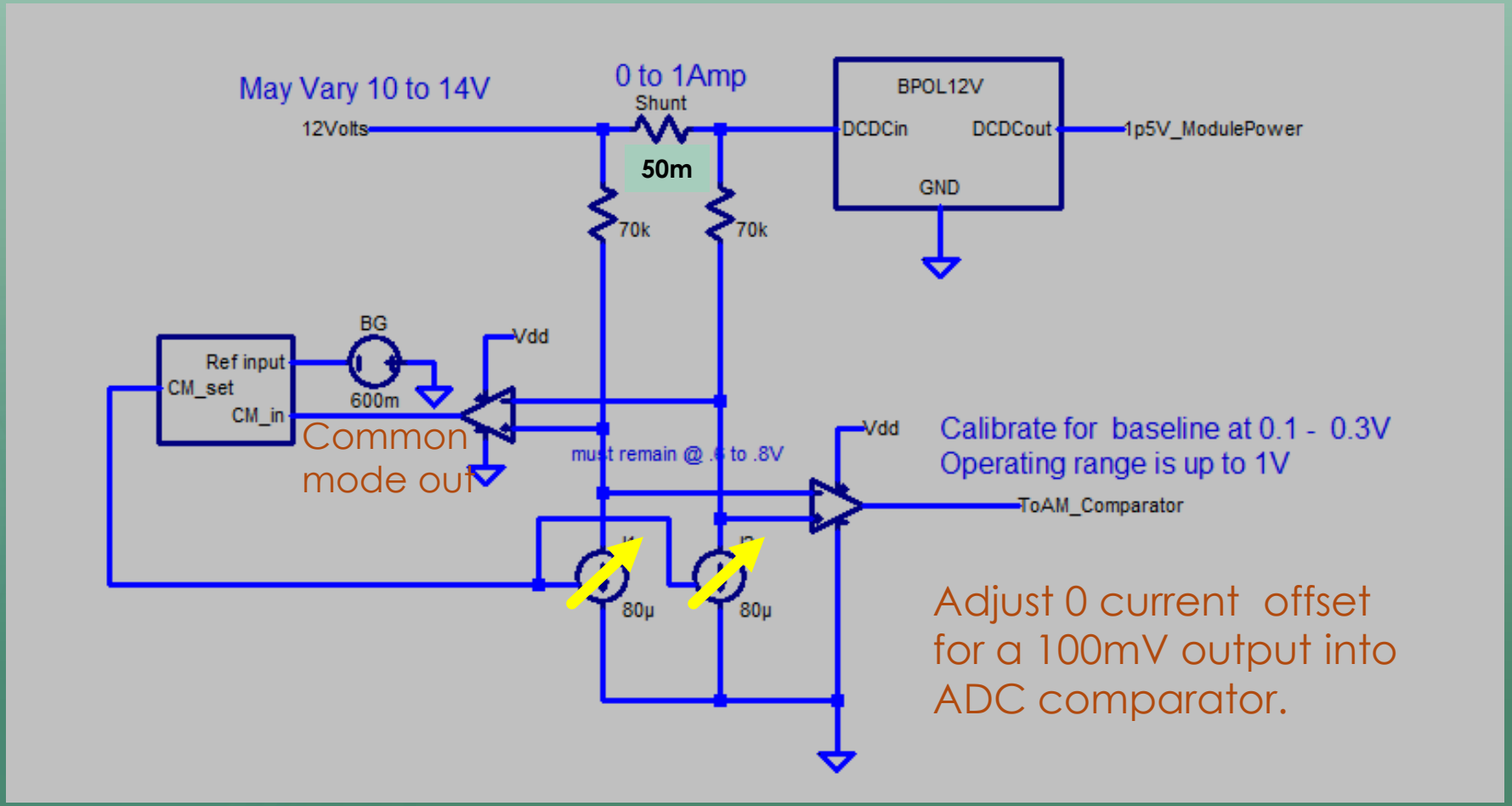
DCDC **Input Side** Shunt measurements.

- DCDC Input voltage 10-14 V
- Current: 0 – 1Amp (A maximum of 0.6 is expected)
- Shunt resistor 50 milliohms

Approach:

Use two matched high impedance current sources (with programmable trim) internally on AMAC and two matched external resistors to significantly reduce the amount of attenuation across the shunt resistor 0.6 to 0.8V.

Current Monitor Input Approach



Final ADC Measurements (abbreviated)

ADC Wilkinson Ramp 10bit type with multiple comparators

ADC value based on 1024 charge injection steps.

- Range -25mV to 1V
- Accuracy ~.1% of Full Scale 0-750mV ~.5% 750 to 1V
- 16 Ramp referenced comparators - each with a Zero Volt Calibration input MUX
- Ramp step counter recorded when ramp exceeds measured value twice.

4 LV supply values Two internal BG Voltages

High Side DCDC input Current, High Side DCDC output Current

Sensor Current

3 NTC and one internal Temp measurement

Calibration Voltage from End of Stave

3 Off chip ground reference voltages

4 8 bit, AMAC based D/A converter output voltages (CERN designed D/A's)

Experience with AMAC V1A

Measurement Results AMAC V1a on Power Board

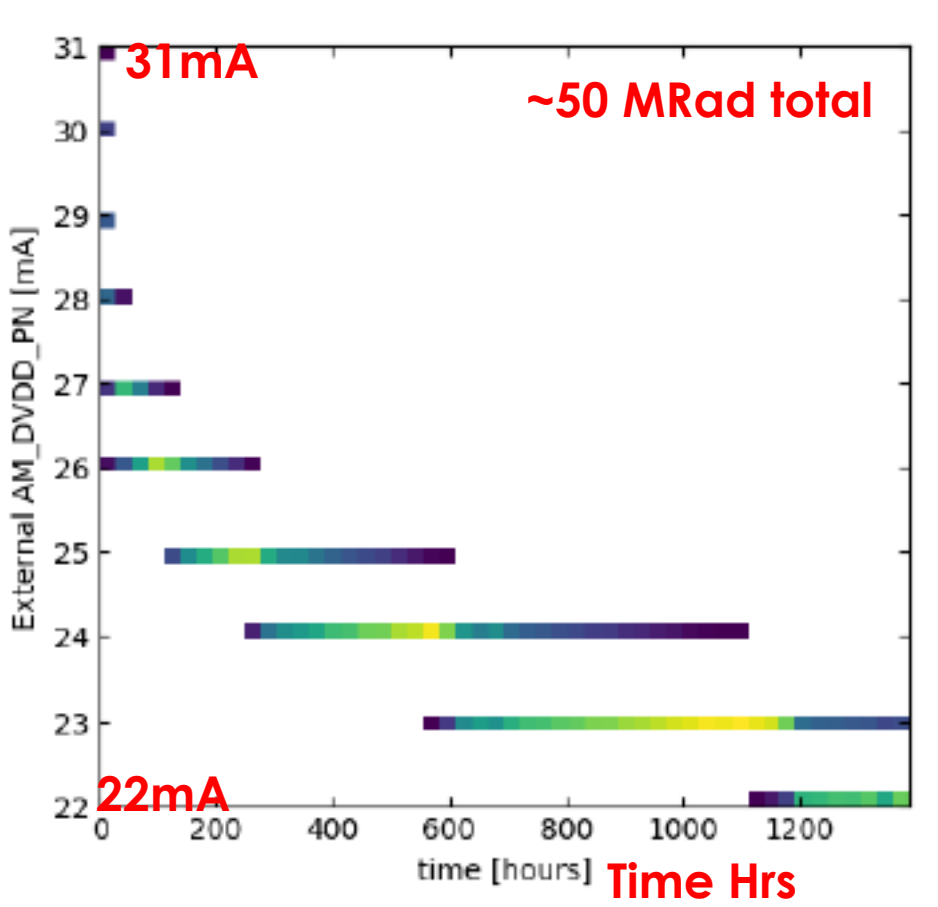
Monitoring and Control

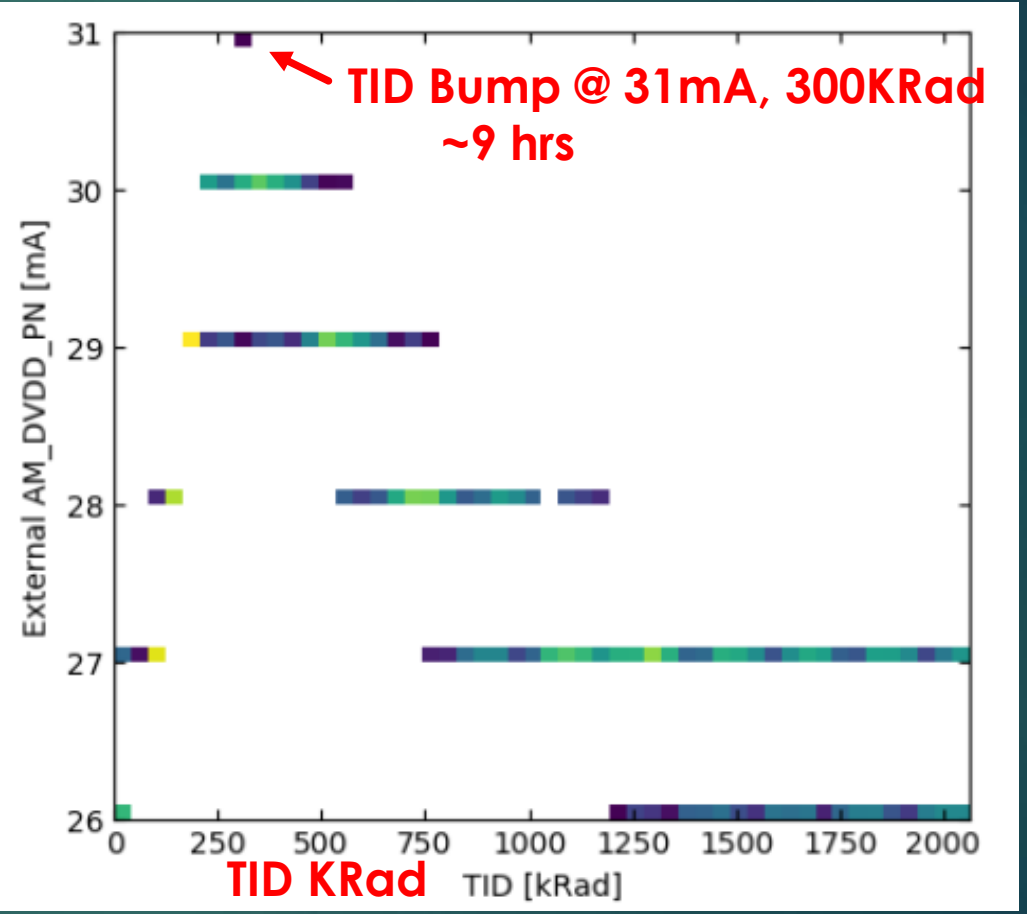
- AMAC monitoring of temperatures, voltages and LV currents successfully demonstrated
- Calibration of the AMAC comes from initial powerboard tests performed at LBL
- All monitored values within expectation
- HV and LV switching also works

Variable	Value	Notes
Chiller temperature	17 °C	
NTC temperature	17.4 °C (LV off), 23.5 °C (LV on)	
PTAT temperature	16 °C (LV off), 30 °C (LV on)	
Input voltage	10.938 V	PSU @ 11 V
Output current	2.06 A	Consistent with pre-PB
Output voltage	1.491 V	Confirmed with DVM

TID tests @ BNL AMAC V1a

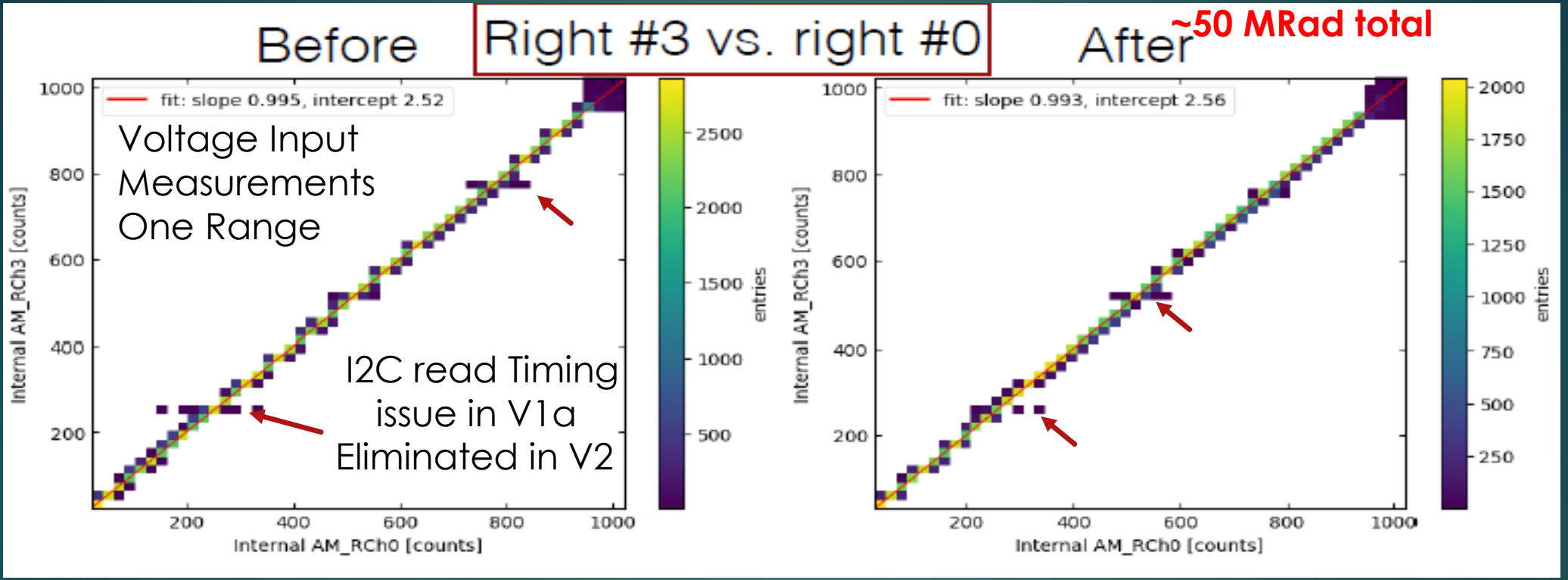
Exposed to .85 MRad/day for 58 days @ Room Temp (296°C)





TID tests @ BNL AMAC V1a

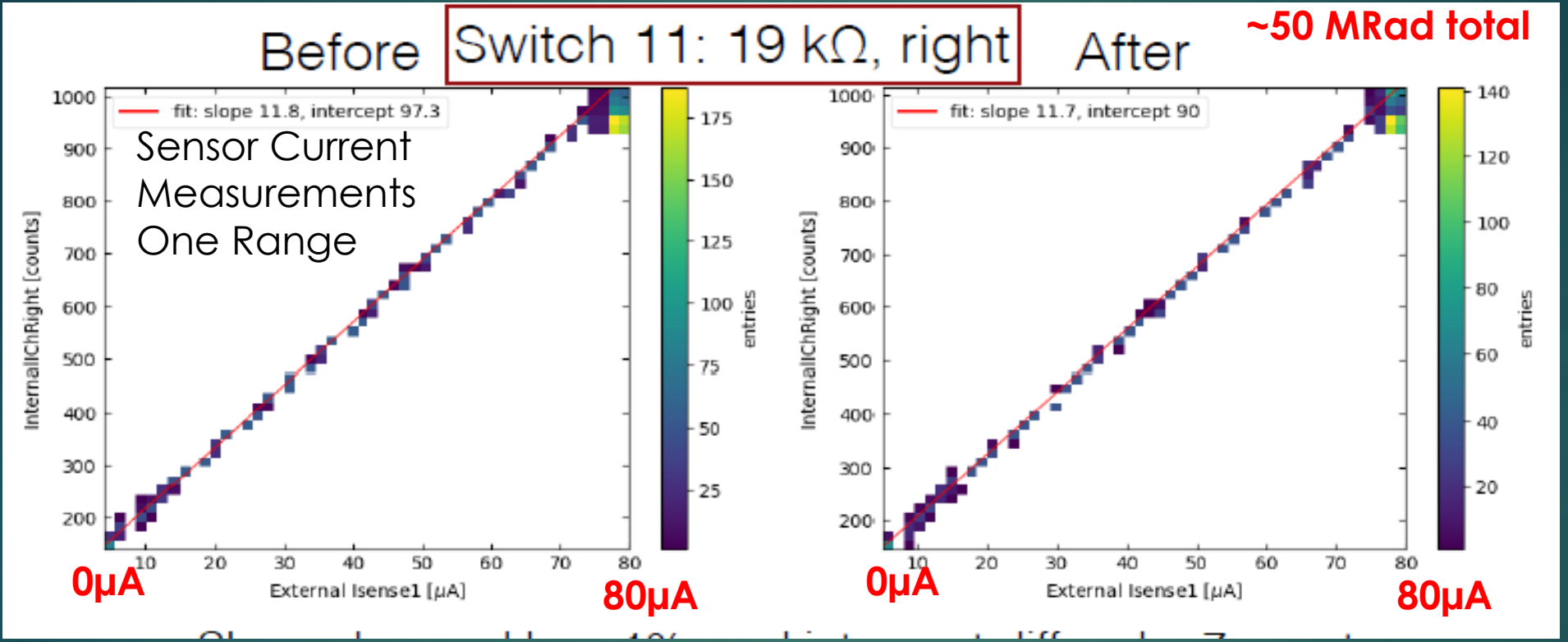
AMAC V1a ASIC exposed to .85 MRad/day for 58 days



Two Channels monitored #0 and #3 Ramped by External source
Before and After Voltage measurements (Slope & Intercept) ~ 0.5%

TID tests @ BNL AMAC V1a

AMAC V1a ASIC exposed to .85 MRad/day for 58 days



Two Channels monitored #0 and #3 Ramped by External current source
Before and After current measurements Slope Changed by 1% Intercept 7 counts

Status

AMAC V2 was due out of FAB in February but the 130 MPW has been held up to accumulate all interested parties for the last run.

We expect AMAC V2 to be shipped on Friday. Our hopes are up.

AMAC V2a will be submitted along with The Star Chip set this week.

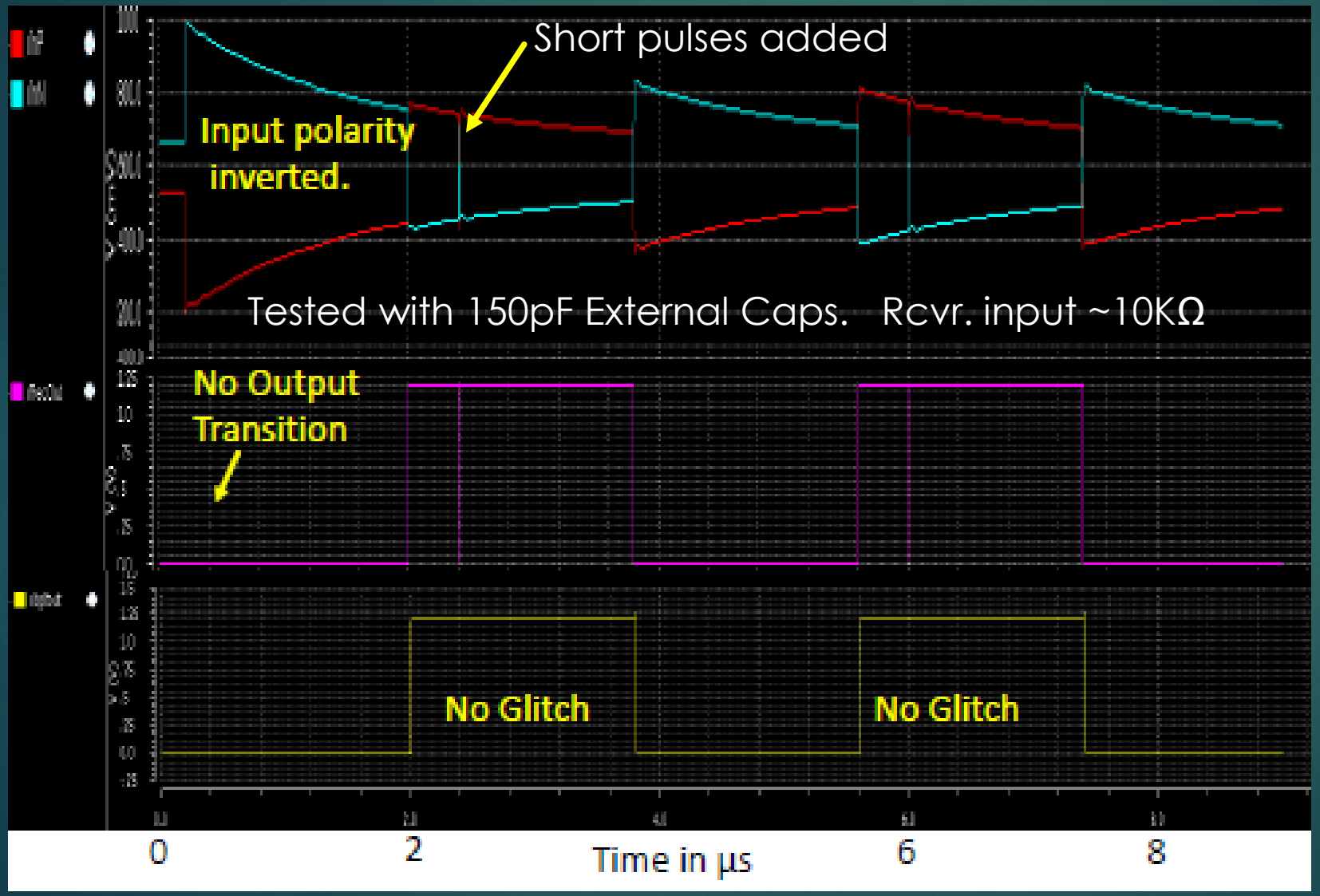
to keep the various Integration prototyping engines running.

We are working with Timon Heim and Karol Kriska @LBL to be ready for tests when AMAC V2 returns from Fab.

AMAC Specification document available on request: Mitch@HEP.UPENN.EDU

Backup

Receiver with Hysteresis for AC coupling & Deglitching for sub 10ns signaling.

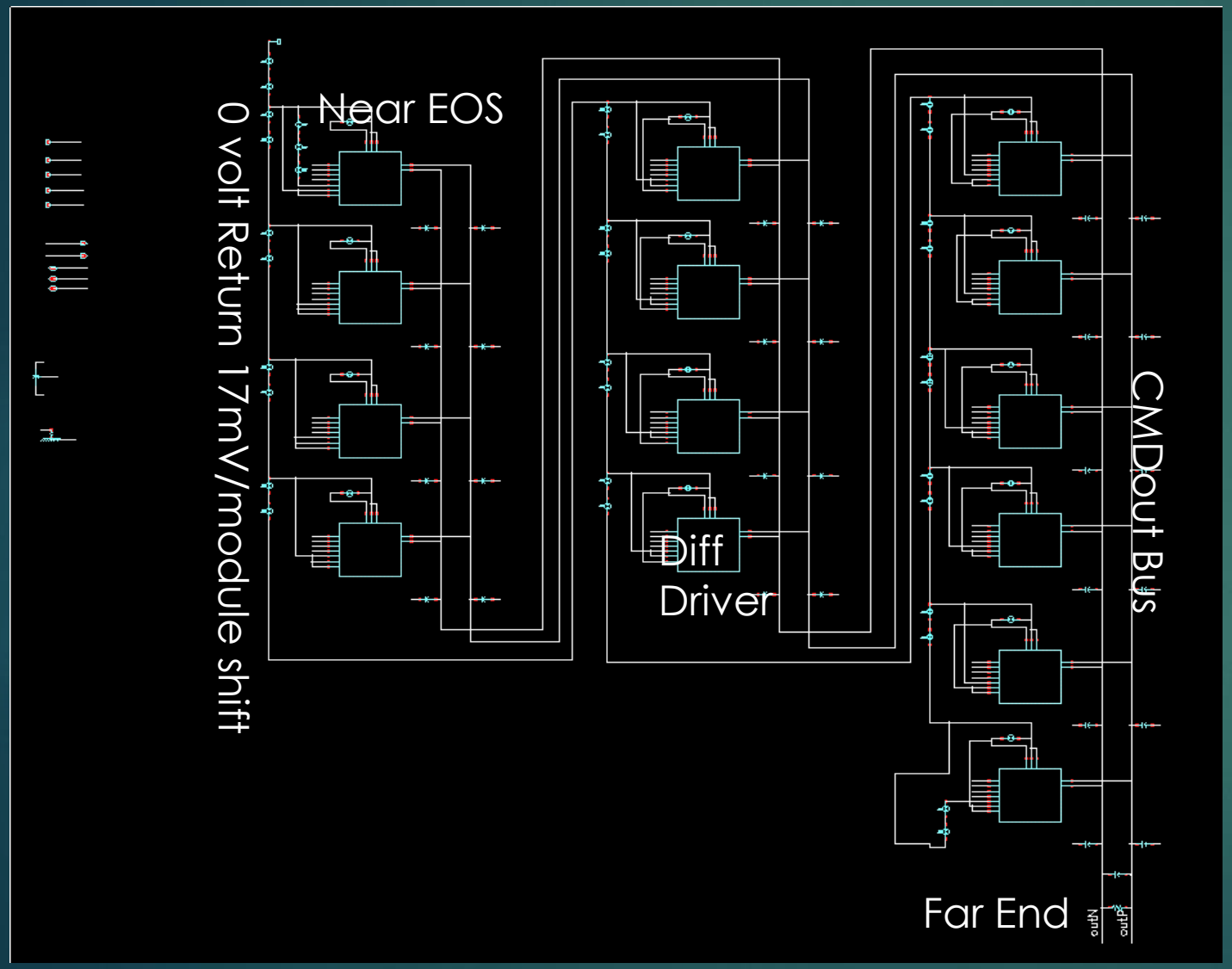


Differential signal on rcvr. side of AC coupling caps First Transition was intentionally Sent with same polarity as Hysteresis and is NOT registered

Receiver Output to deglitcher ckt.

Deglitched Data Received by AMAC

Simulate 14 Tristate Diff. Drivers



- 200mV supply return drop
- Distributed 70pF cap/line

- Each driver enabled separately by remote command

- Common Mode Setting
- First Driver 600mV
- Last driver 400mV
- Prog. Drive Current.

- Endeavor Protocol
- Low speed few MHz
- Long & Short pulse → 1 & 0
- CMD acknowledge

Tri-state Differential Driver Simulations

SLOW transmission 400ns / bit for AMAC Tristate driver