Performance of a digital-SiPM readout chip.

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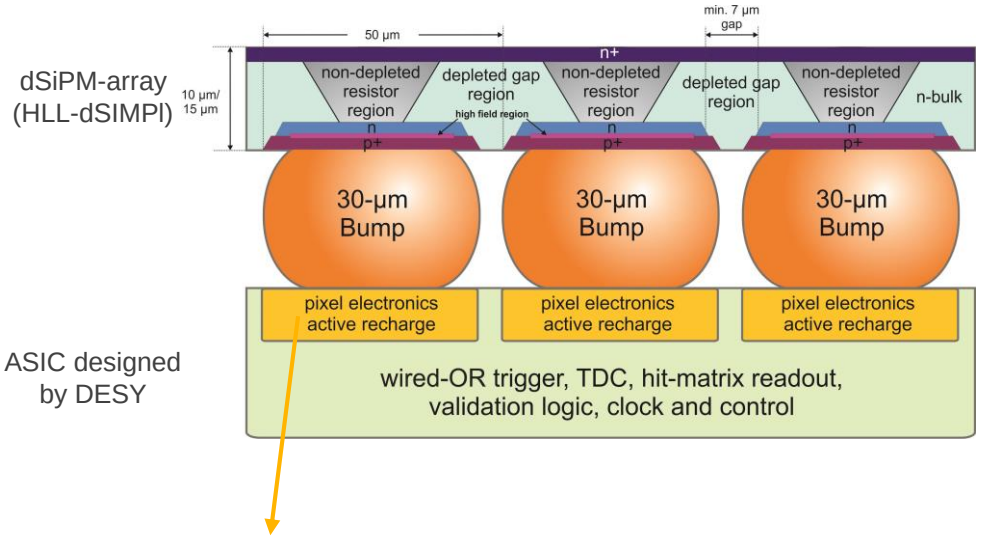
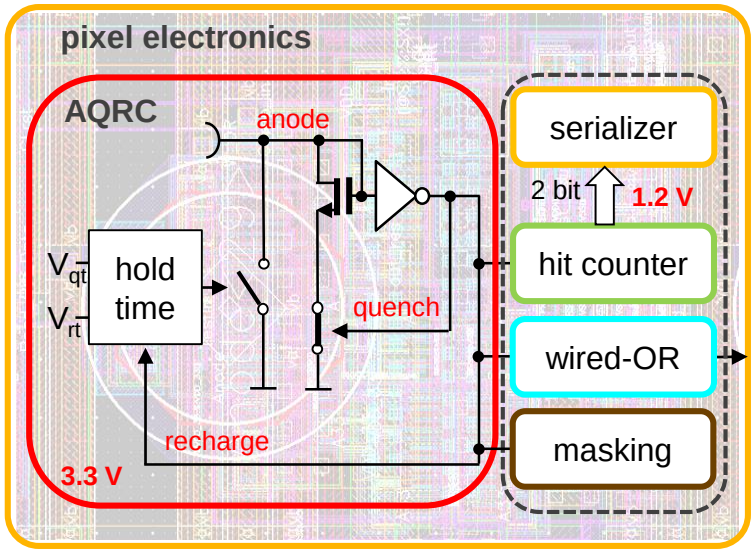
HELMHOLTZ ASSOCIATION

DESY

Readout concept: *hybrid approach*



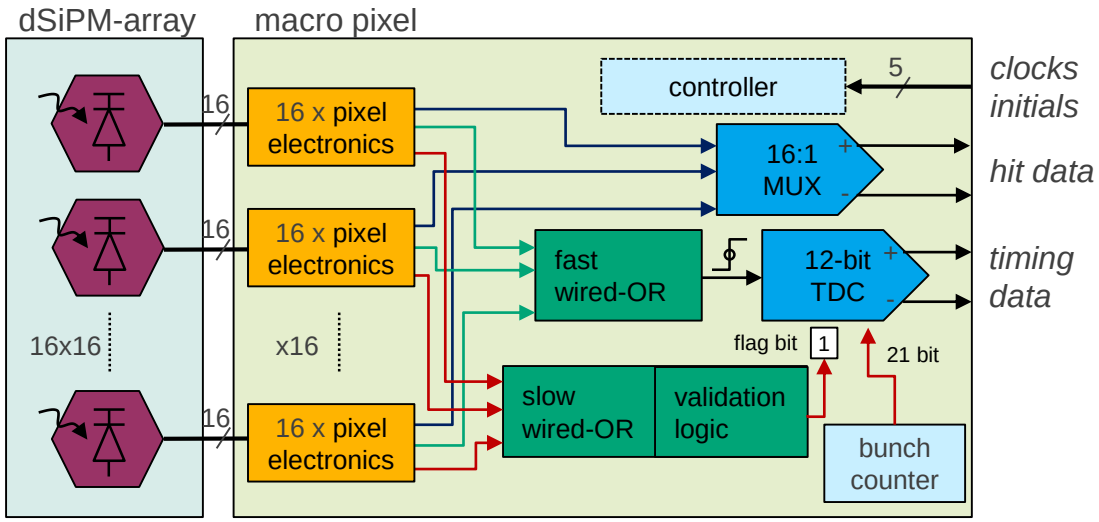


- ultra-thin sensor + fast readout ASIC
- sensor with small bulk resistor – fast recharging
- low over-bias voltage (3.3-V mosfets)
- pixel-wise readout – digital signal (no analog sum)
- high fill factor
- active quenching & recharging circuitry (AQRC)
- adjustable recharge start/hold-time (pile-up rejection)
- masking of noisy pixels
- hit counting
- wired-OR trigger

1st application:

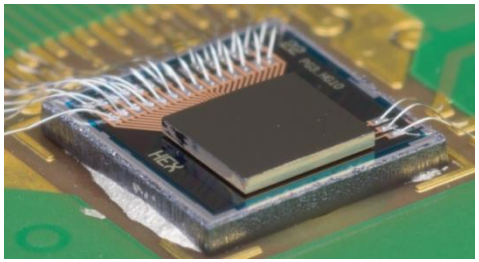
particle tracking

Readout concept: *macro pixel*

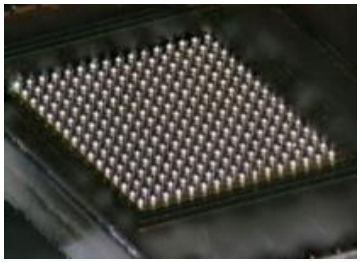


- 16-by-16 pixel unit, 50-µm pitch
- interleaved row-wise 16-to-1 multiplexing
- 12-bit TDC (5-bit fine, 7-bit coarse)
- validation logic with comparators
  - adjustable thresholds
  - row reference: 1 … >4 pixel
  - column reference: 1 … >2 rows
- 21-bit bunch counter
- serialized time stamp / validation flag / frame number
- controller
  - clock division & distribution
  - status control register
- ≤ 3.3-MHz bunch clock scheme
- ≤ 450 MHz fast clock for MUX & TDC
- sustained data throughput @ 3 MHz
  - fast LVDS links
  - 816-Mbps hit data
  - 102-Mbps timing data

prototype

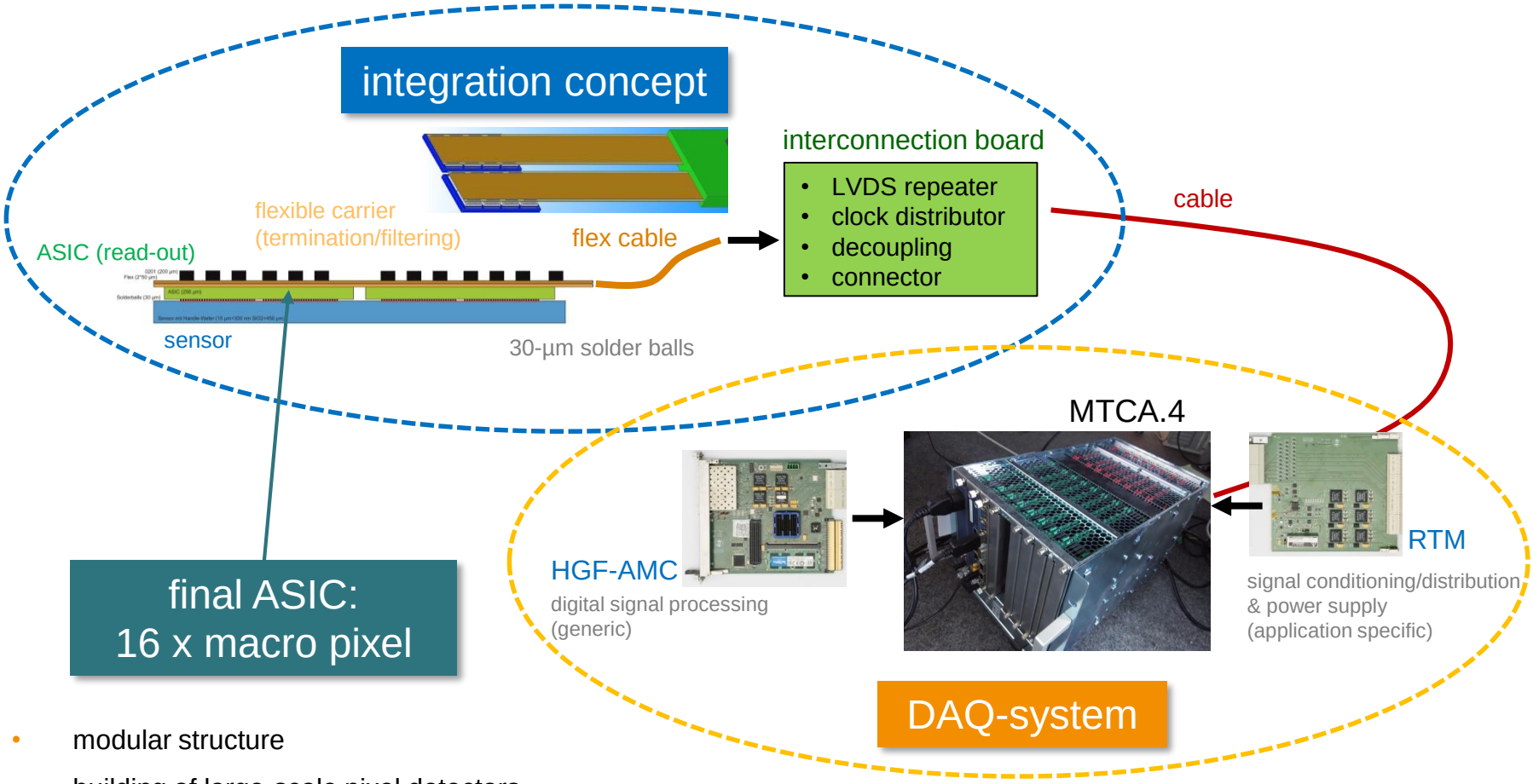


macro pixel
sensor (4x4 mm²) with handle wafer
ASIC (2x2 mm²) on top
130-nm GF 8M1P CMOS



30-µm SAC solder spheres
by using the laser-assisted
jetting technique

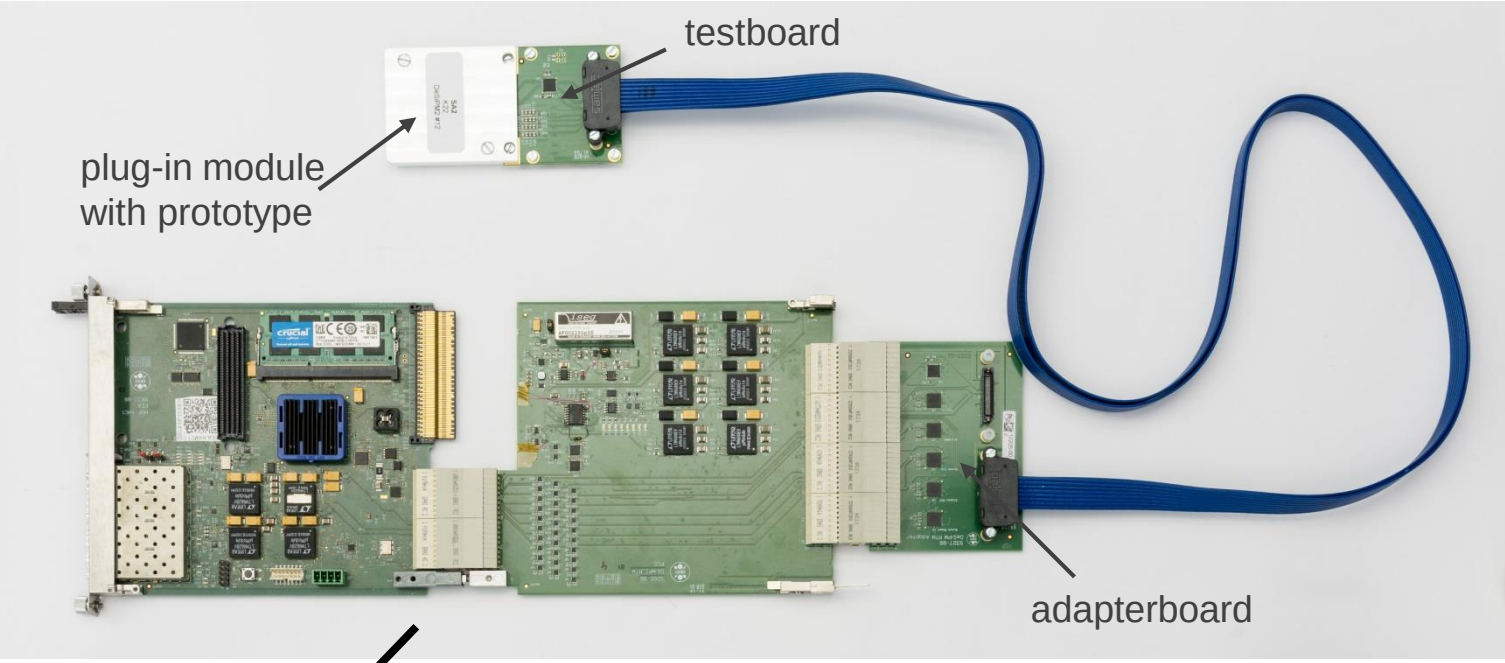
Readout concept: *detector system*



- modular structure
- building of large-scale pixel detectors
- DAQ-system based on MicroTCA.4 standard
- application specific designed RTM
- ~14 Gbps data throughput per ASIC @ 3MHz

1HGF-AMC processes
128 macro pixel

DAQ system: *status*

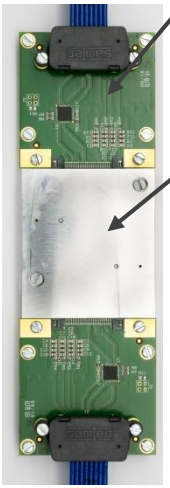


- board design and assembly ready
- FPGA programming in progress
- DAQ system available soon
- testboard with plug-in modules

testboard

plug-in module
with prototype

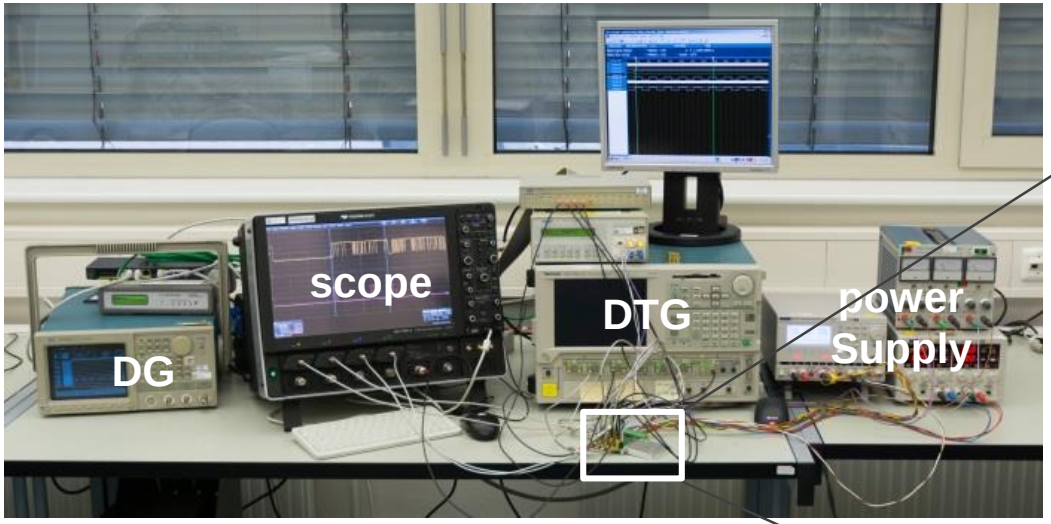
DAQ system: *beamline setup*

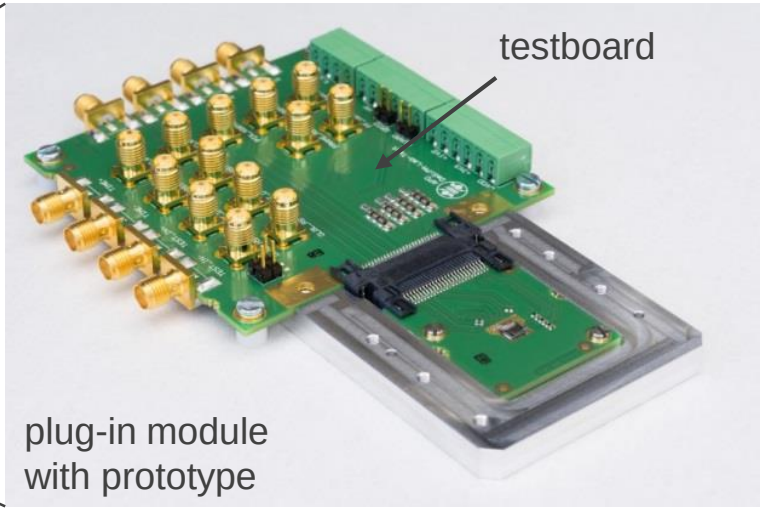


- measurement of charged particles
- 2 prototypes on top of each other
- coincidence measurements
- rejection of dark events

Test setup: *prototype*

test setup at the moment





- lab instruments:
  - pattern generator, oscilloscope, data-timing generator, power supply
- 1 testboard with plug-in modules
- 2 output streams:
  - hit data
  - timing data (valid bit, TDC out, frame number)
- ASIC-behavior test independently of the sensor possible by using a test input
- prototype performance tests only with dark events

ASIC behaves as expected

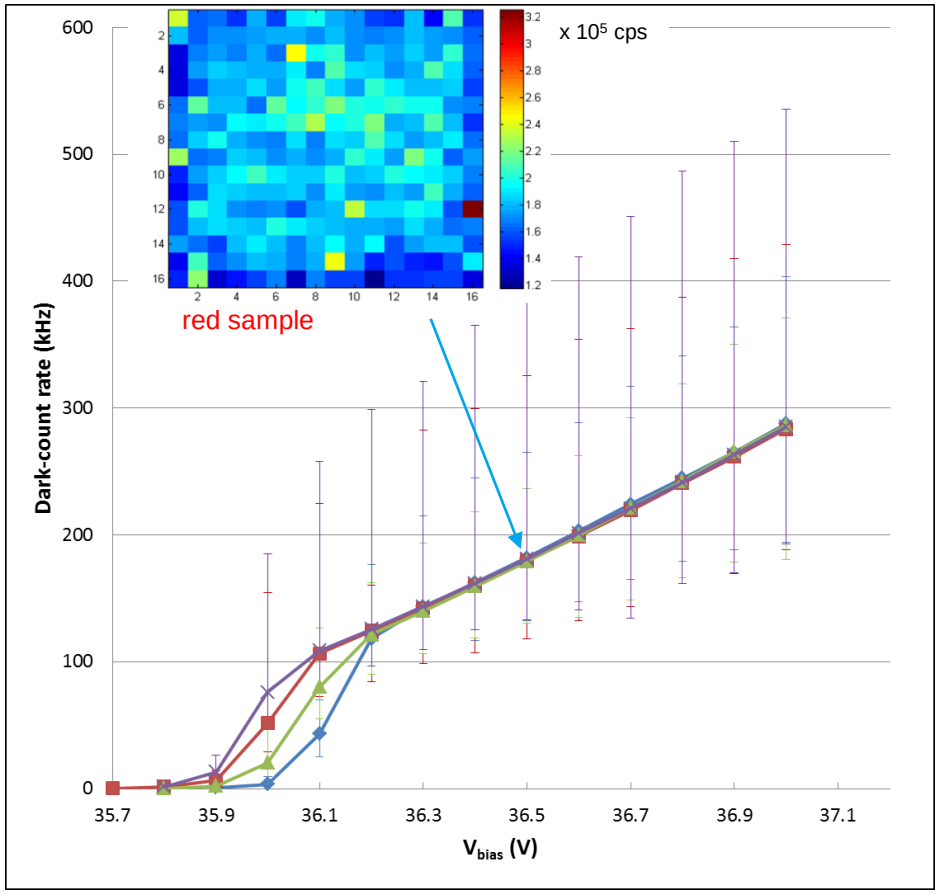
verification of timing characteristics, validation logic, in-pixel hit counting and data processing

Results prototype: *hit data*

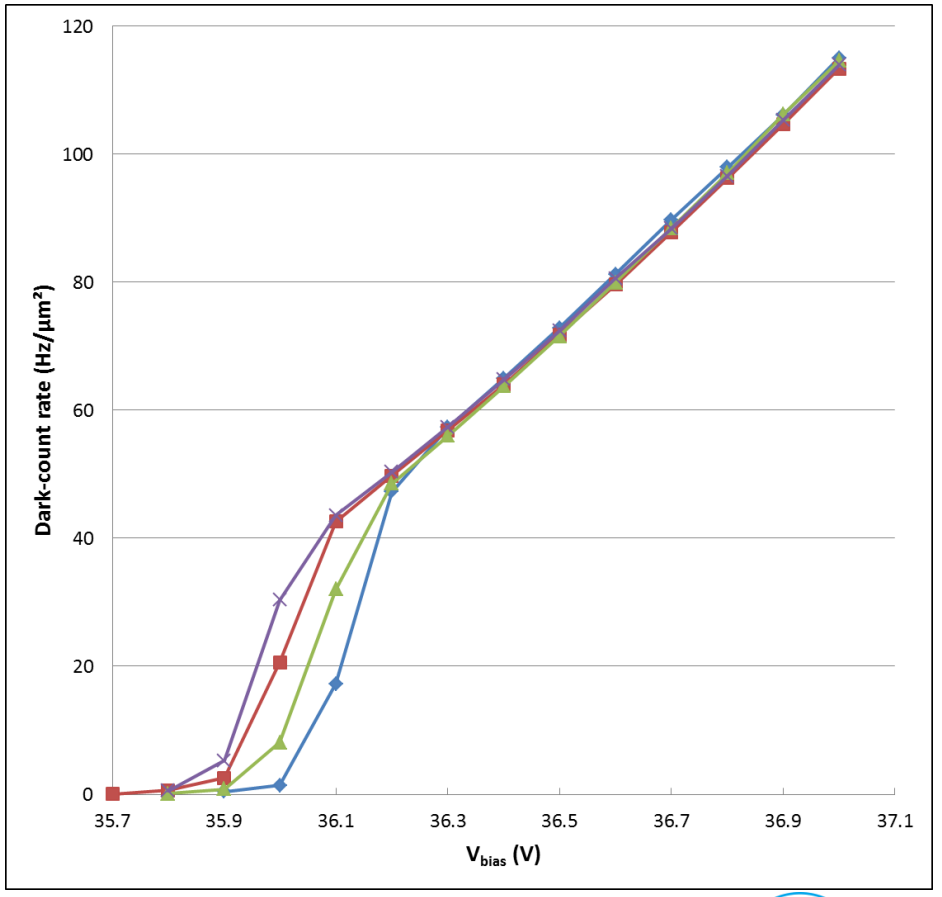
dark-count rate as function of the sensor-bias voltage

- record time: ~12.5 ms
- 1-hit counting per frame (3 MHz-frame rate)

dark-count rate per pixel



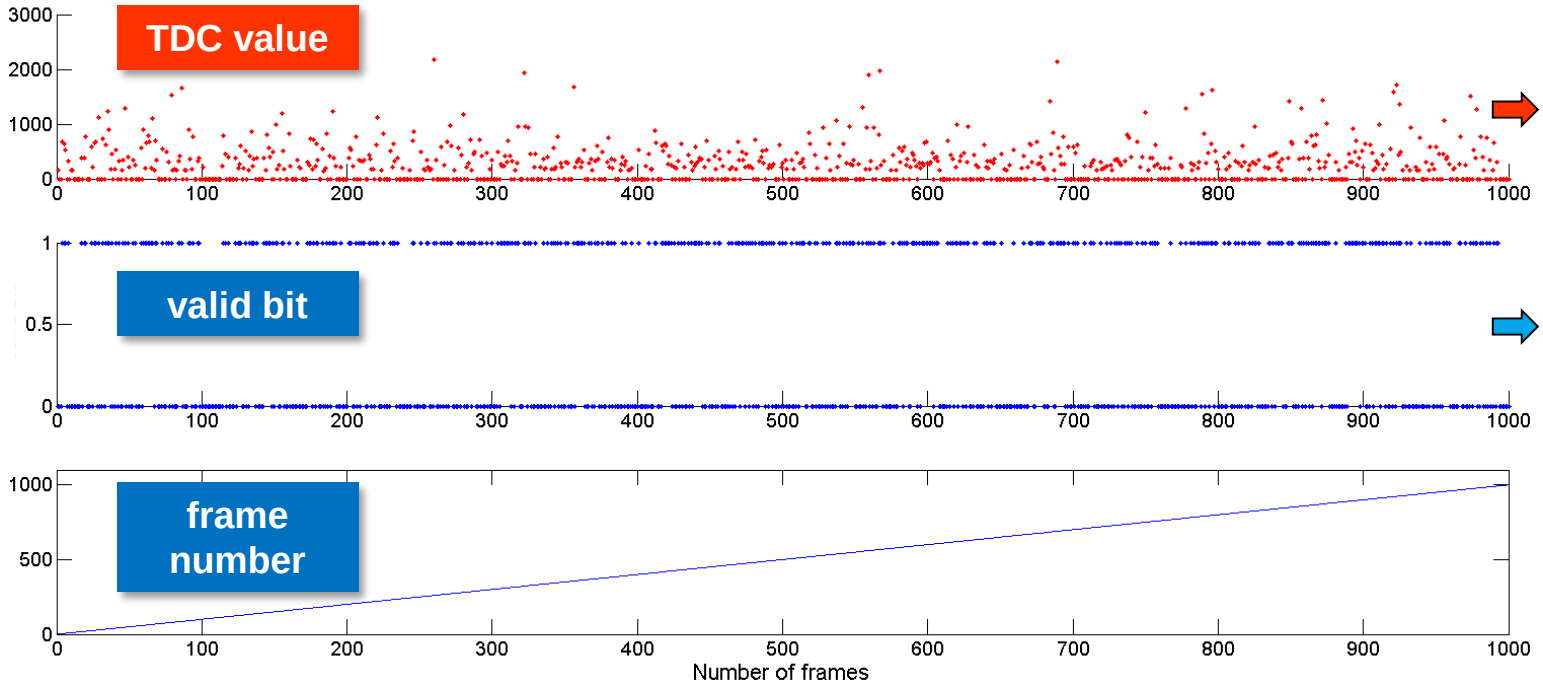
dark-count rate per area



Results prototype: *timing data*

timing data in every frame

- time window: 333 µs = 1000 frames @ 3 MHz
- V_{bias} = 36.5 V



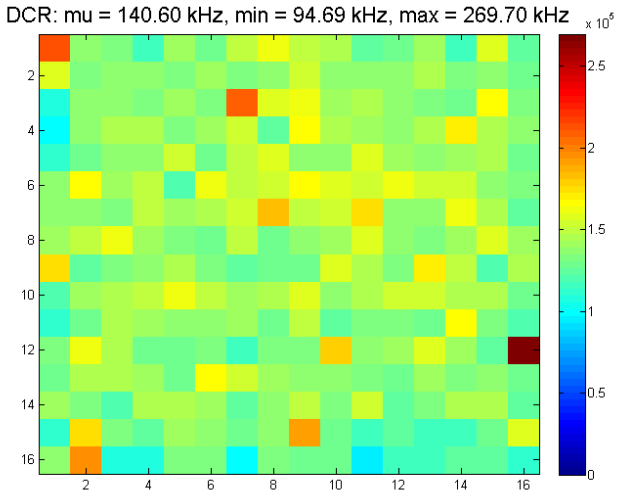
Results prototype: *validation-logic performance*

dark-count rate with consideration of valid bit

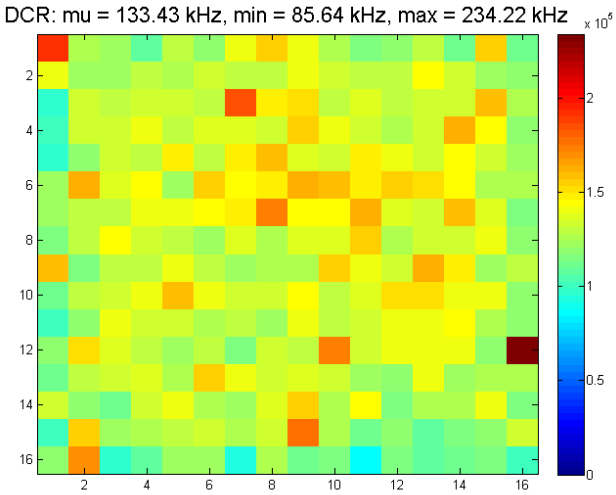
- record time: ~12.5 ms (~38000 frames @ 3 MHz)
- 1-hit counting per frame
- V_{bias} = 36.5 V

validation thresholds:

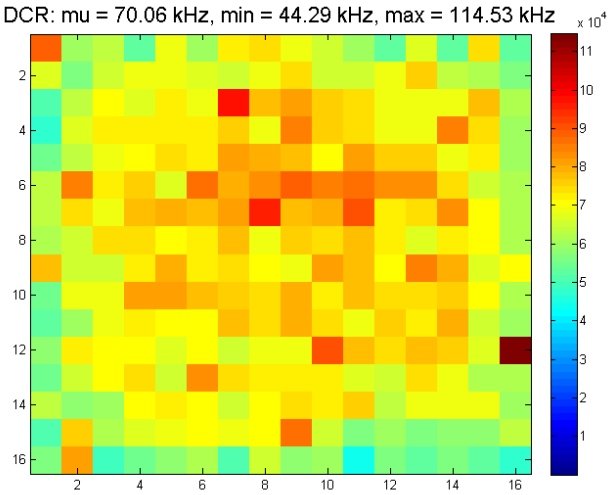
row: 2, col: 1



row: 3, col: 1



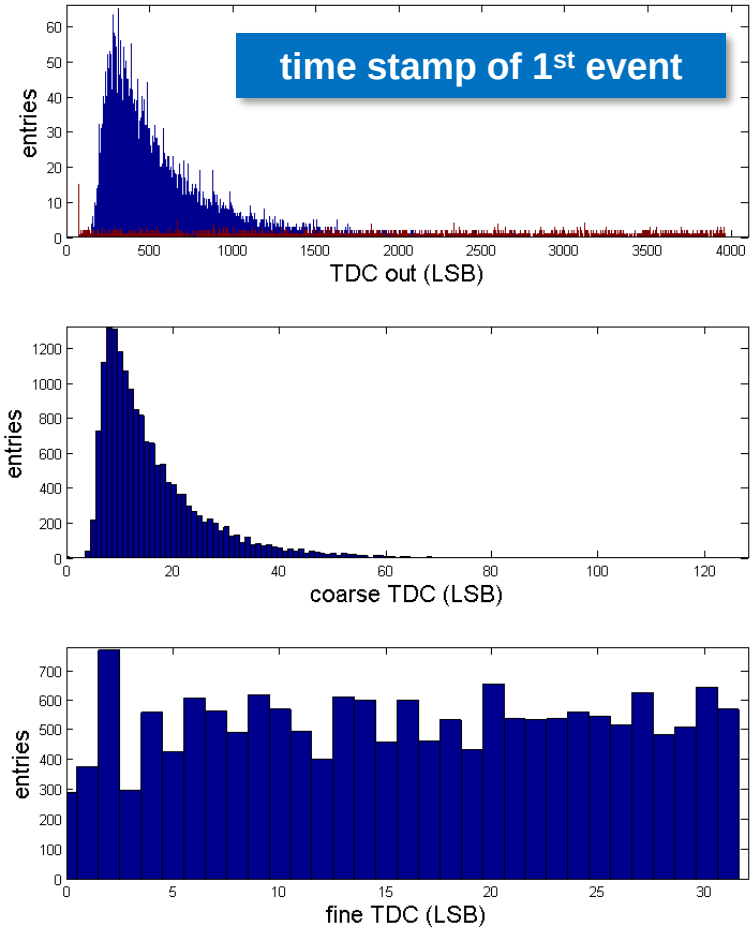
row: 4, col: 1



- DCR can be significantly reduced (compare: DCR w/o validation = 180 kHz)
- crosstalk problematic shown

Results prototype: *TDC performance*

histogram of the TDC values

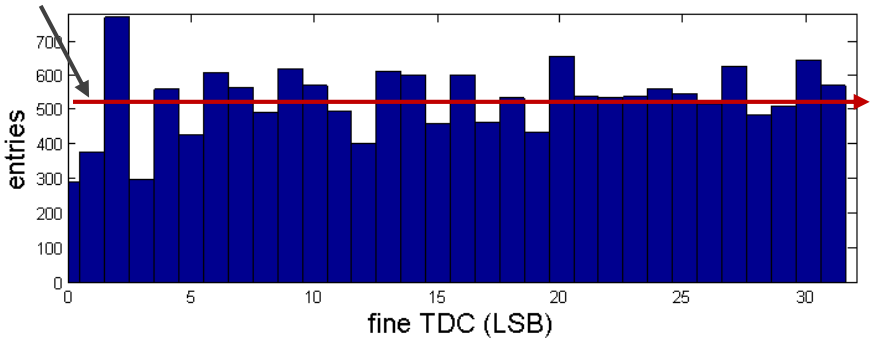


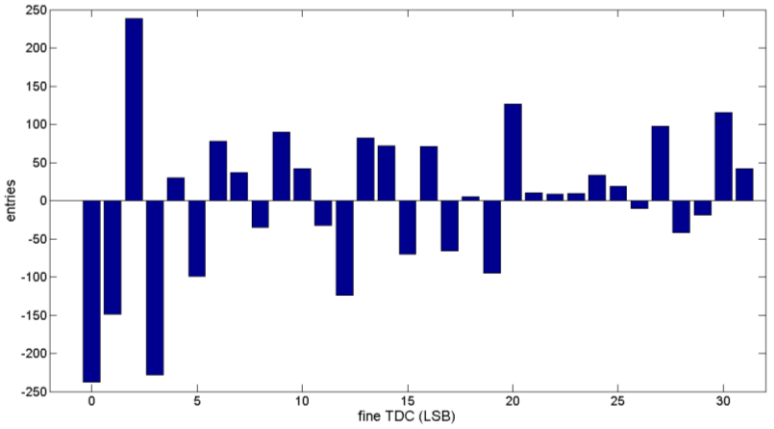
- record time: ~12.5 ms (~38000 frames @ 3 MHz)
- V_{bias} = 36.5 V
- ‘0’ suppression by consideration the valid bit
- mean peak of TDC values at the beginning
  - probability higher by enabling all pixel
  - for 1 pixel enabled it is nearly equal distributed

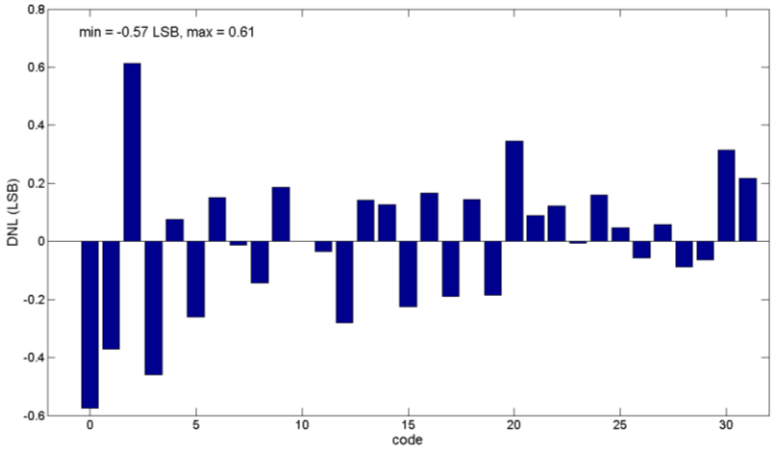
Results prototype: *fine TDC performance*

Distribution of the fine TDC output values for random dark events

Mean value



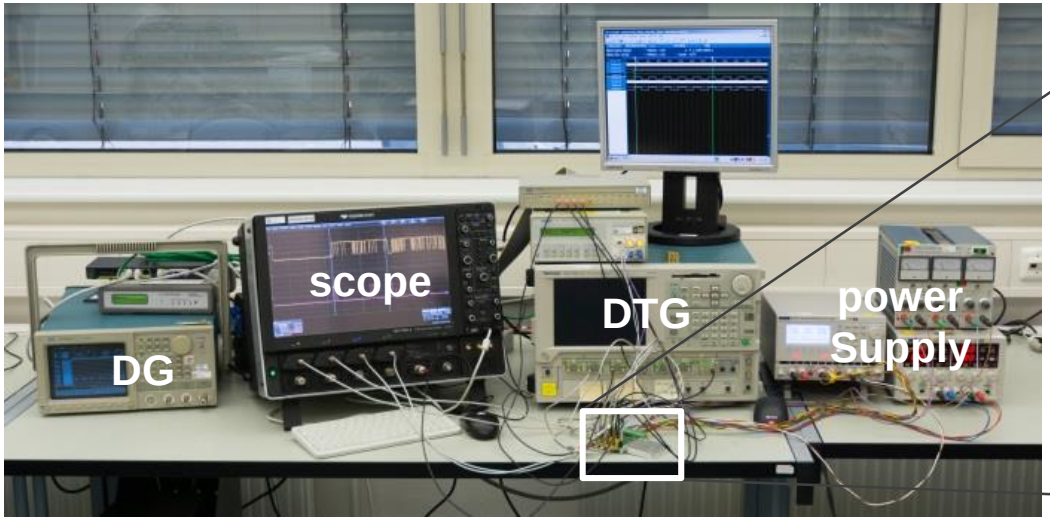




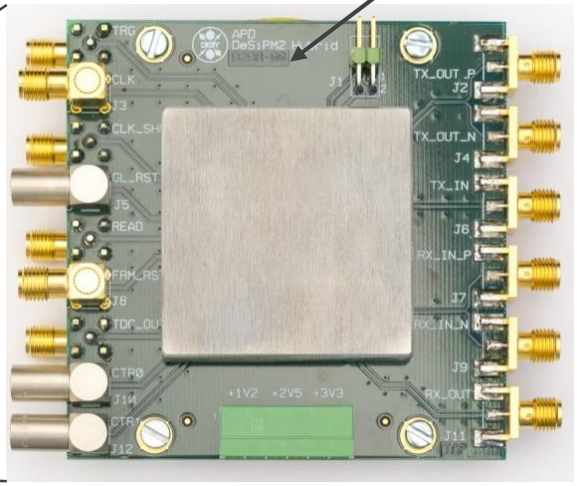
- in good agreement with the fine-TDC DNL
  - determined by using the test input
  - max. DNL error: +0.61/-0.57 LSB

Test setup: *ASIC - separate test circuits*

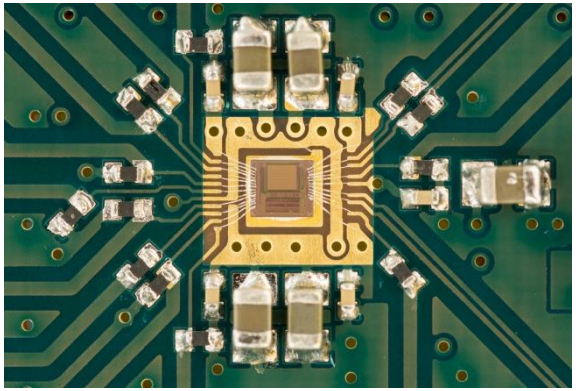
additional performance tests



TC testboard



- lab instruments: pattern generator, oscilloscope, data-timing generator, power supply
- 1 testboard with 1 ASIC sample
- test of separate circuits:
  - 1 TDC
  - 1 LVDS transceiver



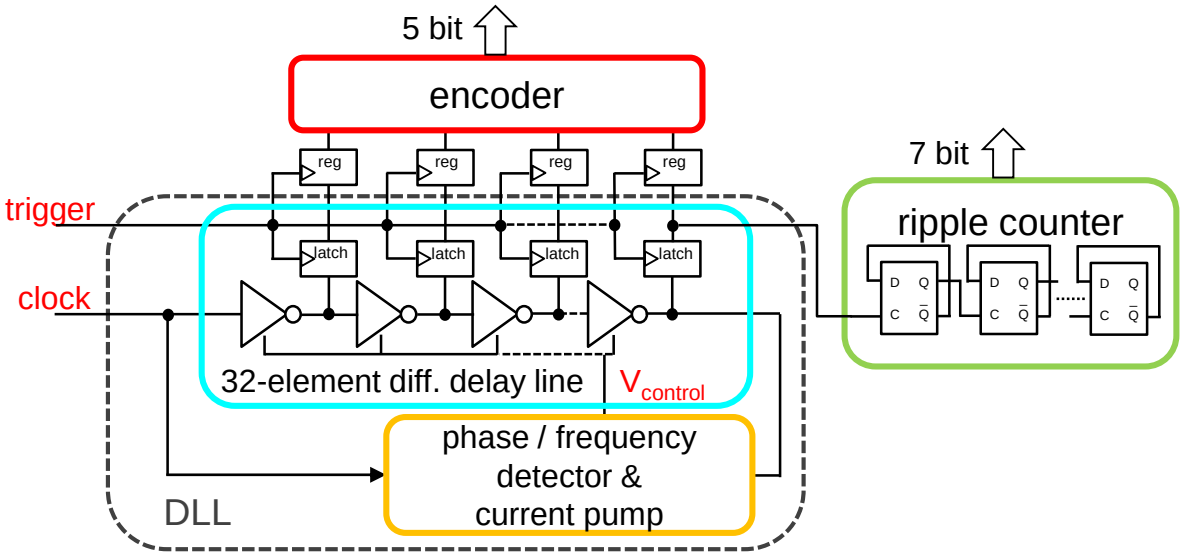
Results test circuits: *time-to-digital converter*

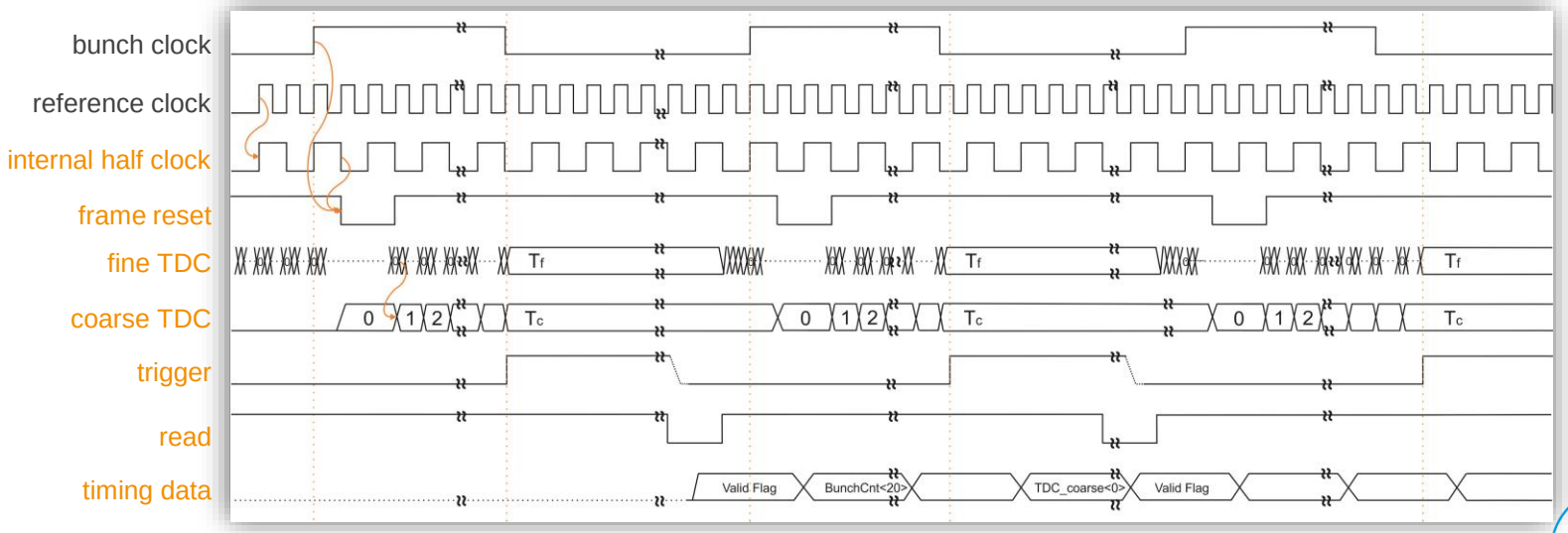
requirements

- 3-MHz bunch clock
  → 408-MHz reference clock
- timing resolution <90 ps

working principle

- delay lock loop (fine TDC)
  - 32 delay elements
  - ~77-ps timing resolution
  - 32-to-5 bit encoder
- ripple counter (coarse TDC)
  → *time stamp: 1st hit*



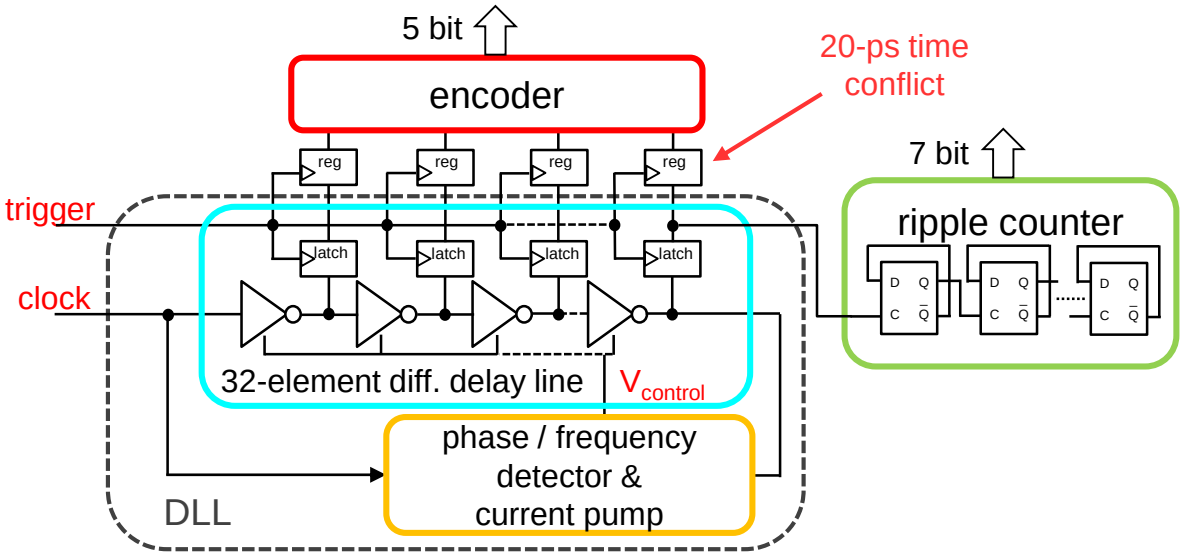


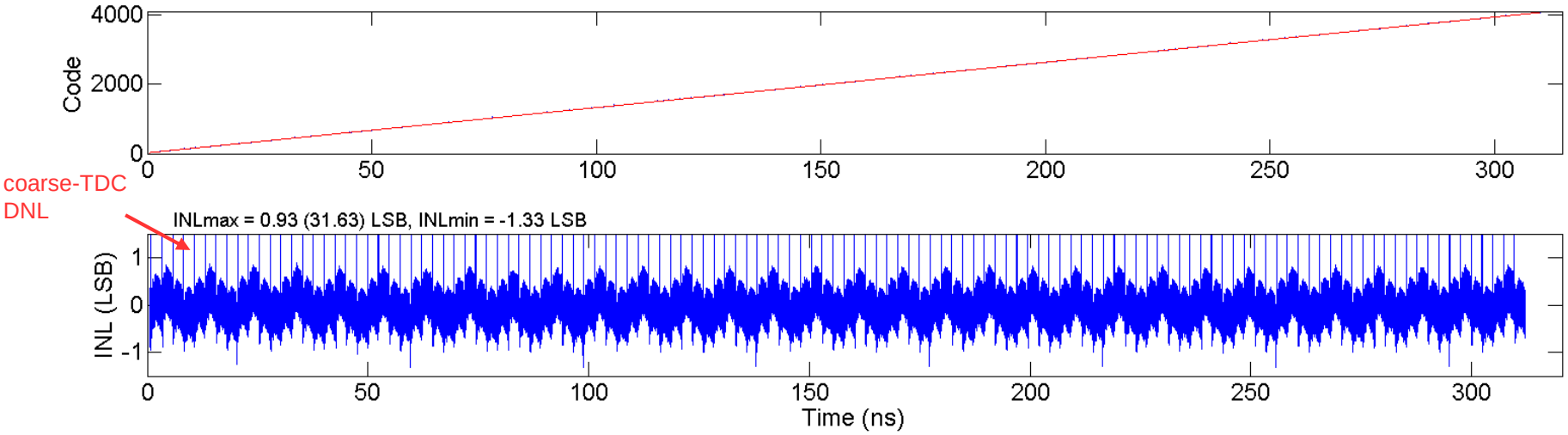
Results test circuits: *time-to-digital converter*

linearity measurement

- determination of INL, DNL and bin width
- small bug, caused by registers setup/hold-time

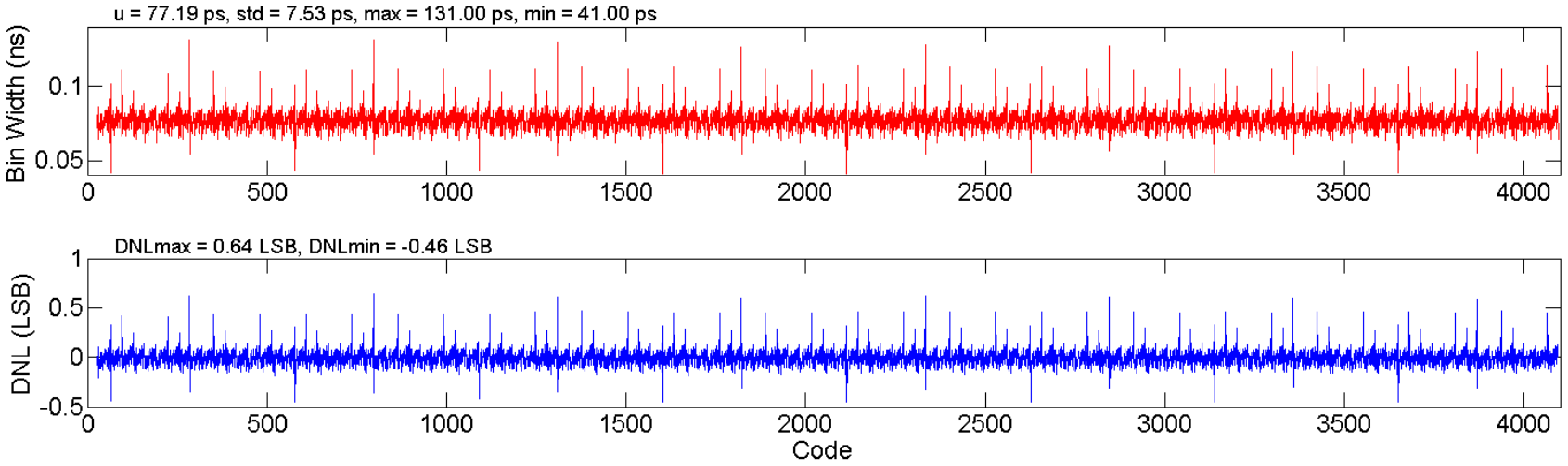
  → can be improved by small design change

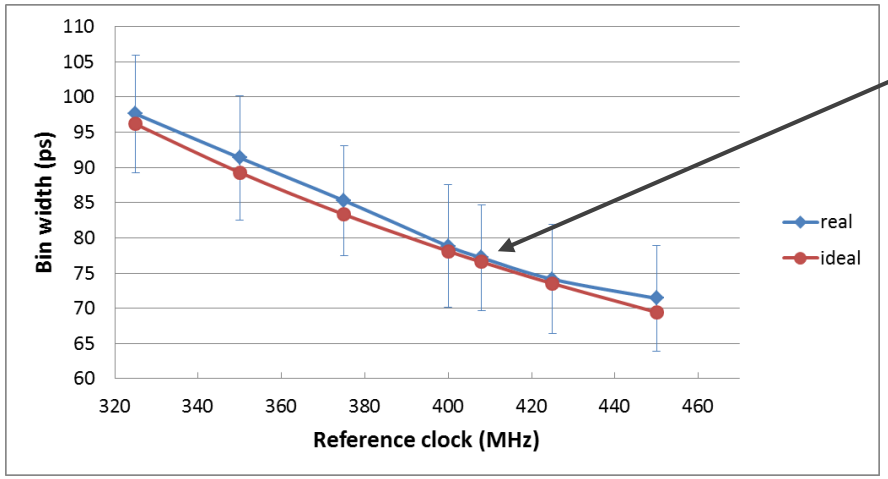




Results test circuits: *time-to-digital converter*

408-MHz reference clock



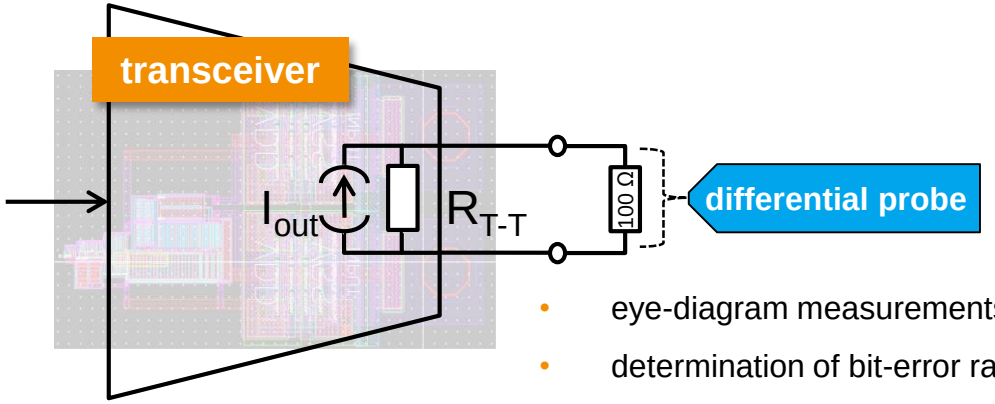


- TDC is designed for target frequency 408 MHz
- mean bin width is in good agreement with ideal value
- upper limit ≤450 MHz

Results test circuits: *LVDS transceiver*

working principle

- voltage conversion
- phase splitting
- current switching with CMFB
- termination R_T = 100 Ω on TX and RX
- V_{cm} = 1.2 V

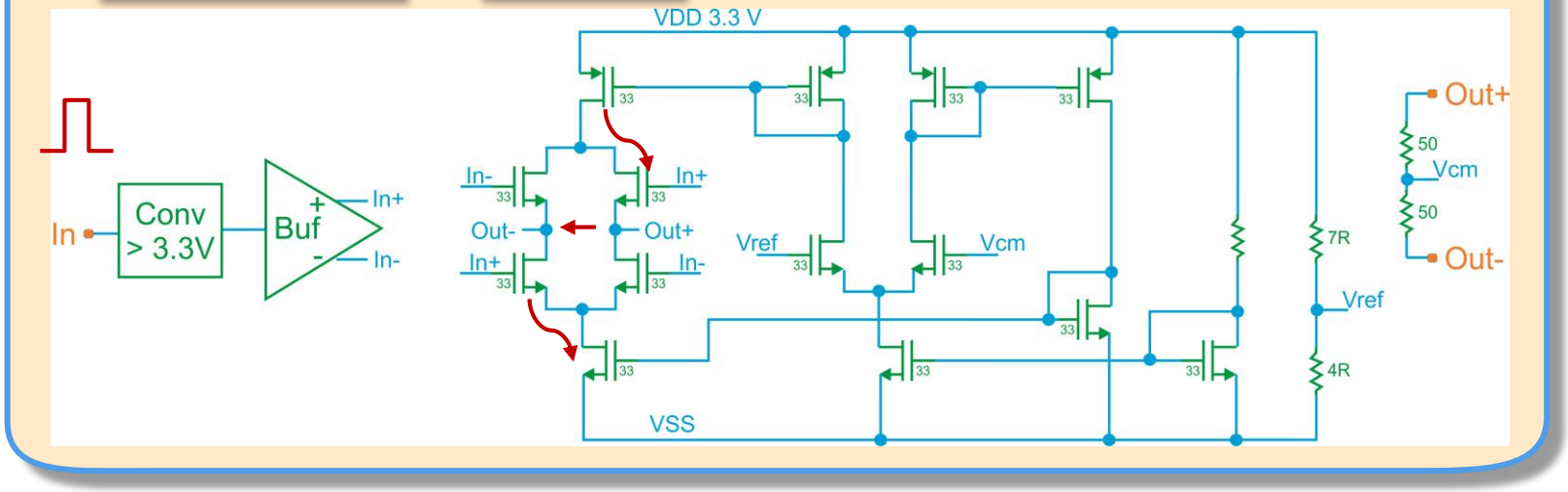


- eye-diagram measurements
- determination of bit-error rate (BER)

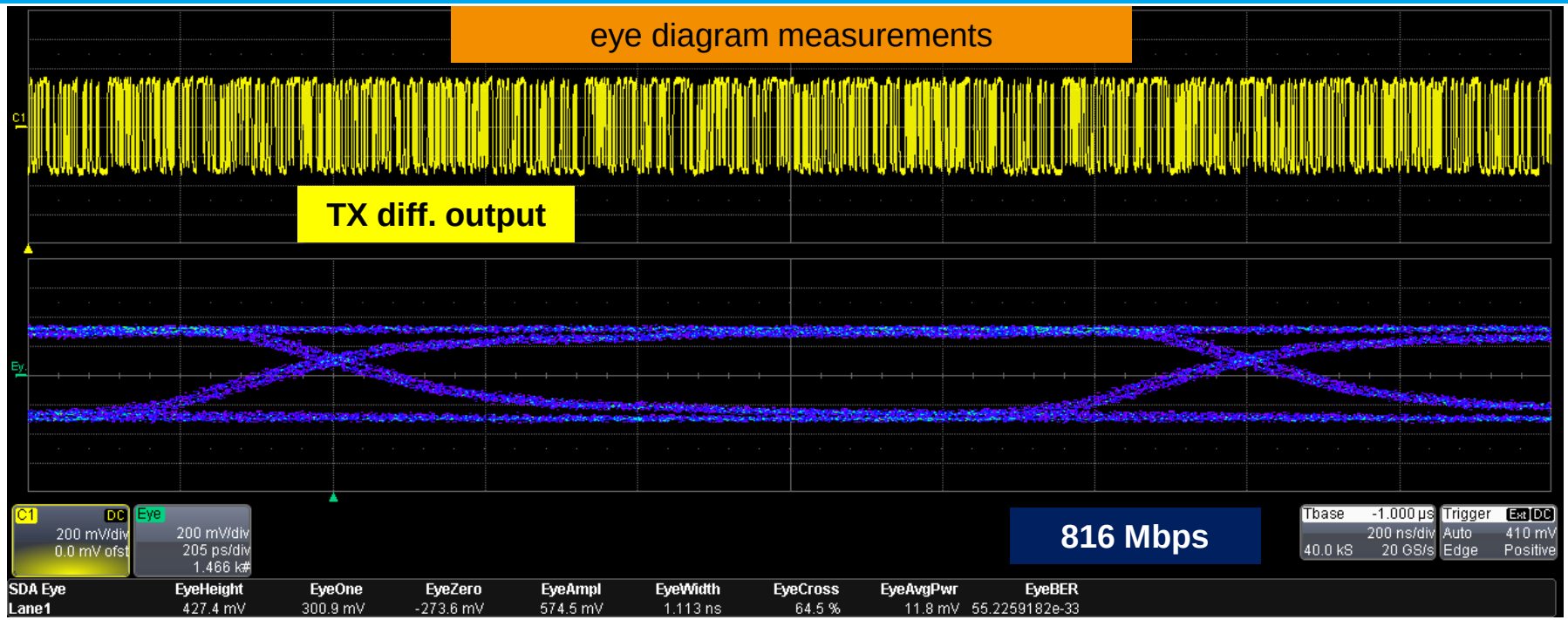
V-conversion phase splitting

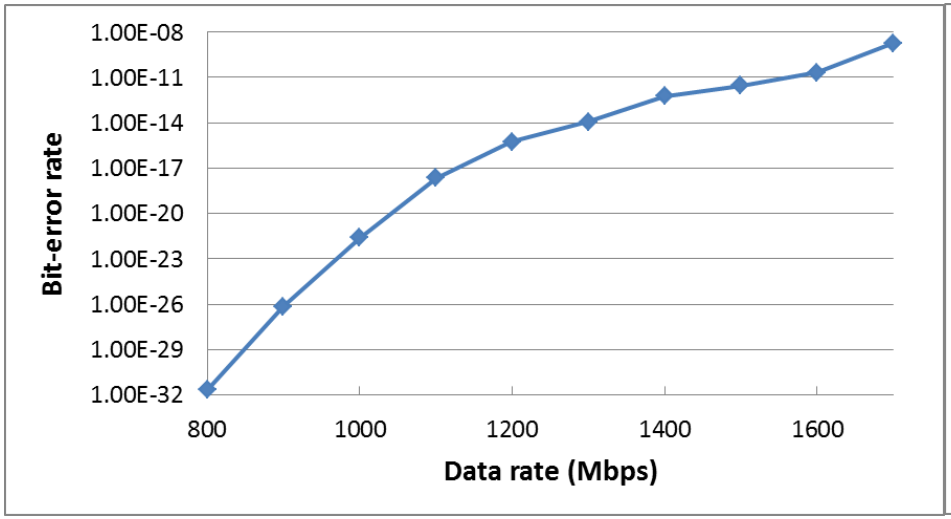
current switching

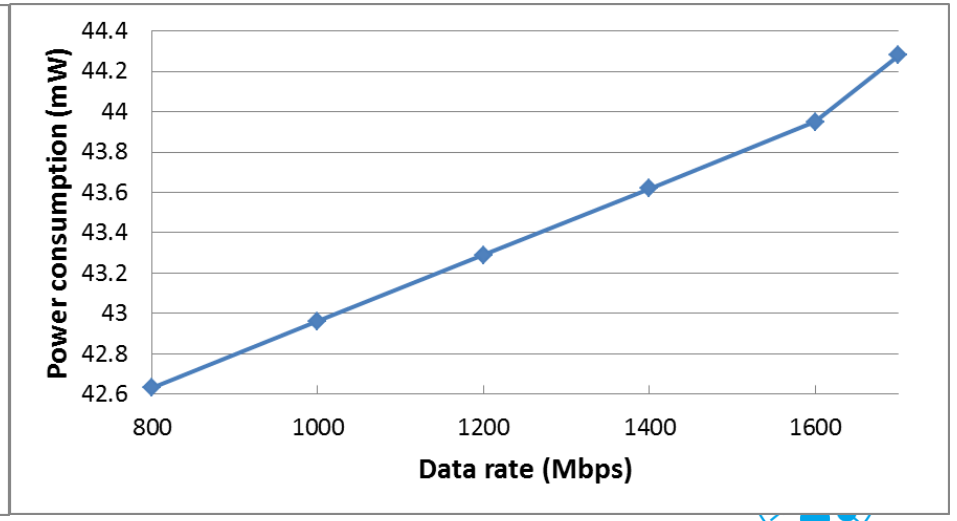
CMFB



Results test circuits: *LVDS transceiver*







Summary

- readout concept and detector system presented
- successfully prototype assembly with 30-µm solder spheres at 50-µm pitch
- functionality of sensor-ASIC prototype tested
  - dark-count rate evaluated versus bias voltage
  - hit detection and time stamping of first hit in macro pixel demonstrated at 3-MHz frame rate
  - basic performance of validation logic using random dark events
  - good agreement of fine-TDC DNL determined by dark image histogram and test input
- 12-bit TDC fulfills the targeted linearity requirements up to 3.3-MHz frame rate
- bit-error rate remains below 10^{-9} up to 1.6 Gbps: link reduction by a factor of 2 is possible
- next steps:
  - test with DAQ system
  - test with particles
- outlook:
  - improve TDC
  - sensor with improved dark-count rate
  - design transfer into new technology necessary

Thank you!