ATLAS Level-0 Endcap Muon Trigger for HL-LHC

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Abstract

High Luminosity LHC (HL-LHC) is an upgrade of LHC to achieve higher luminosities, thereby enabling experiments to reach better physics sensitivity.
Operation of HL-LHC is scheduled to start in 2026 with an instantaneous luminosity of 7.5 x 10^{34} cm^{-2} s^{-1} .
In order to cope with the luminosity at HL-LHC, the trigger and readout systems need to be upgraded.
The design for the Level-0 endcap muon trigger of the ATLAS experiment at HL-LHC and the status of the development are presented.

Level-0 endcap muon trigger for HL-LHC

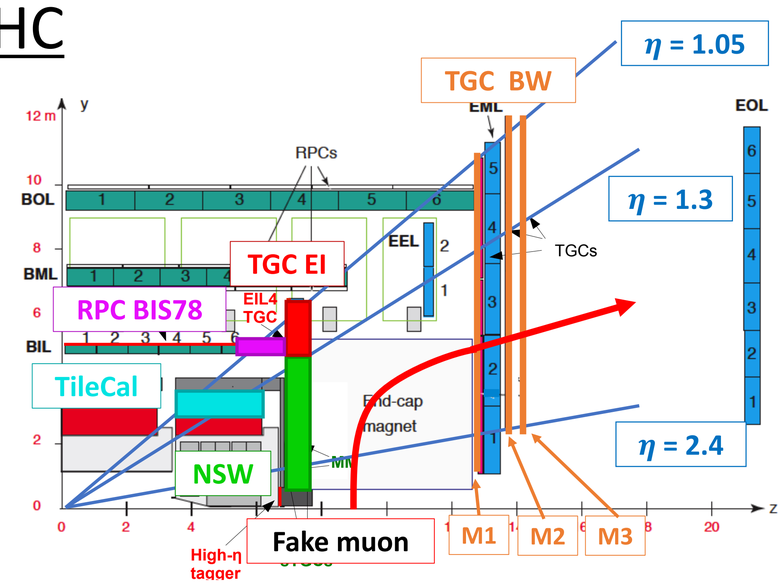
In the original scheme for the first level of the muon trigger, muon track candidates are identified by simple coincidence logic in on-detector boards and the transverse momentum (p_T) is evaluated by look-up tables in off-detector trigger logic boards.

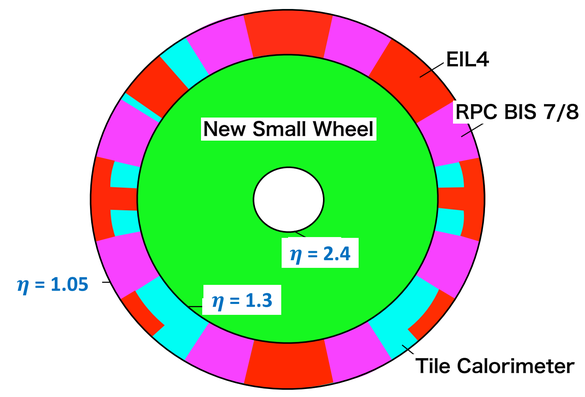
In the new Level-0 endcap muon trigger for HL-LHC, all hit information is transferred from the on-detector boards to off-detector boards. Track segments are reconstructed in the Thin Gap Chamber on the Big Wheel (TGC BW) due to the availability of the individual hits. TGC is a multi-wire proportional chamber which measures two-dimensional position using signals from wires and strips orthogonal to the wires. TGC BW consists of three stations. Station M1, M2 and M3 have three, two and two layers respectively.

The main source of background in the muon endcap system is low-momentum charged particles emerging from the endcap toroid magnets (fake muons). Triggers by the fake muons are suppressed by combining the signals from various subdetectors, TGC in the Endcap Inner station (TGC EI), Resistive Plate Chambers in the barrel inner station (RPC BIS78), New Small Wheel (NSW), and Tile hadronic calorimeter (TileCal).

After muon track candidates are provided by TGC BW and various subdetectors, the Monitored Drift Tube (MDT) is used to improve the p_T resolution at the Level-0 muon trigger.

The trigger logic is provided for each sector defined by the boundaries of combinations of RPC and TGC chambers, implemented in Sector Logic (SL). SL communicates with electronics of various detectors. Main functions of SL is implemented on one FPGA. The Virtex UltraScale(+) FPGAs provided by Xilinx are assumed for the FPGA on SL.

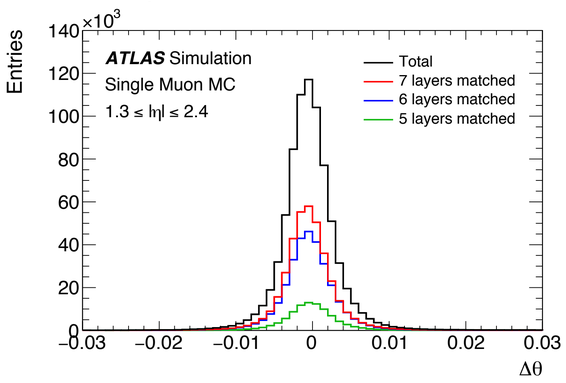




TGC track segment reconstruction

Track segments are reconstructed in TGC with a pattern matching algorithm that compares the TGC hits with predefined hit lists for high-p_T muons. Each predefined hit pattern has angle and position associated to a track segment.

Run-2 trigger requires at least two (one) hits in the inner three (two) layers and at least three hits in the outer four layers for wires (strips).
In the Endcap Sector Logic for HL-LHC, a looser coincidence with at least five (four) hits in seven (six) layers for wires (strips) is required to improve the efficiency.

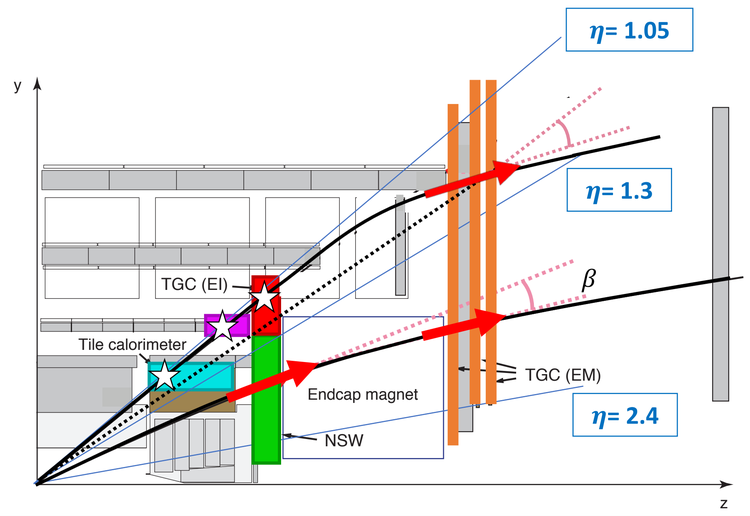


Distributions of the difference of the polar angle (Δθ) between the TGC track segment and the track segment reconstructed by the ATLAS full offline analysis.
Track segments are reconstructed with an average angular resolution of **4 mrad**.

Trigger scheme using inner detectors

★ 1.05 < |η| < 1.3 :
p_T is determined from a combination of the position and the angle of the TGC BW track segments and the positions of the hits in the TGC EI, RPC BIS78 and TileCal.

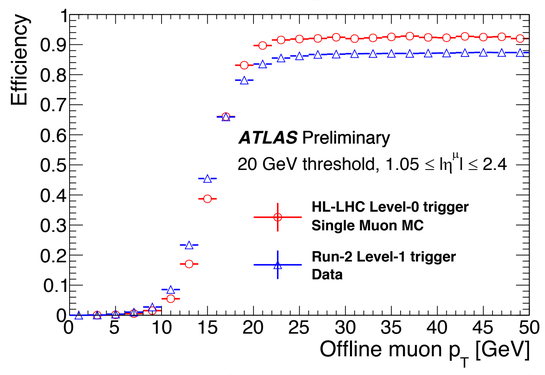
★ 1.3 < |η| < 2.4 :
p_T is determined from the polar angle difference (β) between the TGC BW track segments and the tracks reconstructed in NSW.



Improvement of trigger performance

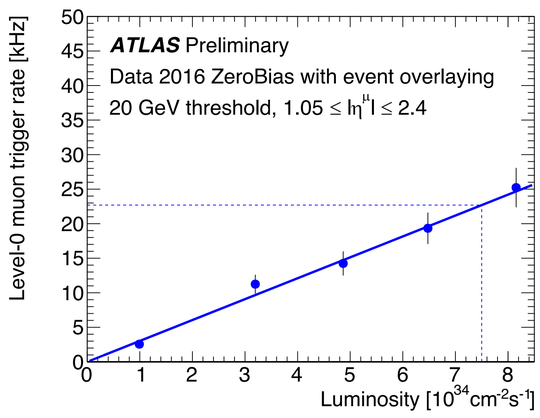
Trigger performance of the Level-0 endcap muon trigger (not including the more precise p_T measurement in MDT) was evaluated.

Expected efficiency to offline muons of the new trigger algorithm was obtained from a single muon MC simulation sample.



Compared to the Run-2 trigger
- **higher efficiency** in the plateau region due to the looser coincidence
- **better rejection** for low p_T muons thanks to the good angular resolution

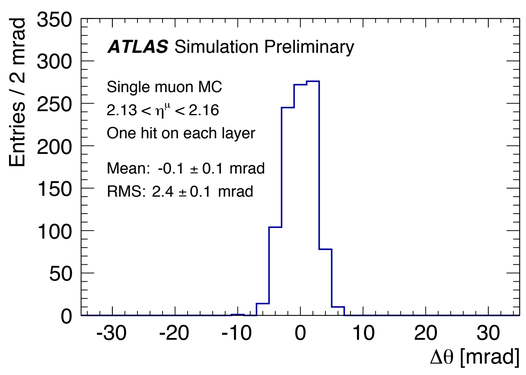
Expected trigger rate was obtained from a Run-2 data taken with random trigger and overlaid to account for higher luminosity points.



- The obtained value for 20 GeV threshold is about **30 kHz.** If this new trigger logic could be adopted in Run2 (~1 x 10^{34} cm^{-2} s^{-1}), trigger rate would be reduced to ~3 kHz (compared to the actual trigger rate of 6 kHz)
- Further rate reduction by ~50% in the next step with MDT is expected

Initial test of TGC segment reconstruction

A test firmware of TGC pattern matching algorithm is implemented in an FPGA to estimate performance.



Test result with the evaluation kit VCU118.
Test vectors of TGC hits is obtained from Monte-Carlo (MC) sample and used as the FPGA inputs.
The angular resolution estimated from the offline analysis is reproduced in the test.

Expected memory usage for the full η range is about 100 Mbit, which is one-third of RAM resources on XCVU9P.

References :
[1] The ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ system, CERN-LHCC-2017-020.
[2] The ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer, CERN-LHCC-2017-017.
[3] https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicReults