The Phase-II Upgrade of the ATLAS Monitored Drift Tube Detector and Frontend Electronics

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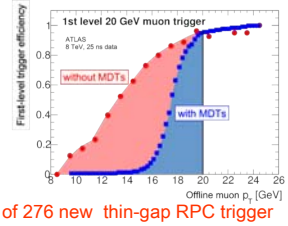
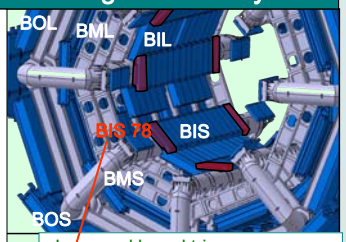
Goals of the Muon Detector Upgrade for High-Luminosity LHC

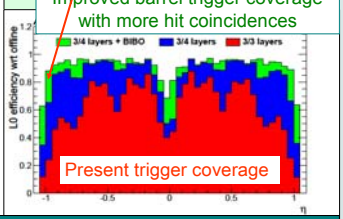
1 Increase of the 1st level muon trigger selectivity and p_T resolution by factor 10 by implementing a fast track trigger based on the Monitored Drift Tube (MDT) precision tracking chambers.
Requires replacement of the MDT frontend electronics.



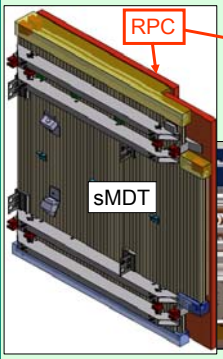
2 Installation of 276 new thin-gap RPC trigger chambers with longer lifetime at HL-LHC in the barrel inner layer BI, combined with 96 new small-diameter muon drift tube (sMDT) chambers in the small azimuthal (BIS) sectors.
16 BIS 78 chambers already for LHC Run 3.

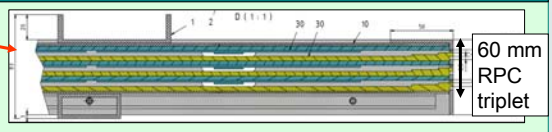


Improved barrel trigger coverage with more hit coincidences

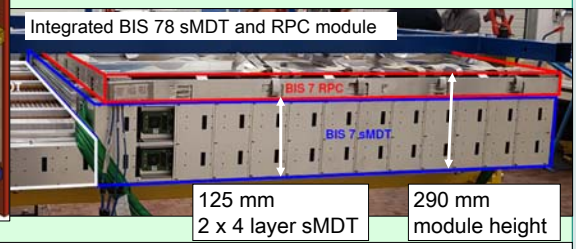


Integrated Thin-Gap RPC and sMDT Chambers



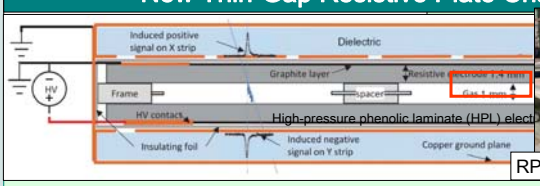


Integrated BIS 78 sMDT and RPC module



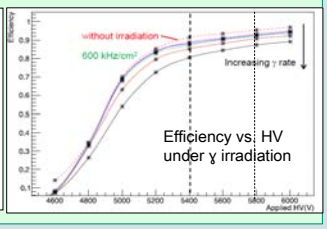
Installation of new triplet RPC chambers in the BIS layer requires replacement of the existing MDT chambers by sMDT chambers to provide sufficient radial space.
Independent interleaved supports on common rail system.

New Thin-Gap Resistive Plate Chambers



RPC triplet assembly & test

Reduction of gap thickness from 2 mm to 1 mm and new highly sensitive preamplifiers
allow for operation at 5.8 kV instead of 9.6 kV
and 15 times lower gas gain.
⇒ increased rate capability of > 10 kHz/cm² and lifetime 2.5 times requirement for HL-LHC.
BIS78 RPC construction in progress.
Design optimization for Phase-II upgrade.



New Small-Diameter Muon Drift Tube (sMDT) Chambers

Reduction of driftt tube diameter from 30 mm to 15 mm and otherwise unchanged operating conditions increases the rate capability to > 30 kHz/cm².
14 sMDT chambers operated in ATLAS in run 2. 5 µm wire positioning accuracy achieved.
BIS78 sMDT chamber construction completed (pilot project for the Phase-II upgrade).
BIS1-6 sMDT design completed. Serial production in 2020-2023 at two production sites.

Automated drift tube assembly in clean room

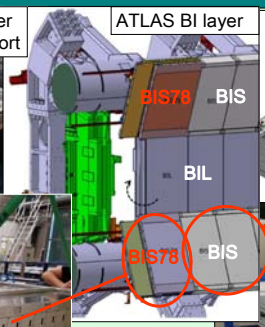
Positioning of tube ends in jigging matrix with 5 µm accuracy

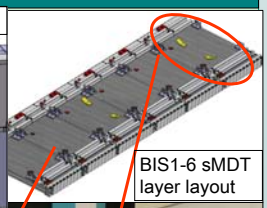
Automated glueing of drift tube layers

BIS sMDT and RPC Chambers for Run 3 and HL-LHC

Integrated BIS7 RPC chamber mounted in mechanical support

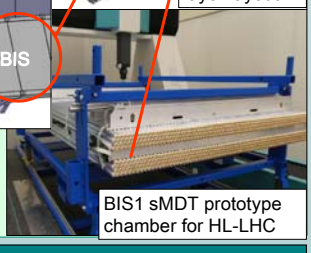
ATLAS BI layer





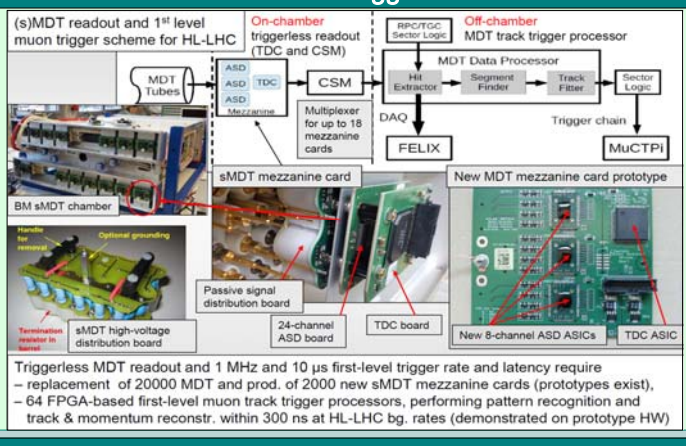
BIS1-6 sMDT layer layout

Integrated BIS78 sMDT and RPC chamber



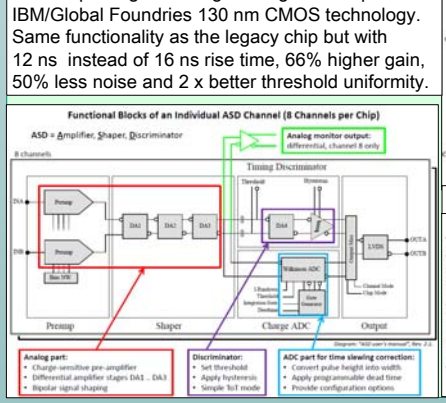
BIS1 sMDT prototype chamber for HL-LHC

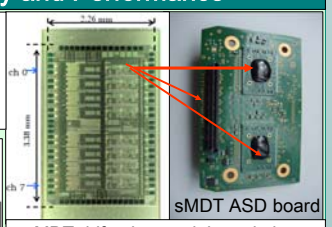
MDT Frontend Electronics and Triggerless Readout for HL-LHC



New ASD ASIC Functionality and Performance

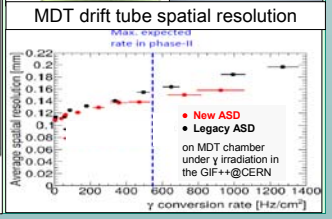
ASD chip design and engineering run completed in IBM/Global Foundries 130 nm CMOS technology.
Same functionality as the legacy chip but with 12 ns instead of 16 ns rise time, 66% higher gain, 50% less noise and 2 x better threshold uniformity.





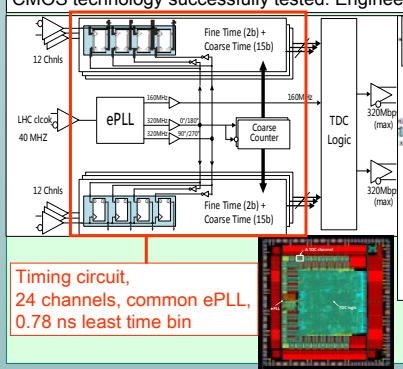
sMDT ASD board

MDT drift tube spatial resolution

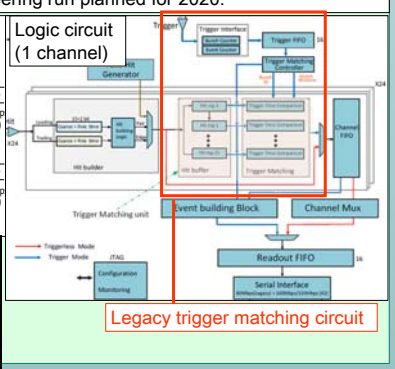


New TDC ASIC Functionality and Performance

The TDC chip combines the new continuous readout mode for HL-LHC operation with the legacy triggered mode needed for chamber testing. Full prototype chip in TSMC 130 nm CMOS technology successfully tested. Engineering run planned for 2020.



Timing circuit,
24 channels, common ePLL,
0.78 ns least time bin



Legacy trigger matching circuit