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# The ATLAS Hardware Track Trigger design towards first prototypes

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## Summary

In the High Luminosity LHC, planned to start with Run 4 in 2026, the ATLAS experiment will be equipped with the Hardware Track Trigger (HTT) system, a dedicated hardware system able to reconstruct tracks in the silicon detectors with short latency. This HTT will be composed of about 700 ATCA boards, based on new technologies available on the market, like high speed links and powerful FPGAs, as well as custom-designed Associative Memories ASIC (AM), which are an evolution of those used extensively in previous experiments and in the ATLAS Fast Tracker (FTK).

The HTT is designed to cope with the expected extreme high luminosity in the so called L0-only scenario, where HTT will operate at the L0 rate (1 MHz). It will provide good quality tracks to the software High-Level-Trigger (HLT), operating as coprocessor, reducing the HLT farm size by a factor of 10, by lightening the load of the software tracking.

All ATLAS upgrade projects are designed also for an evolved, so-called "L0/L1" architecture, where part of HTT is used in a low-latency mode (L1Track), providing tracks in regions of ATLAS at a rate of up to 4MHz, with a latency of a few micro-seconds. This second phase poses very stringent requirements on the latency budget and to the dataflow rates.

All the requirements and the specifications of this system have been assessed. The design of all the components has being reviewed and validated with preliminary simulation studies. After these validations are completed, the development of the first prototypes will start. In this paper we describe the status of the design review, showing challenges and assessed specifications, towards the preparation of the first slice tests with real prototypes.


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