RD53A: a large scale pixel chip demonstrator for ATLAS and CMS pixel phase 2 upgrades

F. Loddo
INFN-BARI
flavio.loddo@ba.infn.it

Outline

- RD53 Collaboration
- RD53A: motivations and specs
- Floorplan and implementation strategy
- Test systems
- Preliminary test results:
  - CDR/PLL
  - Digital & Analog scans
  - Calibration, bias and monitoring
  - Synchronous FE
  - Linear FE
  - Differential FE
  - ShuntLDO
- Conclusions and future plans

RD53 Collaboration

RD53 is a collaboration among **ATLAS-CMS** communities for the development of **LARGE scale pixel chips for ATLAS/CMS phase-2 upgrades**

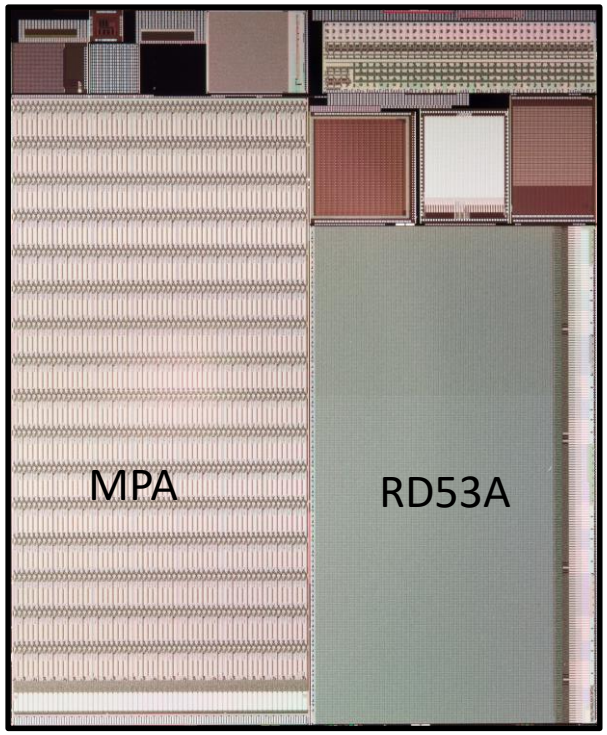
24 Institutions from Europe and USA:
Annecy-LAPP, Aragon, Bergen, Bonn, CERN, FH-Dortmund, FNAL, INFN (Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino), LBNL, Marseille-CPPM, New Mexico, NIKHEF, Orsay–LAL, Paris-LPNHE, Prague IP-FNSPE-CTU, RAL-STCF, Sevilla, Santa Cruz

- **TSMC 65 nm CMOS** is the chosen technology
- **RD53 goals**:
  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
  - Development of **methodology** to efficiently design large complex mixed signal chips
  - Design of a **shared rad-hard IP library**
  - Design and characterization of **full sized pixel array chip**

RD53A

- **RD53A** is intended to demonstrate, in large format IC, the suitability of the chosen 65nm CMOS technology for the innermost layers of particle trackers for the HL-LHC upgrades of ATLAS and CMS

- RD53A is not intended to be a final production chip:
  - size: 20 x 11.8 mm^2 (half size of production chip)
  - 400 columns x 192 rows (50 x 50 μm^2 pixels)
  - contains design variations for testing purposes
  - wafer scale production allows prototyping of bump bonding assembly with sensor
  - will form the basis for production designs of ATLAS and CMS: architecture designed to be easily scalable to a full scale chip



- Submitted at the end of August 2017

- Shared engineering run (Process Split) with CMS MPA/SSA and other test chips for cost sharing

RD53A Specifications

Technology	65 nm CMOS
Pixel size	50x50 um^2
Pixels	400x192 = 76800 (50% of production chip)
Detector capacitance	< 100 fF (200 fF for edge pixels)
Detector leakage	< 10n A (20 nA for edge pixels)
Detection threshold	<600 e-
In-time threshold	<1200 e-
Noise hits	< 10^{-6}
Hit rate	< 3 GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1 MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤ 1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500 Mrad at -15°C
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1 W/cm^2 including ShLDO losses
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

http://cds.cern.ch/record/2113263

RD53A core design team

RD53A chip: Jorgen (CERN), Maurice (LBNL)
- Specifications
- Documentation
- General organization

RD53A chip integration/verification: Flavio (Bari), Deputy: Tomasz (Bonn)

Floorplan: Flavio(Bari), Dario(LBNL)
- Pixel array, Bump pad
- EOC
- Power distribution
- Bias distribution
- Analog/digital isolation
- Integration/verification

Analog FEs: Luigi (Bergamo/Pavia), Ennio (Torino), Dario (LBNL)
- Specification/performance
- Interface (common)
- Analog isolation
- Digital/timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Distribution of global analog signals
- Verification of integration

Calibration, Monitoring and IP integration: Francesco (Bergamo/Pavia) , Mohsine (CPPM), Flavio (Bari)
- Specification/performance
- Interface
- Analog isolation
- Digital/ timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Verification of integration

Digital: Tomasz (Bonn)
- **Verification framework: Elia (CERN), Sara (CERN)**
  - Framework
  - Hit generation/ import MC
  - Reference model / score board
  - Monitoring/verification tools
  - Generic behavioural pixel chip
  - SEU injection
- **Architecture: Elia (CERN), Sara (CERN), Andrea (Torino), Luca (Torino),**
  - Evaluation – choice: Performance, Power, Area, ,
  - Simulation/Optimization
  - Functional Verification
  - SEU immunity
- **Pixel array/pixel regions: Sara (Cern), Andrea (Torino)**
  - Latency buffer
  - Core/column bus
- **Readout/control interface: Roberto (Pisa), Francesco (Parigi)**
  - Data format/protocol
  - Rate estimation / Compression
  - Implementation
- **Configuration: Roberto (Pisa), Andrea (Torino), Luca (Torino)**
  - External/internal interface
  - Implementation
- **Implementation: Dario (LBNL), Luca(Torino), Andrea (Torino), Sara (CERN)**
  Script based to "quickly" incorporate architecture/RTL changes
  - RTL - Synthesis
  - Functional verification
  - SEU verification
  - P&R
  - FE/IP integration
  - Clock tree synthesis
  - Timing verification
  - Power verification
  - Physical verification
  - Final chip submission

Digital lib.: Dario (LBNL), Mohsine (CPPM), Sandeep (FNAL)
- Customized rad tol library
- Liberty files (function, timing, etc.) Characterized for radiation
- Custom cells (Memory, Latch, RICE)
- Integration with P&R
- Radiation tolerance
- Integration in design kit

Power: Michael (Dortmund), Sara (CERN), Stella (CERN)
- Shunt-LDO integration
- On-chip power distribution
- Optimization for serial powering
- System level power aspects
- Power Verification

IO PADFRAME: Hans (Bonn)
- Wirebonding pads, ESD, SLVS, Serial readout**, Shunt-LDO**, analog test input/output

Testing optim.: Luca (Torino)
- Testability
- Scan path

Support and services:
- Tools, design kit: **Wojciech (CERN)**
- Cliosoft repository: **Elia (CERN), Wojciech (CERN)**
- Radiation effects and models: **Mohsine (CPPM)**

+ IP designers from RD53 Institutes

Technology

Technology: TSMC 65 nm

- High density required in small pixels for hit storage during trigger latency
- 130 nm not enough dense
- Radiation tests on other 65 nm tech. show similar or worse behaviour

RD53A metal stack : 1p9m6x1z1u + RDL : 7-thin, 1-thick, 1-UTM , RDL (28k)

Used devices:

- Core transistors:
  - a) Standard Vt
  - b) Low Vt
  - c) High Vt
- High Value Resistors
- Triple well isolation
- NO I/O MOSFETs
- NO MIMCAPs

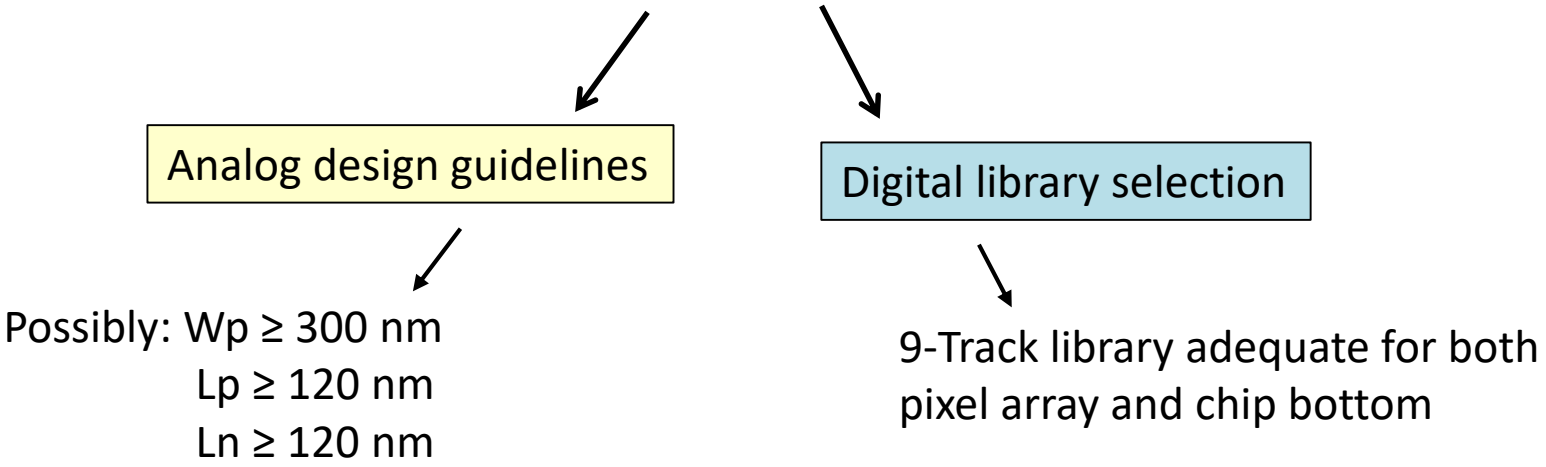
Radiation tolerance

- RD53A should be capable to operate at least up to 500 Mrad

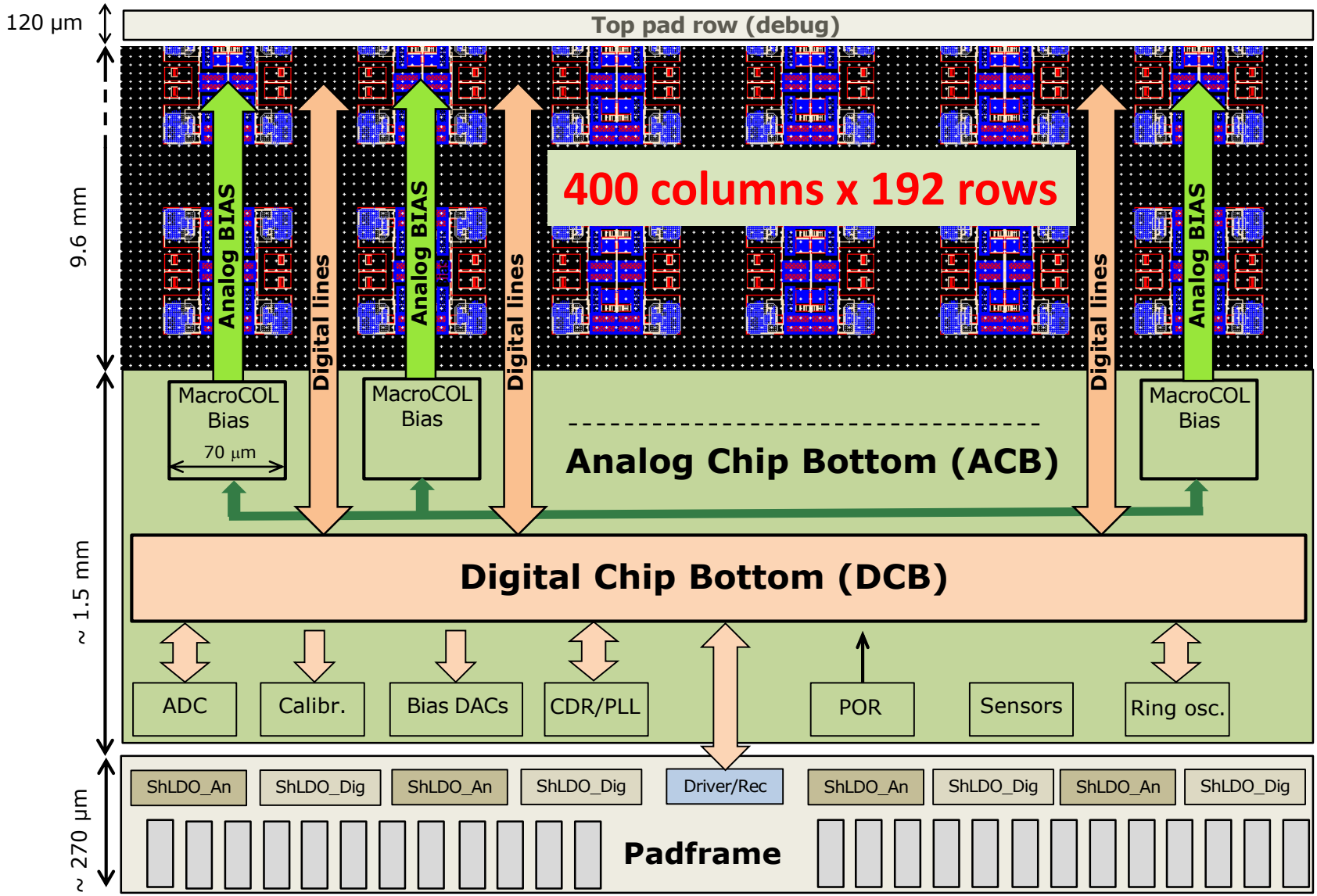
- Extensive irradiation campaign to qualify the technology
  - Prototypes of all IPs / Fes, small scale demonstrators: **FE65_P2**, **Chipix65**
  - **DRAD** Chip: test chip to study effects on std cells

- Significant radiation damage above 100 Mrad:
  - Analog: transconductance, Vt shift
  - Digital: speed degradation

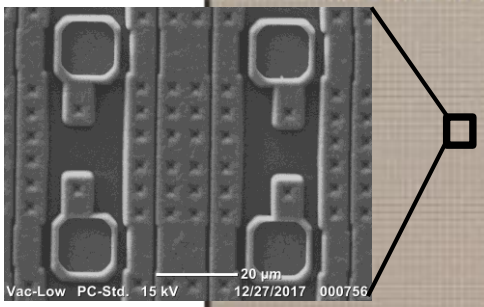
- 200 Mrad and 500 Mrad simulation models were developed to “predict” the circuit behaviour during design phase



RD53A functional floorplan



RD53A



Chip size: 20.066 x 11.538 mm²
400x192

- **Aug. 31, 2017: Submission**
- **Dec. 6, 2017: First chip test**
- **Mar. 15, 2018: 25 wafers ordered**
- **Apr. 13, 2018: First bump-bonded chip test**

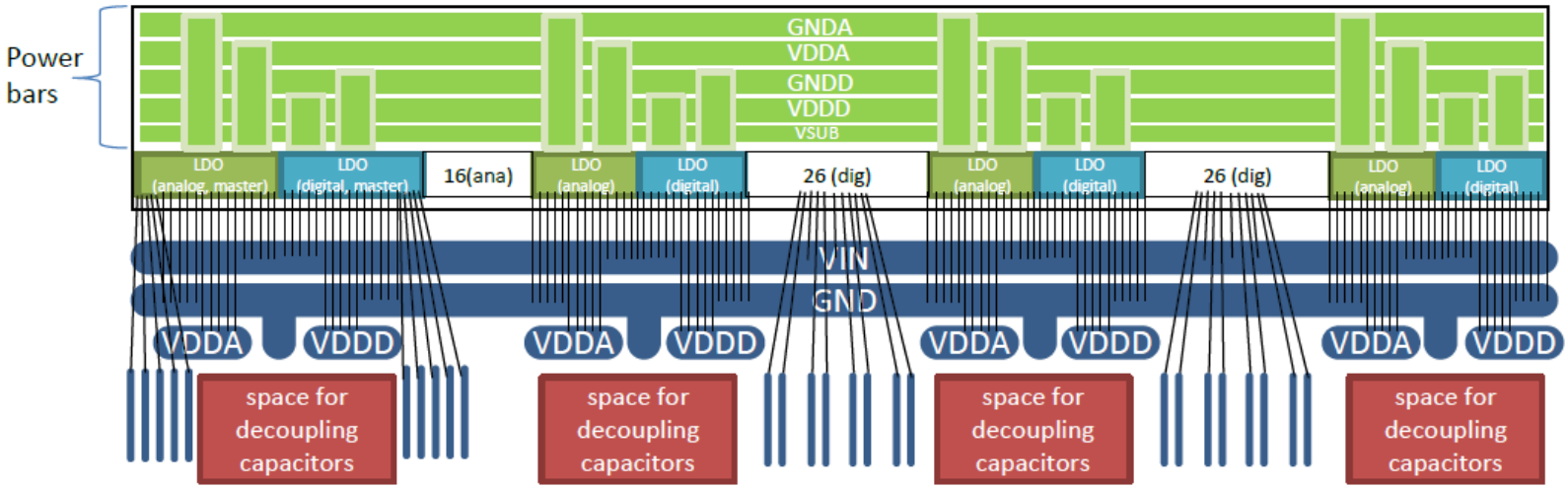
Chip doc on CDS: http://cds.cern.ch/record/2287593

Power domains and isolation methodology

Two power domains → two ShuntLDOs

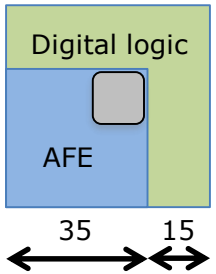
- analog (VDDA, GNDA)
- digital (VDDD, GNDD)
- Analog and digital circuitry in separated deep N-wells for maximum possible substrate isolation
- Throughout the chip no active device on the global p-substrate
- Global p-substrate biased by VSUB

- ShuntLDOs are located in the Padframe and distributed along the full chip width
- 4 blocks with sets of 5 Wire Bonds per power net
- Power lines come only from the bottom
- GNDA-GNDD-VSUB connected off-chip

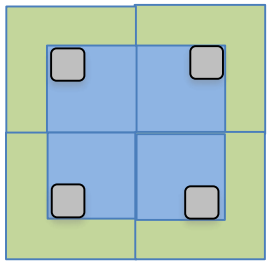


50μm X 50μm Pixel floorplan

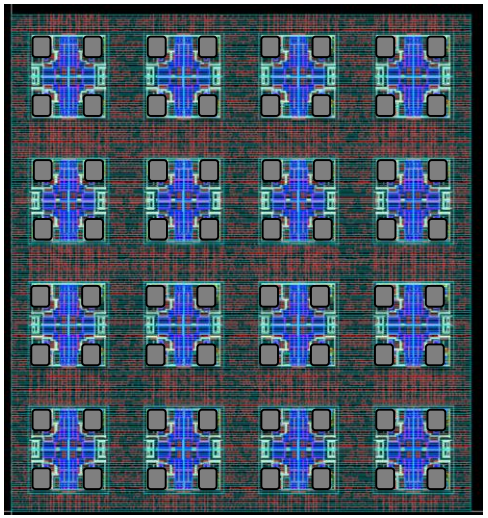
- 50% Analog Front End (AFE), 50% digital cells
- The pixel matrix is built up of **8 x 8 Pixel Cores**
  → **16 analog islands (2x2 quads)** embedded in a flat digital synthesized sea
- A Pixel Core can be simulated at transistor level with analog simulator
- All Cores (for each AFE flavour) are identical → Hierarchical verifications



PIXEL



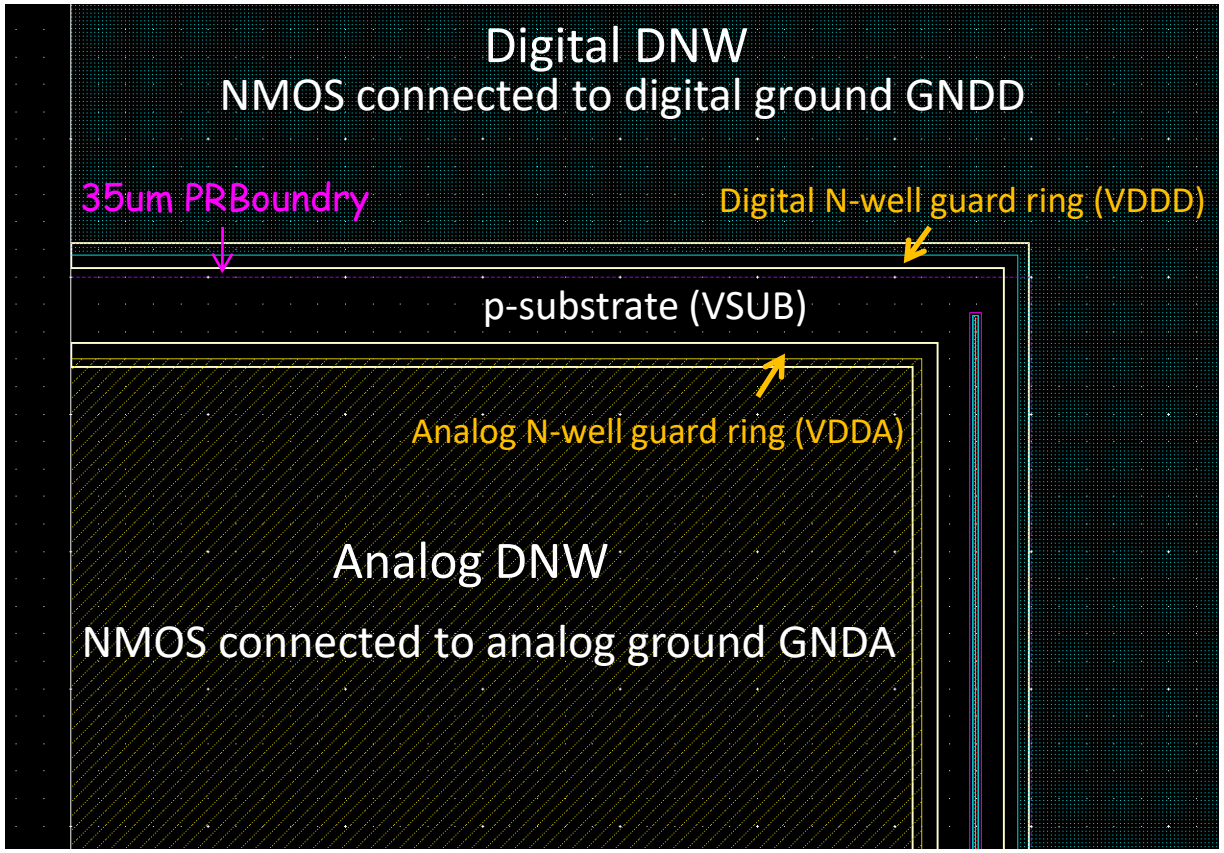
ANALOG ISLAND



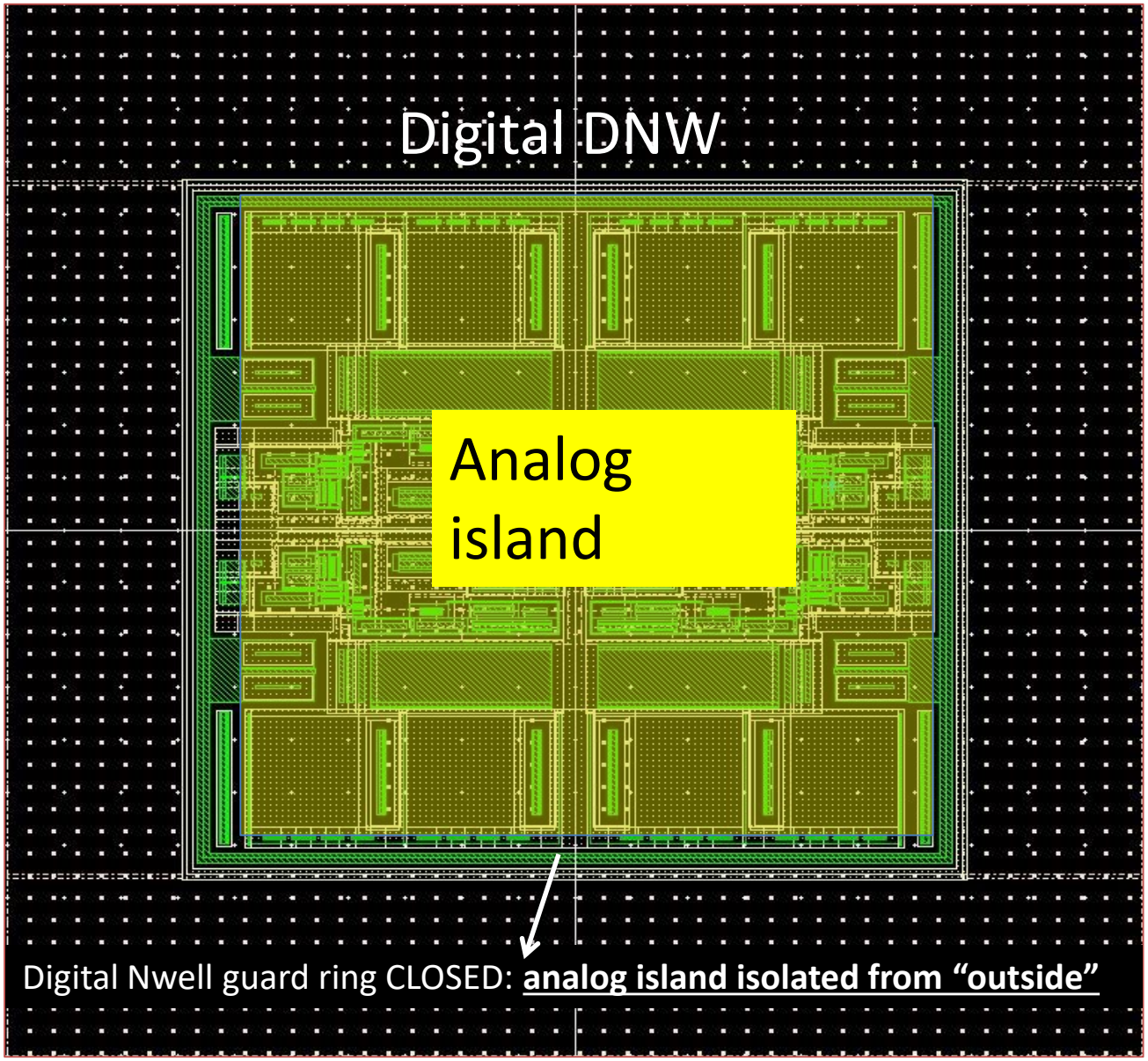
PIXEL CORE

Pixel substrate floorplan

- Analog FE in “analog” Deep Nwell with local ground = GNDA
- Digital logic in “digital” Deep Nwell with local ground = GNDD
- Global p-substrate biased by VSUB



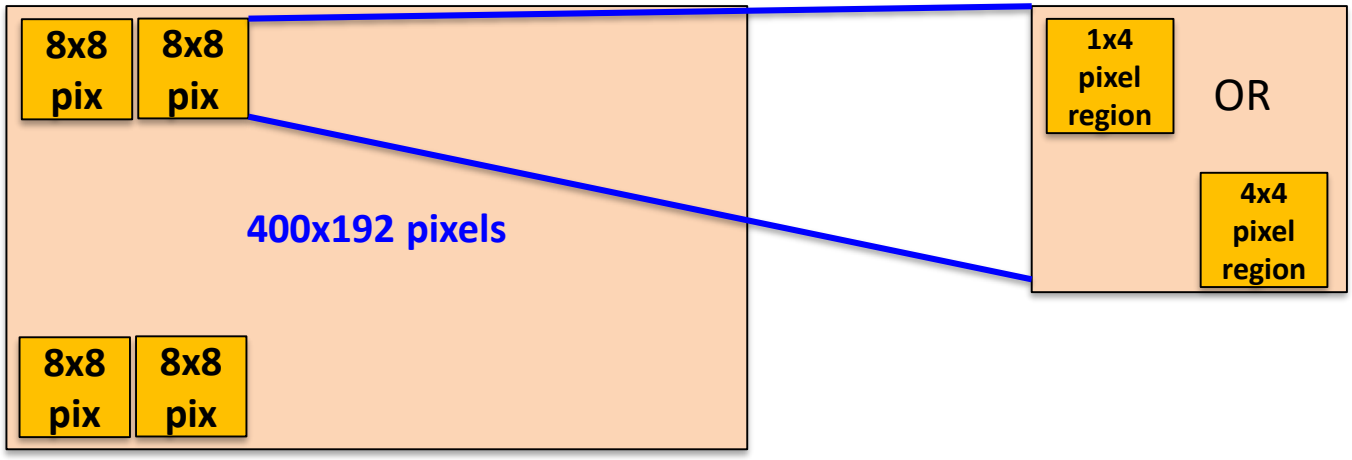
2x2 analog quad



Pixel array logic organization

Array organization

basic layout unit: **8x8 digital Pixel Core → synthesized as one digital circuit**



- **One Pixel Core** contains **multiple Pixel Regions (PR) and** some **additional arbitration and clock logic**
- **Pixel Regions share most of logic and trigger latency buffering**

Distributed Buffering Architecture (DBA) (FE65_P2 based (1x4)):
- distributed TOT storage
- Integrated with LIN and DIFF FE

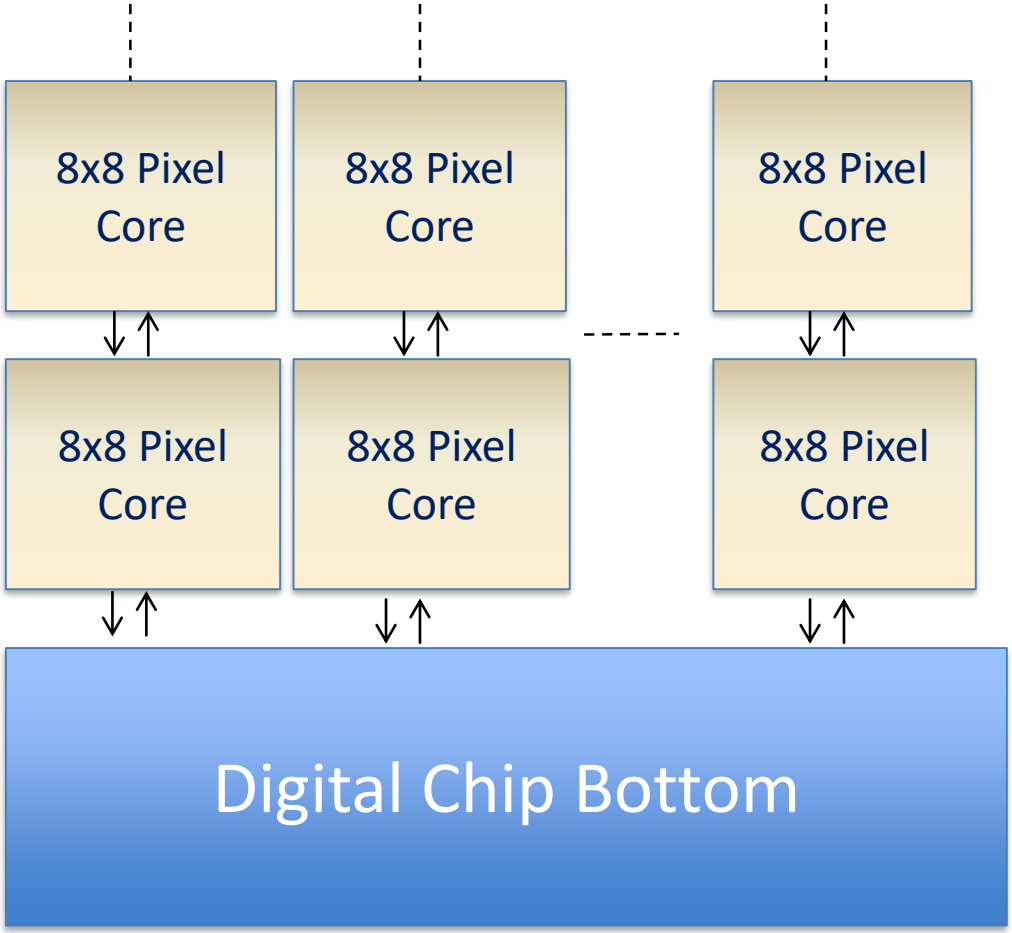
Centralized Buffering Architecture (CBA) (Chipix65 based (4x4)):
- centralized TOT storage
- ~ same power
- ~ 10% less area
- Integrated with SYNC FE

Pixel array logic organization

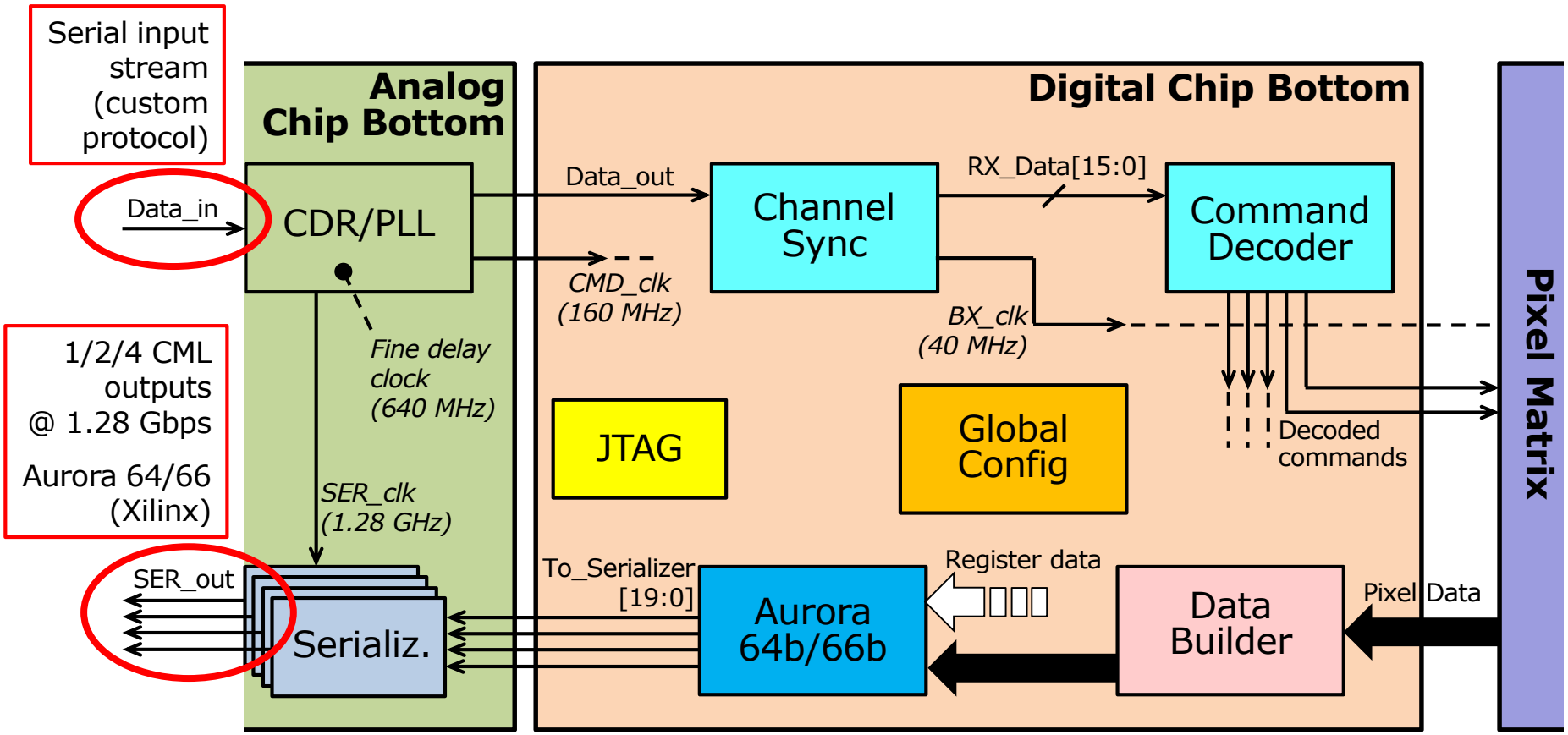
• Pixel Cores are stacked-up: each Core receives all input signal from the previous Core (closer to the Digital Chip Bottom) and regenerates the signals for the next Core

• The timing critical clock and calibration injection signals are internally delayed to have a uniform timing (within 2 ns)

• Cores are abutted
→ no external routing for connections
→ efficient hierarchical physical verifications

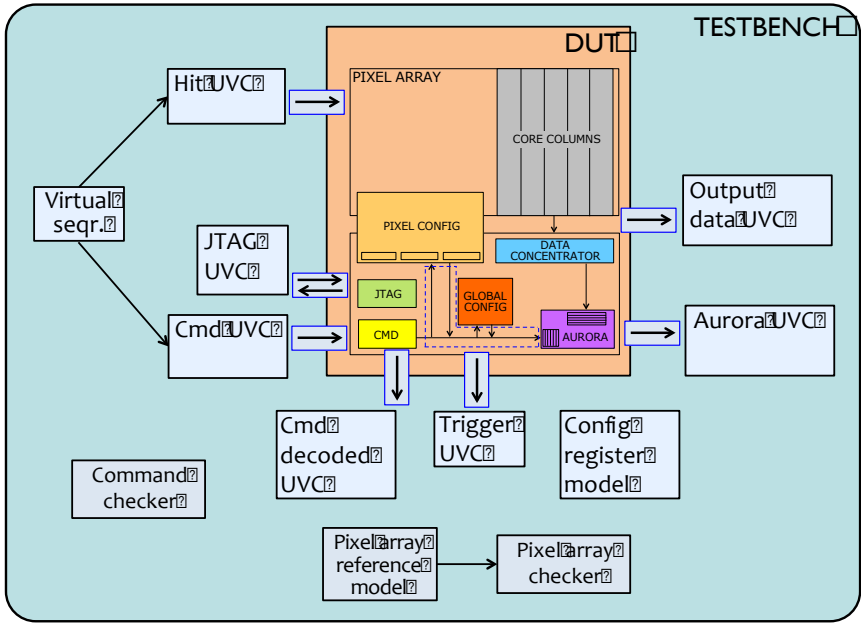


Digital Chip Bottom



RD53A Verification

- ***VEPIX53***: simulation and verification environment (UVM) supporting design from initial architectural modeling to final verification
  - generation of different kinds of input stimuli (internally generated or from Monte Carlo)
  - automated verification features
- Pixel array architecture performance metrics: *hit loss* and *latency buffer occupancy*
- *Comparable performance* found between CBA and DBA architectures in terms of buffer overflow hit loss



Main interface verification components (UVC):

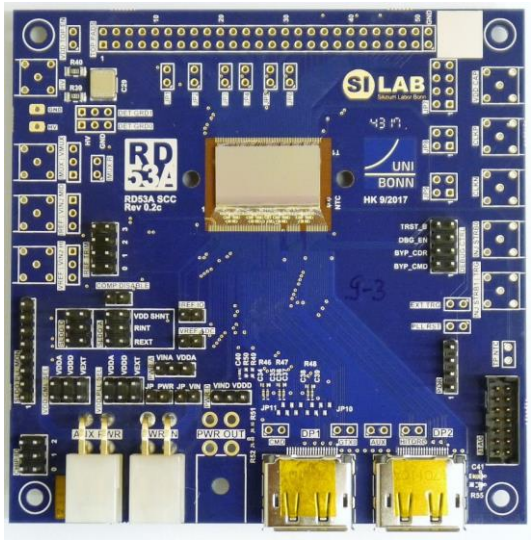
- Hit (sensor pixel hit data)
- Command (custom input protocol for control and trigger)
- Aurora (monitor pixel chip output)
- JTAG

Automated verification components:

- Pixel array reference model (predict output hits according to trigger)
- Pixel array checker (compare predicted output vs real output)
- Lost hits classifiers
- Configuration register model (reference for operations to global configuration and pixel configuration)

RD53A test

RD53A Single Chip Card

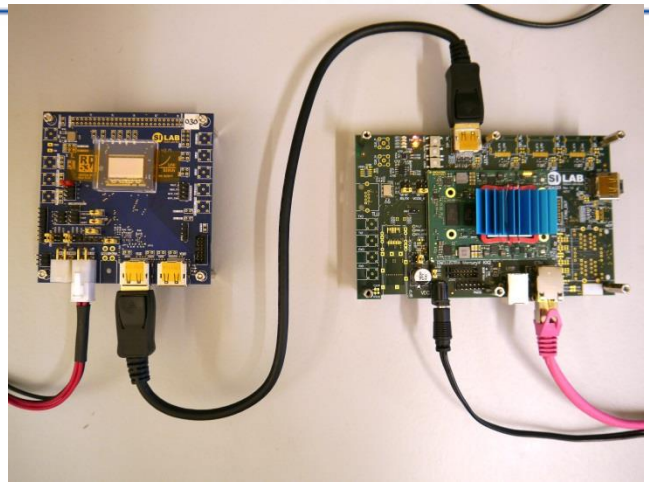


- **Two test systems**:
  - **BDAQ53** – Bonn University → https://gitlab.cern.ch/silab/bdaq53
  - **YARR** – LBNL → https://gitlab.cern.ch/YARR/YARR
- **Functional testing** of RD53A (on-going)
- **Distribution** of setups across collaboration has started

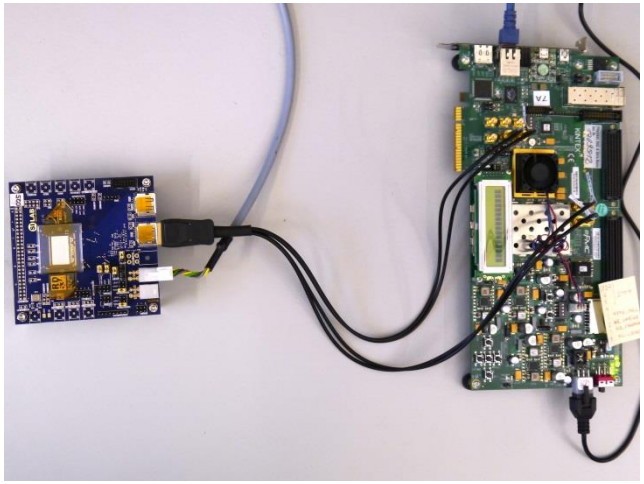
RD53A public plots: https://twiki.cern.ch/twiki/bin/view/RD53/RD53APublicPlots

BDAQ53 Test System

- BDAQ53 FPGA card
  - Standard DP cable to connect SCC

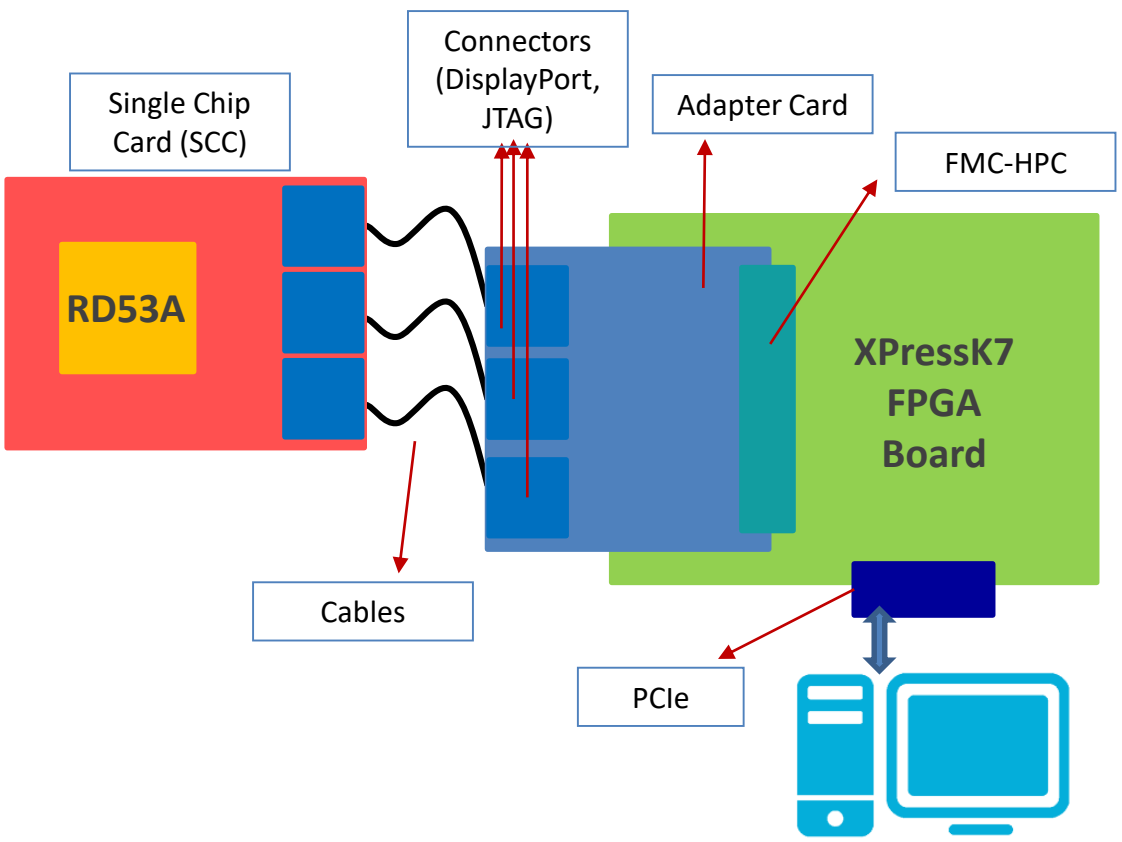


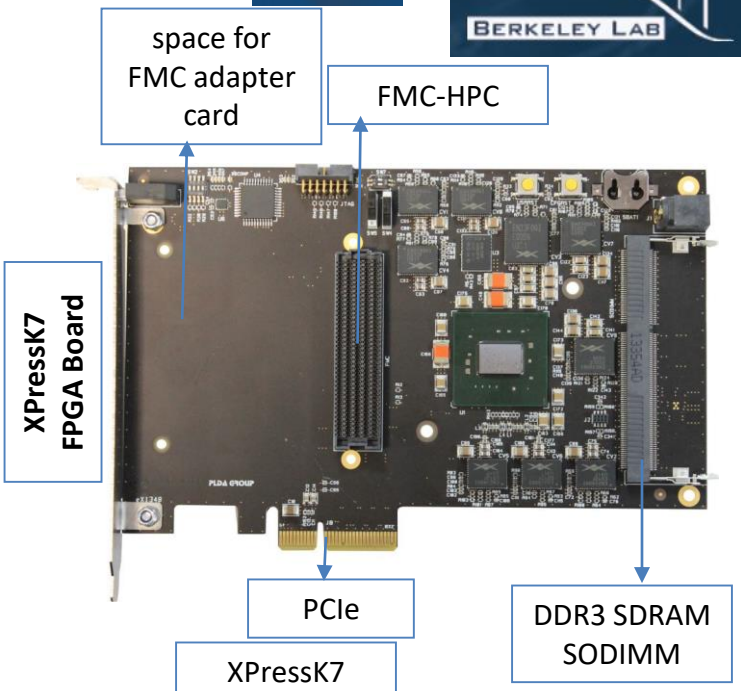
- Xilinx KC705 development board
  - DP to SMA adapter cable (single Aurora lane)
  - Planned support for the FMC adapter card

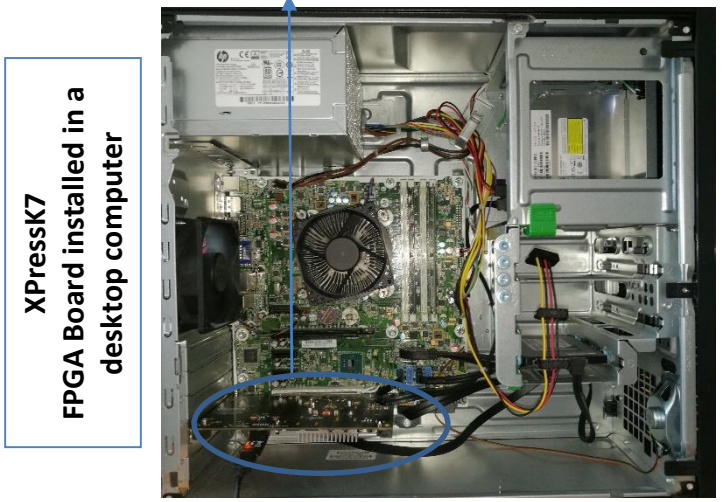


- FW and SW compatible with both options
- Both are using Gigabit Ethernet for data transfer
- Developed beforehand based on chip simulation
- Now in a stable state

YARR System


Single Chip Card (SCC)
Connectors (DisplayPort, JTAG)
Adapter Card
FMC-HPC
RD53A
XPressK7 FPGA Board
Cables
PCIe


space for FMC adapter card
FMC-HPC
XPressK7 FPGA Board
PCIe
DDR3 SDRAM SODIMM
XPressK7


XPressK7 FPGA Board installed in a desktop computer

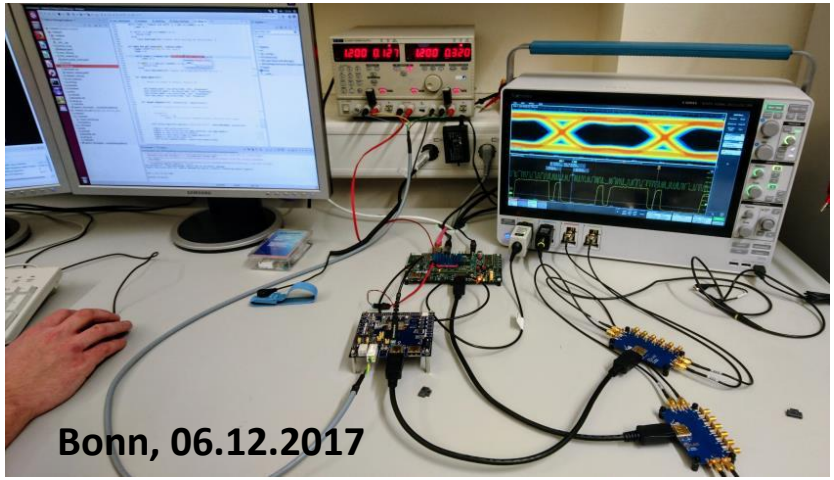
RD53A testing plans

- **Radiation campaigns** in different sites
  - X-rays @CERN
    - March 2018: done
    - May 2018: on-going (unbiased chips)
  - Low dose rate X-rays irradiation (May-June)
  - Gammas, protons, …. : being planned

- **Wafer probing**:
  - Developed needle probe cards for fast sequential testing of RD53A on wafers
  - Probe testing being debugged with single chips. Whole wafer probing to begin soon
- **Bump-bonding with first sensors**:
  - 3 wafers under processing at IZM for bump-bonding to CMS and ATLAS sensors. First chips received recently

RD53A measurements

- Preliminary results shown in next slides are from measurements performed by:
  - ❑ Bonn University
  - ❑ CERN
  - ❑ INFN Torino
  - ❑ LBNL
  - ❑ FH-DORTMUND



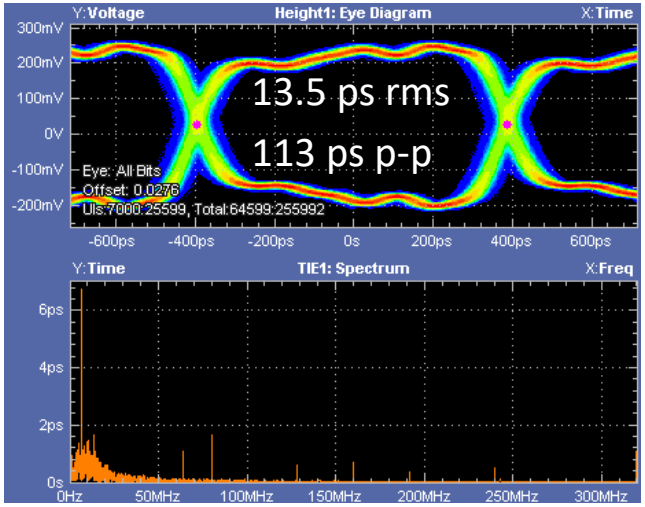
- **The chip is fully operating using its normal I/O ports (no backup)**
  - **160 Mbps CMD input (LVDS) → Clock + Data**
  - **CML output (Aurora link)**

- PLL locks
- Aurora link is stable (@ 1.28 Gbps)
- Command decoder responds → we can configure and readout the chip

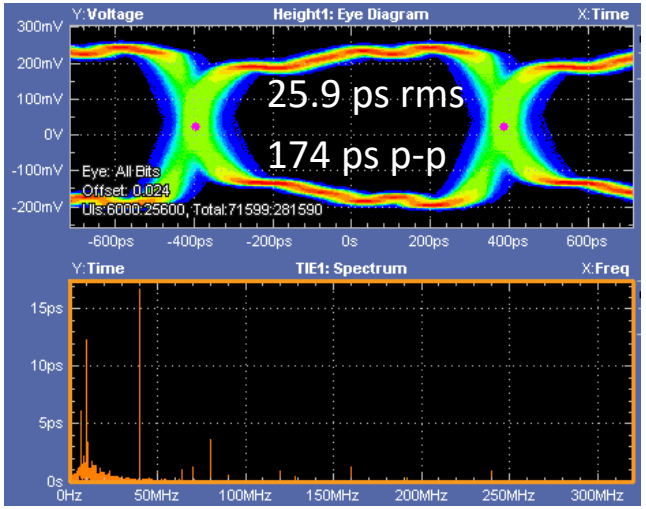
CDR/PLL

- The CDR/PLL recovers data and clock from input stream @ 160 MHz
- It works fine but in certain conditions we encounter a lock issue that can be solved with proper SCC configuration. This solution is under verification across supply, T and radiation and will allow to operate RD53A reliably in the different test sites
- Moreover, it exhibits a jitter higher than expected from simulations
- Output link jitter strongly influenced by chip activity

No CLK to matrix, all columns off



CLK send to matrix, all columns on

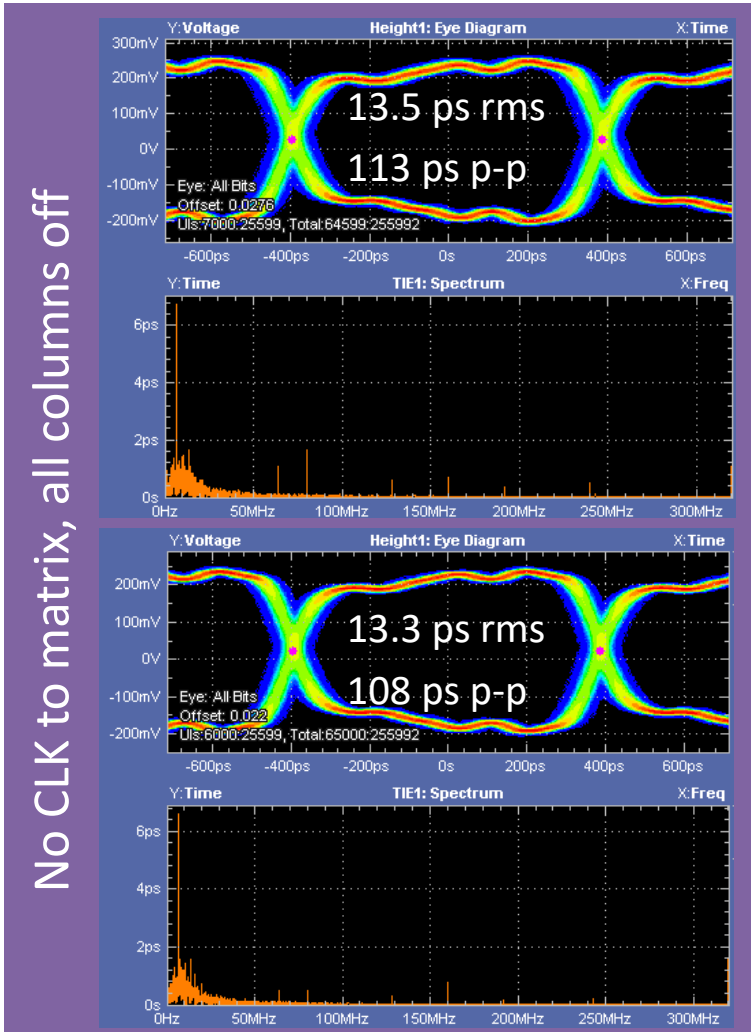


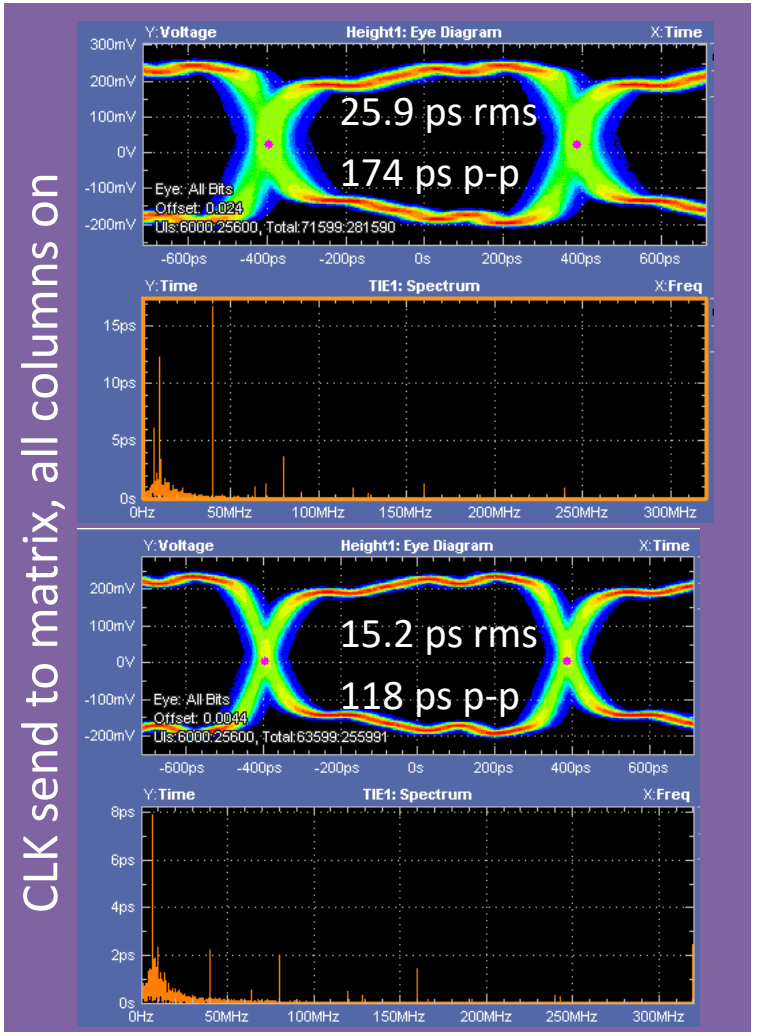
Jitter problem caused by missing buffers for the configuration bits
Confirmed by surgical fix in few chips using FIB (Focused Ion Beam) → see next slide

CDR/PLL post FIB measurements

Not modified

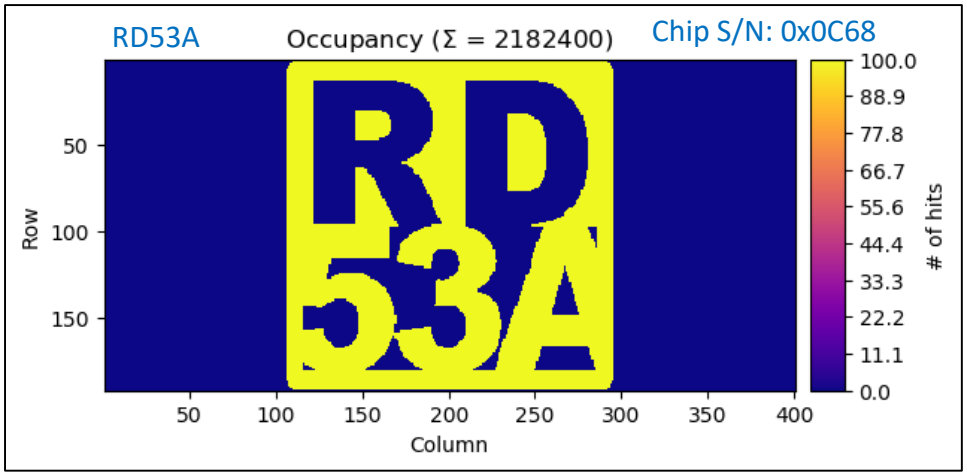
FIB edited



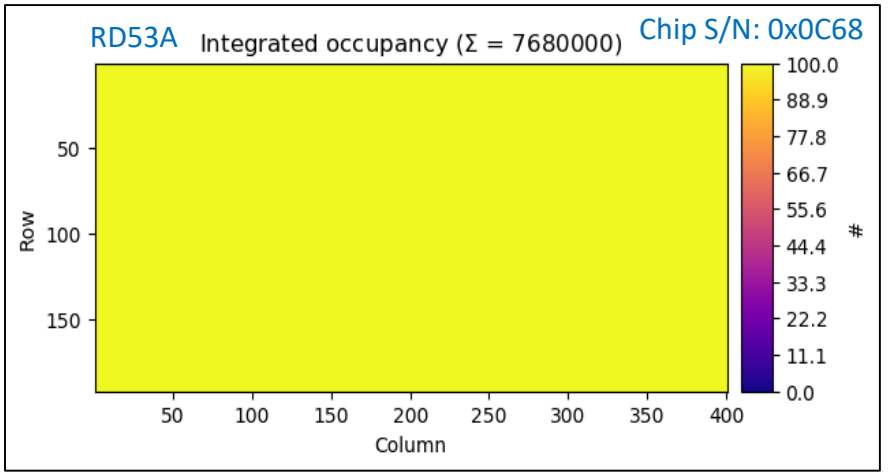


- Bug fix implemented for production chip
- Prototype submission in summer to test farther improvements

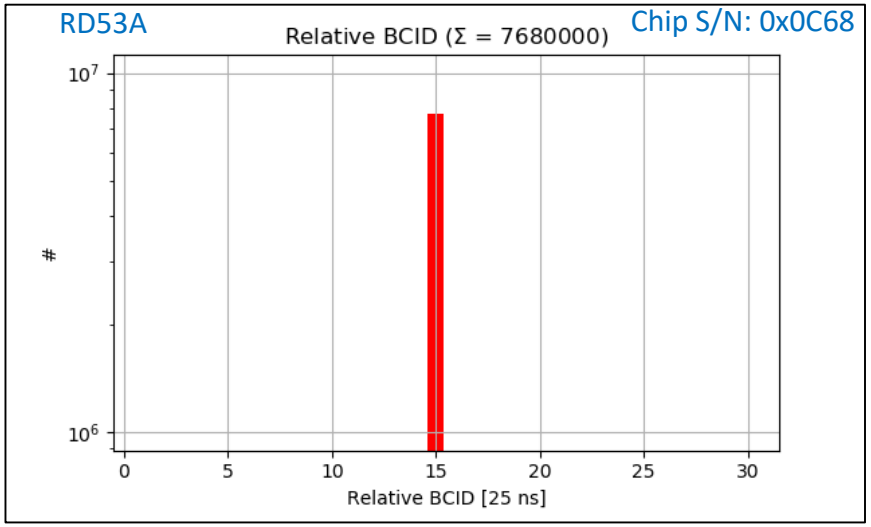
Digital scan

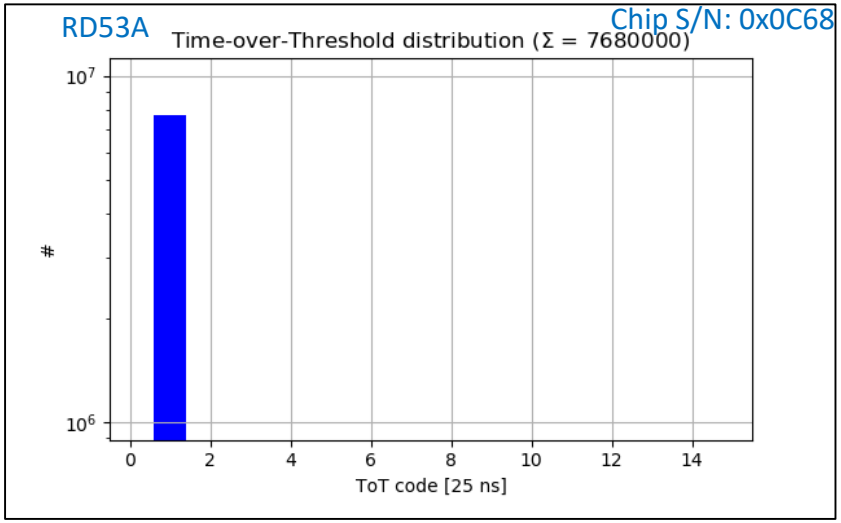


Complex mask



Full chip

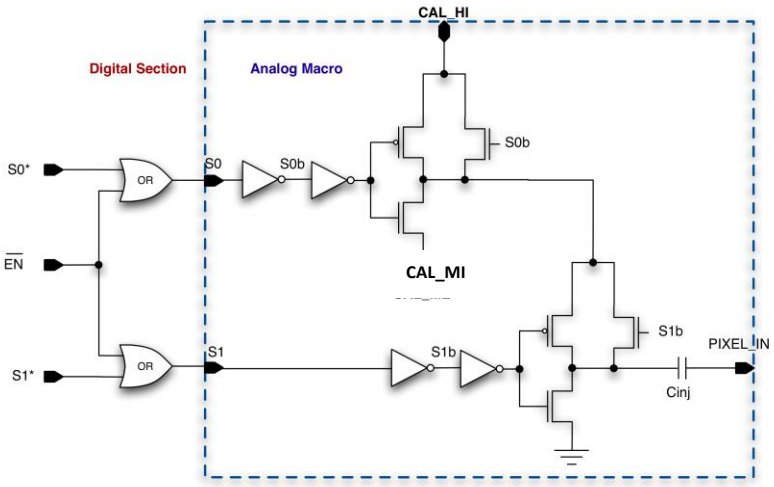


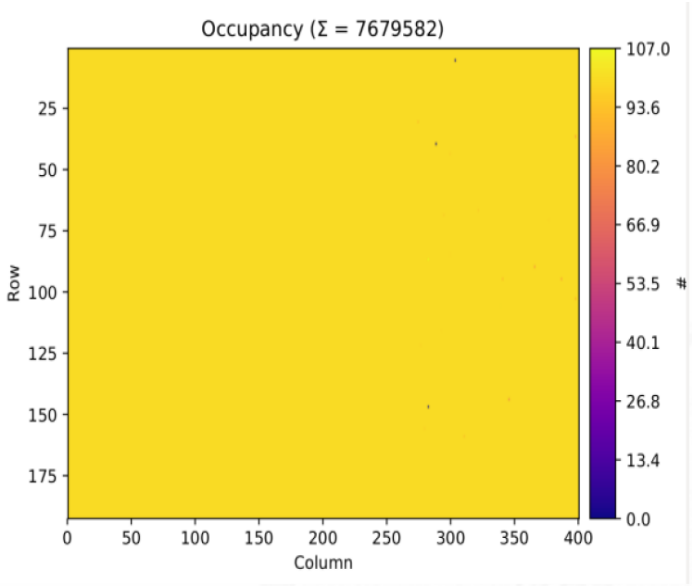


Analog scan

Calibration circuit (inside pixel)

- Local generation of the analog test pulse starting from 2 DC voltages CAL_HI and CAL_MI distributed to all pixels and a 3rd level (local GND)
- Two operation modes:
  1. Inject two consecutive signals of the same polarity
  2. Inject different charges in neighboring pixels at the same time
- Cal levels generated by 12 bit VDACs



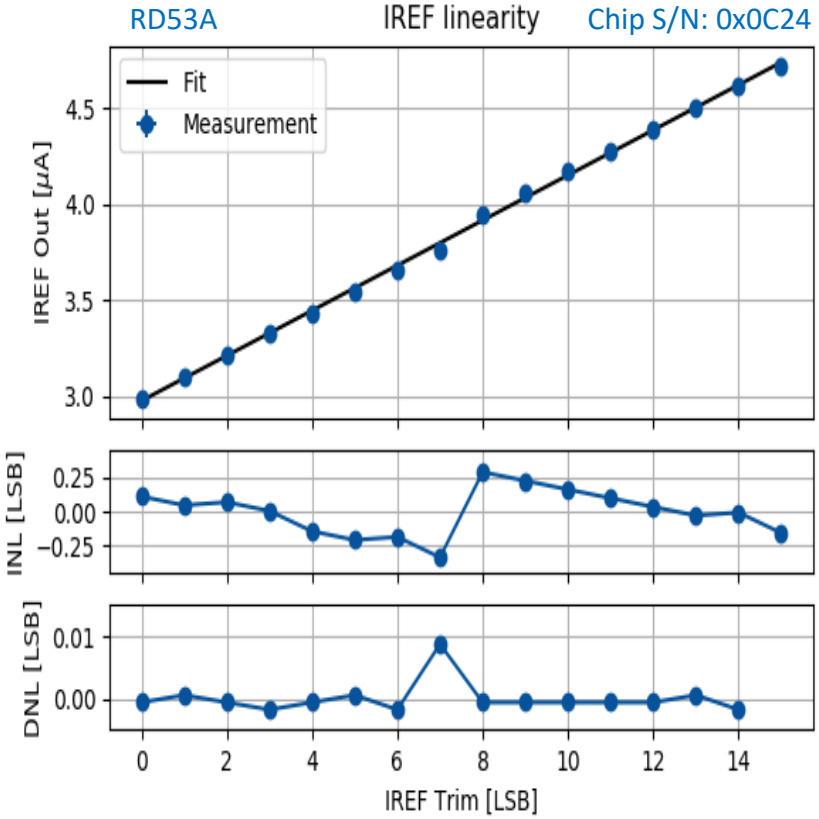


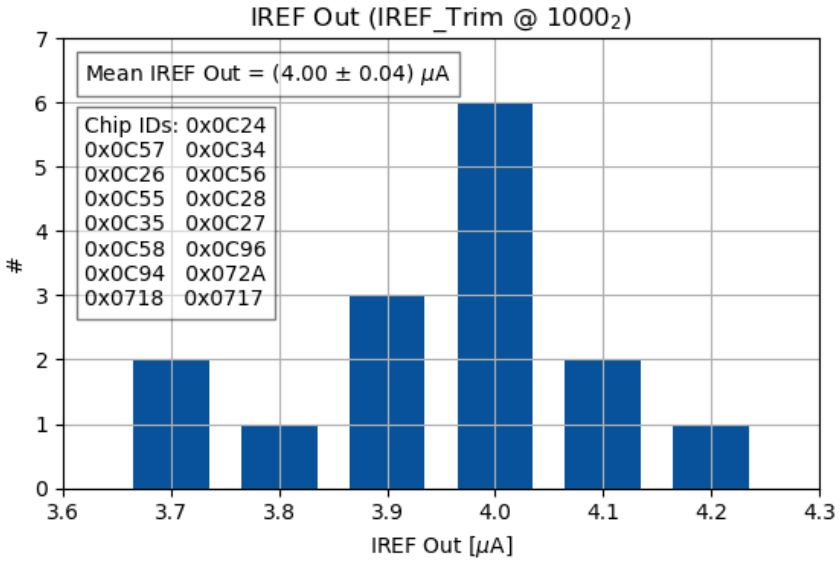
- Full chip responds
- High injection (30 ke-)

Bias, calibration and monitoring

IREF measurement and trimming

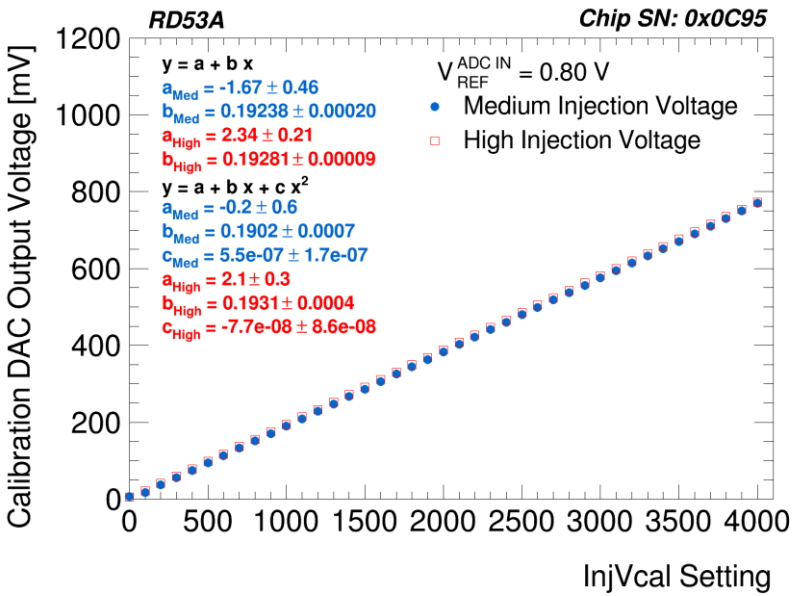
- All biases are provided by internal current DACs, using an internally generated reference current IREF (**4 µA** nominal) derived by a Bandgap Reference circuit (independent from T, tolerant to TID)
- To compensate for process variations, we can tune IREF by means of 4-bit DAC (wire bonding settings)

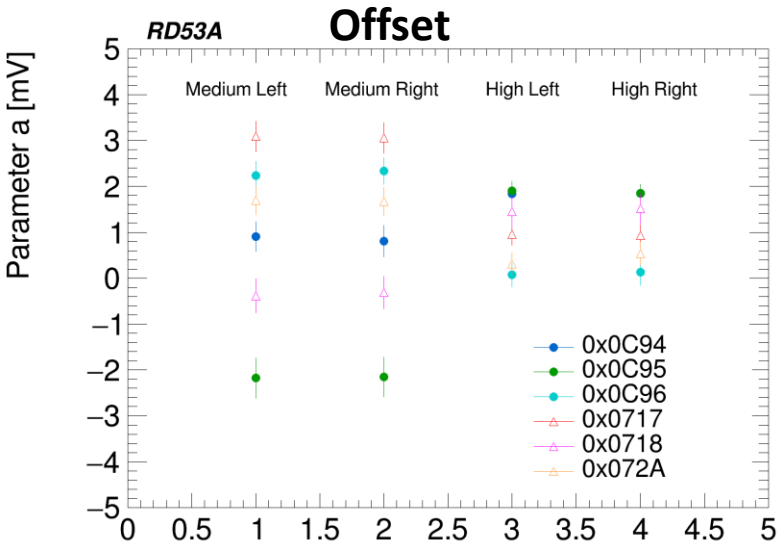


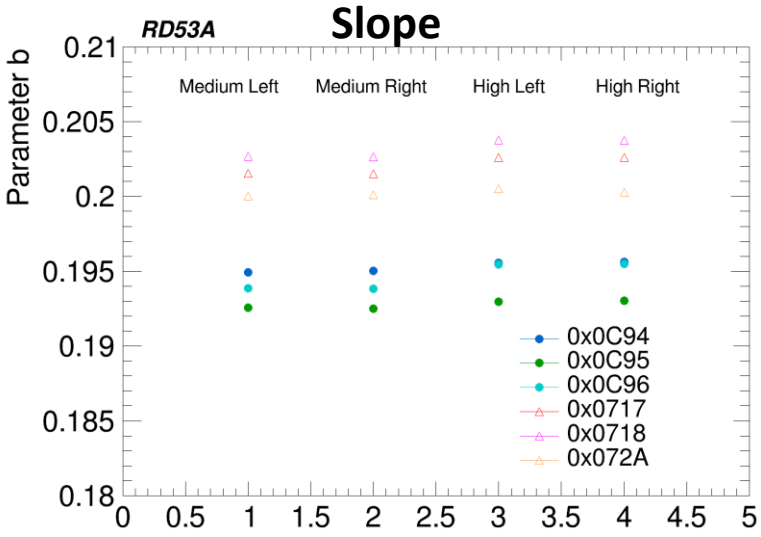


Statistical evaluation of the IREF output for IREF Trimming setting = 8 for a sample of 15 chips

Characterization of injection 12-bit DACs



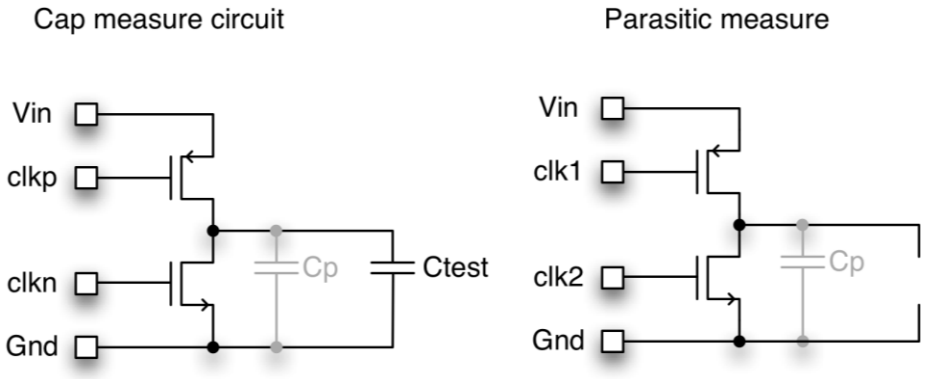


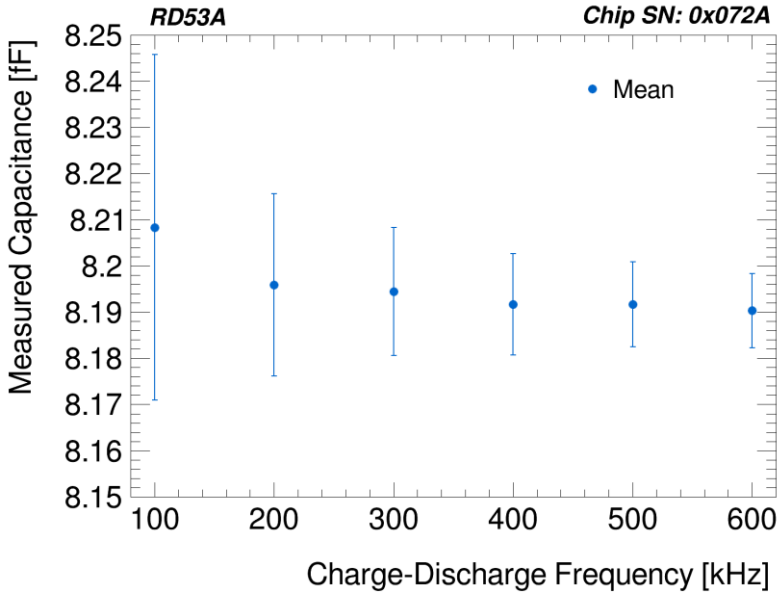


- Value of offset(a) and slope (b) from linear fit of CAL_HI and CAL_MI measured on the left and right sides of the chip (the chip has two monitoring outputs for each voltage).
- The plots shows results for three chips from each of two wafers. Circles are one wafer and triangles the other wafer.

Measurement of injection capacitance

- Each RD53A has two banks of 100 replicas of injector capacitors (top left – top right) for the purpose of measuring the capacitance
- Methodology: cyclically charging and discharging the banks using external non-overlapping clocks
- The capacitance can be deduced from the frequency and measured current
- A dummy bank without inj. capacitor replicas but all other metal and switches to be measured and subtracted



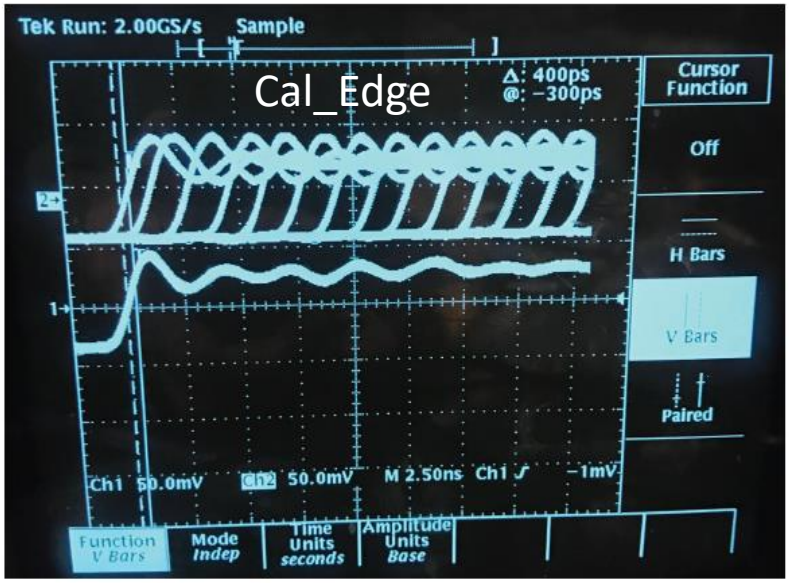


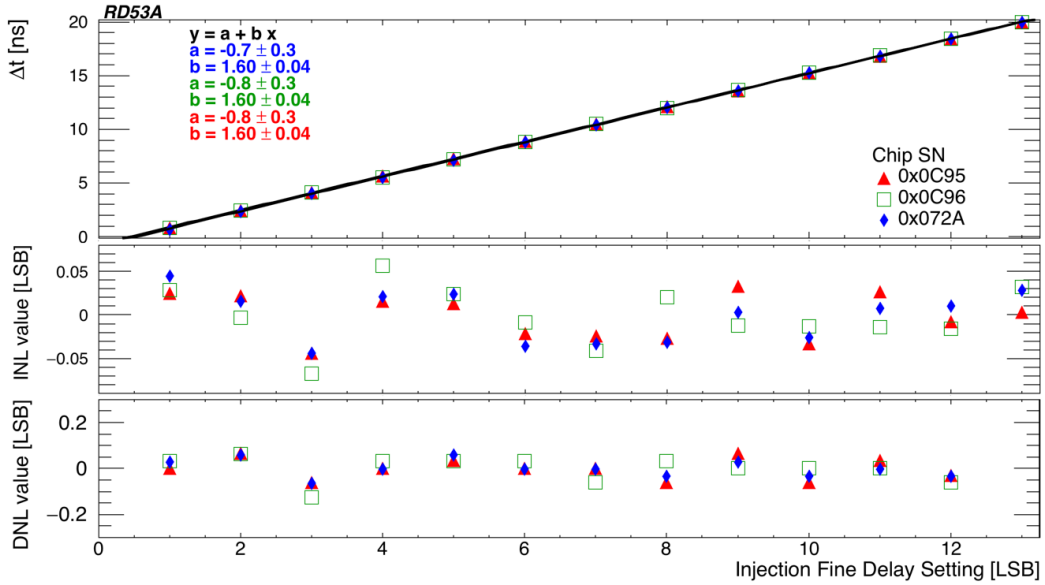
Good agreement with the nominal value (typical corner = 8.5 fF)

Considering C_{inj} ~ 8.2 fF → Q_{inj} ~ 10 e^-/ ΔVCAL (close to simulated value 12 e^-/ ΔVCAL)

Injection fine delay scan

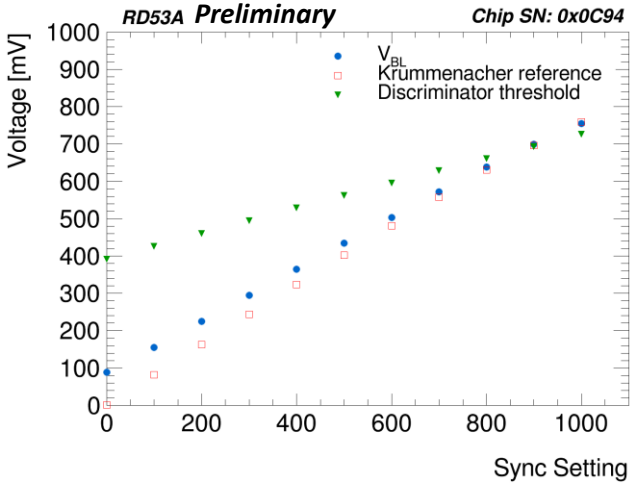
- The injection pulse can be delayed in steps of ~ 1.6 ns

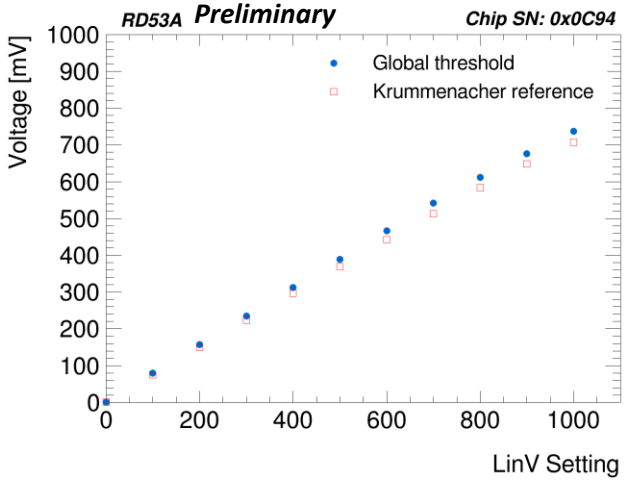


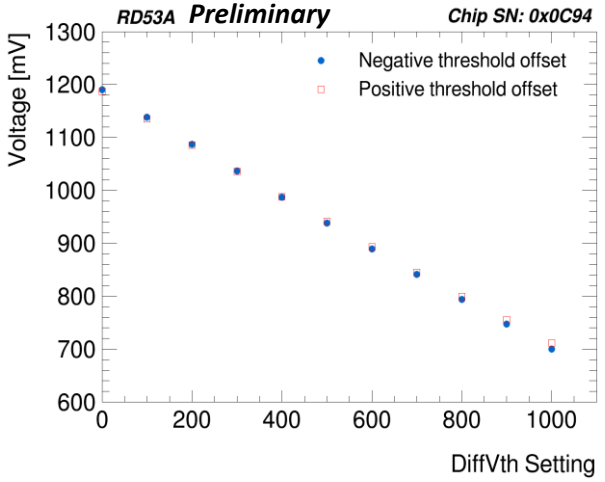


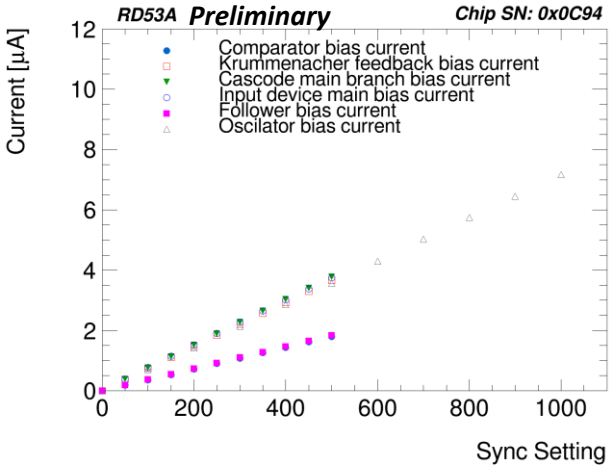
Scan of Bias 10-bit DACs

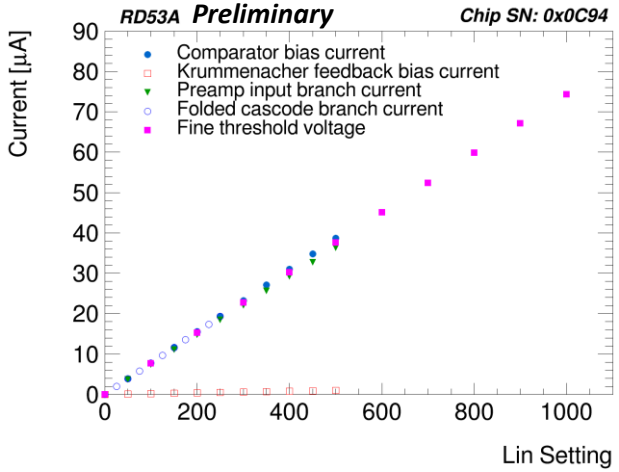
- All internal bias currents and voltages can be monitored using internal 12-bit ADC and can be accessed on two multiplexed outputs: IMUX and VMUX (used also for ADC calibration)
- Voltages on top row, currents on bottom row

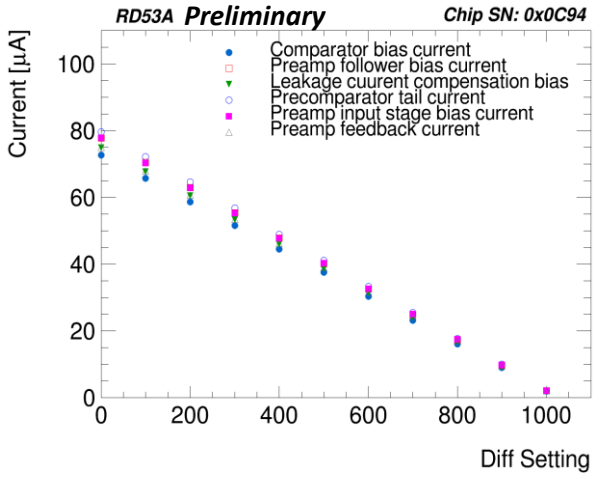












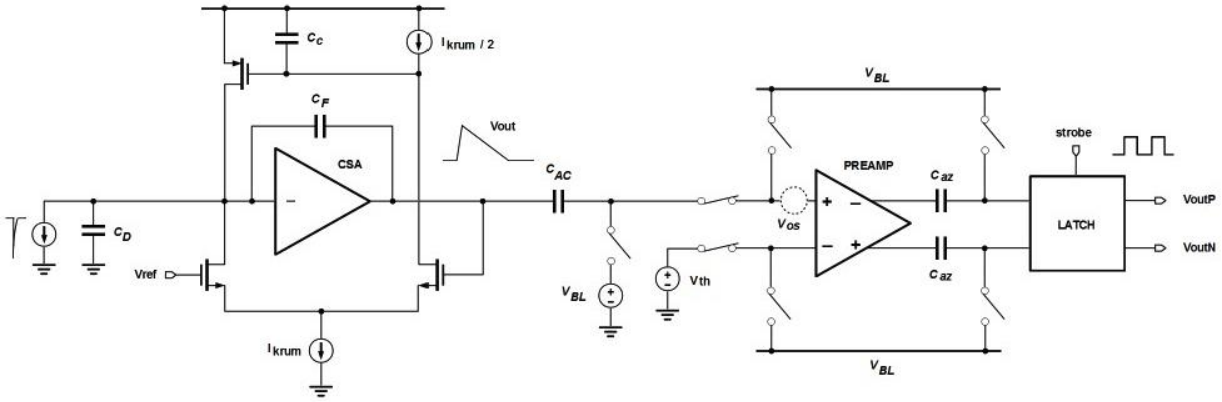
Analog Front-Ends

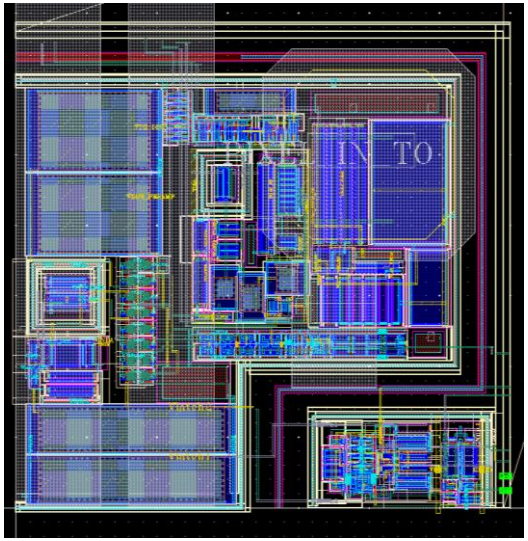
AFEs main features

	Synch AFE	Lin AFE	Diff AFE*	spec
Charge sensitivity [mV/ke]	43	25	103	-
ENC rms [e]	67	83	53	<<126
Threshold dispersion σ(Qth) rms [e]	93	32	20	<<126
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ [e]	115	89	54	≤126
In-time overdrive [e-]	≤ 50	≤ 100	0	≤ 600
Current consumption [μA/pixel]	3.3[1]	4.3	3.5	≤ 4
Time over threshold [ns]	121	99	118	< 133

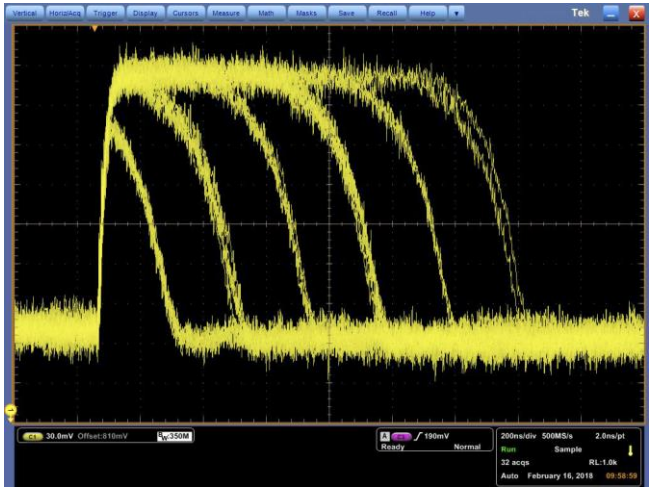
- Post-layout simulations (*except for the Diff AFE→ schematic level sim), CD=50 fF, T=27°C, Qth= 600 e-
- In-time overdrive→ relative to a Qin=30ke-
- Time walk → Qin=1200 e- (relative to a Qin=30ke-)
- ToT → Qin=6ke-
- [1] 5.1uA including the latch (digital domain)

Synchronous FE preliminary results

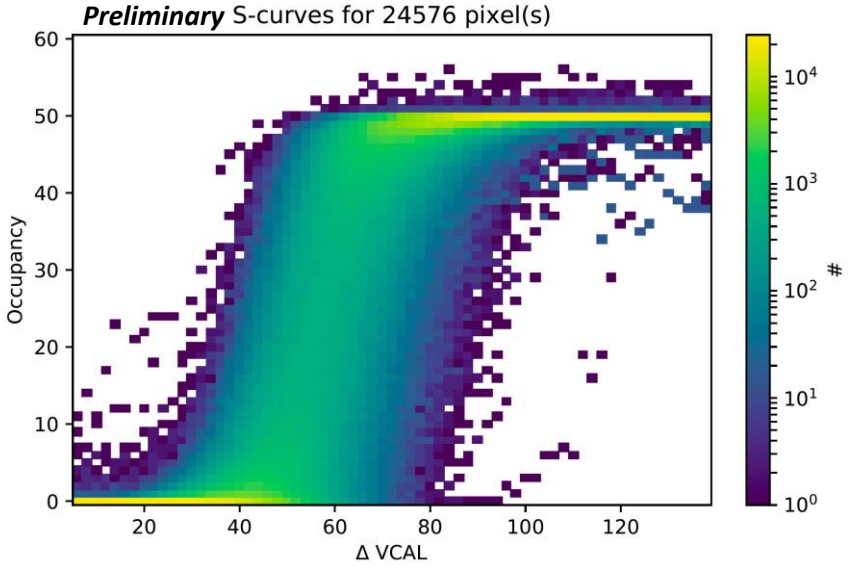


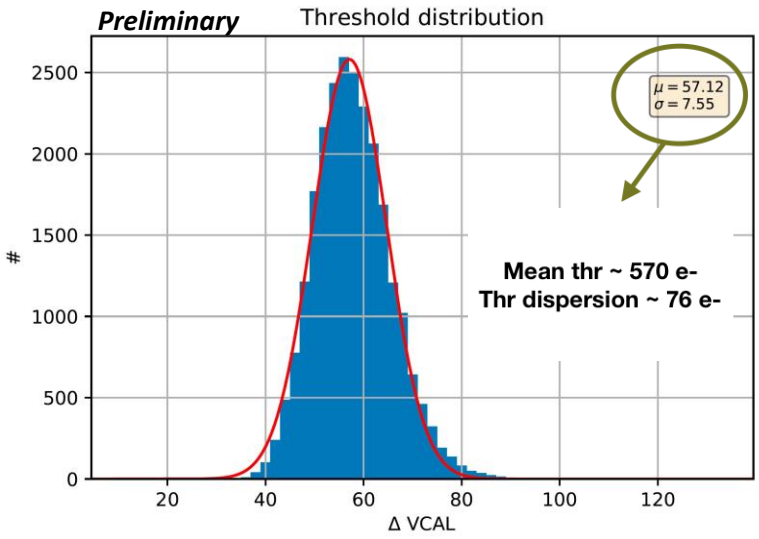


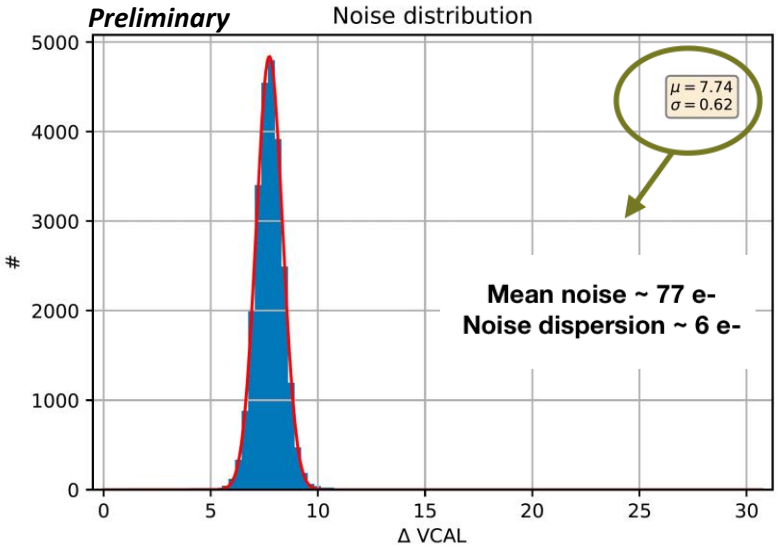
- Telescopic-cascoded CSA with Krummenacher feedback for linear ToT charge encoding
- Synchronous hit discriminator with track-and-latch comparator
- Threshold trimming using the auto-zeroing technique (no local trim DAC)
- ToT counting using 40 MHz clock or fast counting using latch as local oscillator (100-900 MHz)
- Efficient self-calibration can be performed according to online machine operations



Synchronous FE test results



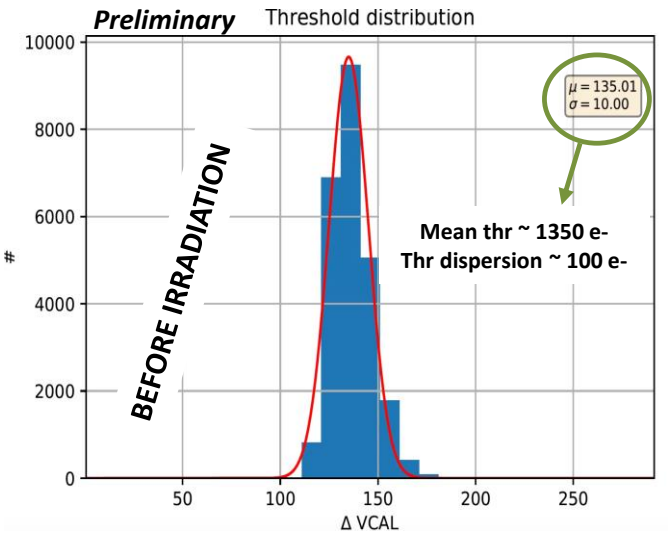


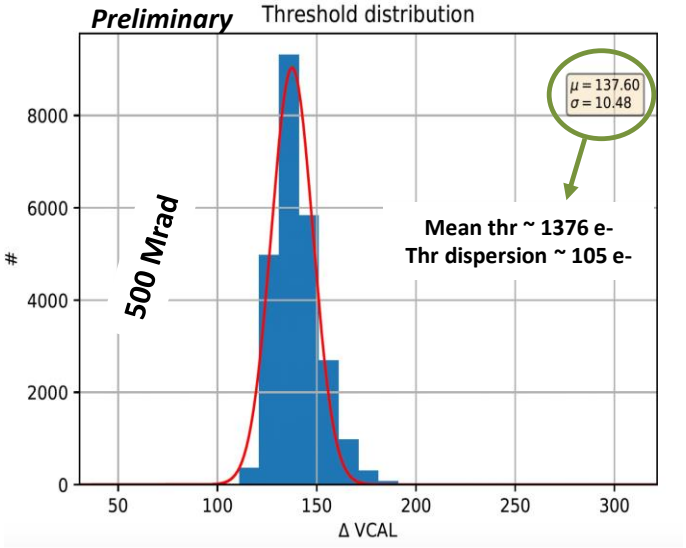


All these values are compliant with simulations

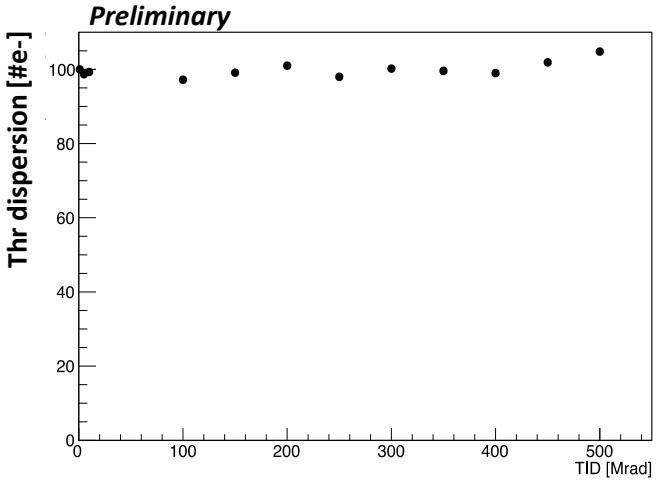
Synchronous FE irradiation test results

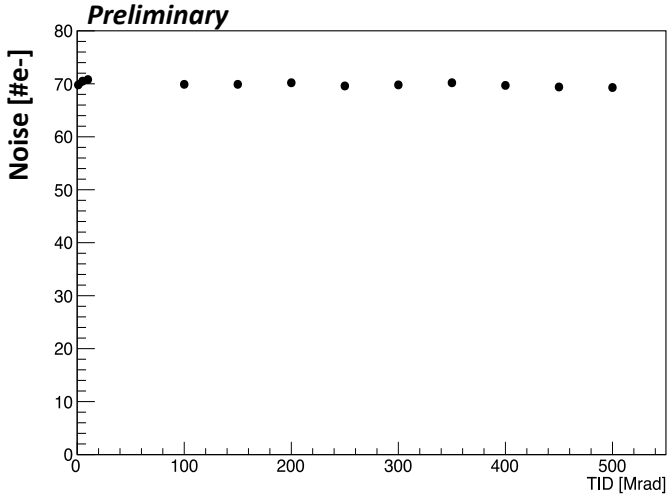
- An X-ray irradiation campaign has been performed at CERN in March
- Results shown here are for T= -10°C, up to 500 Mrad





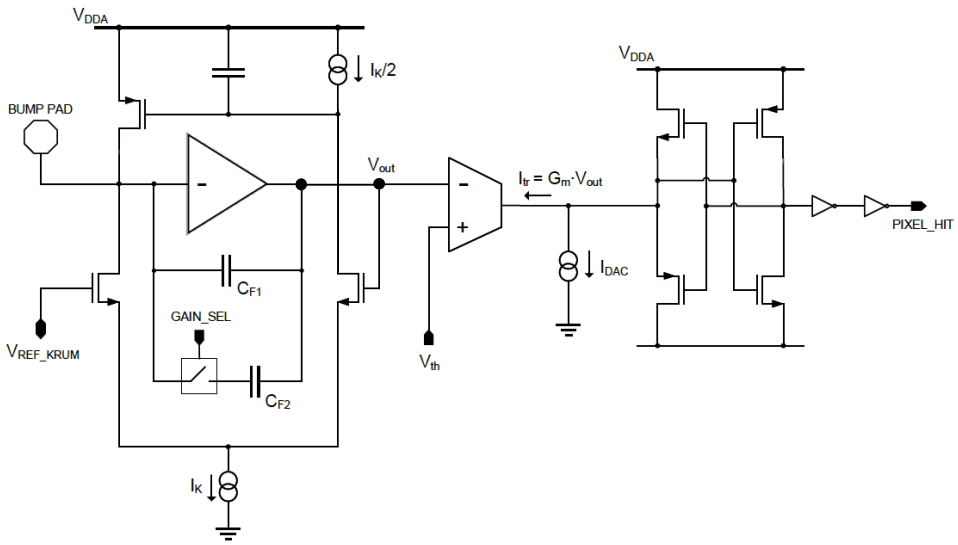
- ❑ **The threshold mean decreases of ~ 25 e-**
- ❑ **The thr. dispersion increases of ~ 5**

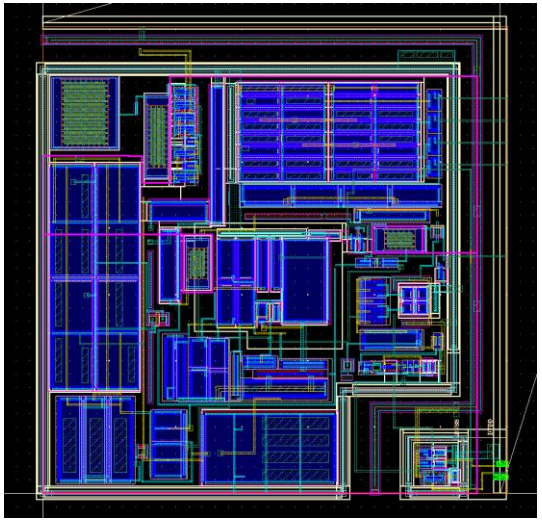




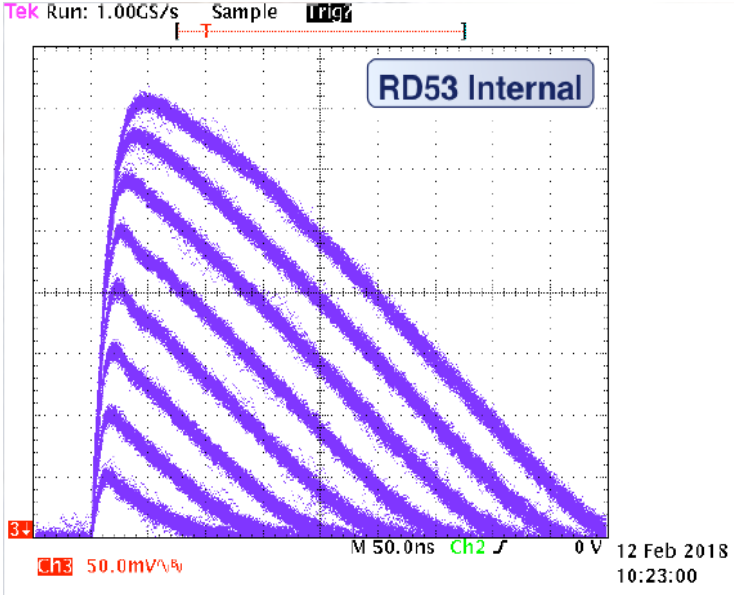
The behavior of the Sync FE is very slightly modified by radiation
Both threshold dispersion and noise do not show significant changes as a function of TID

Linear FE results

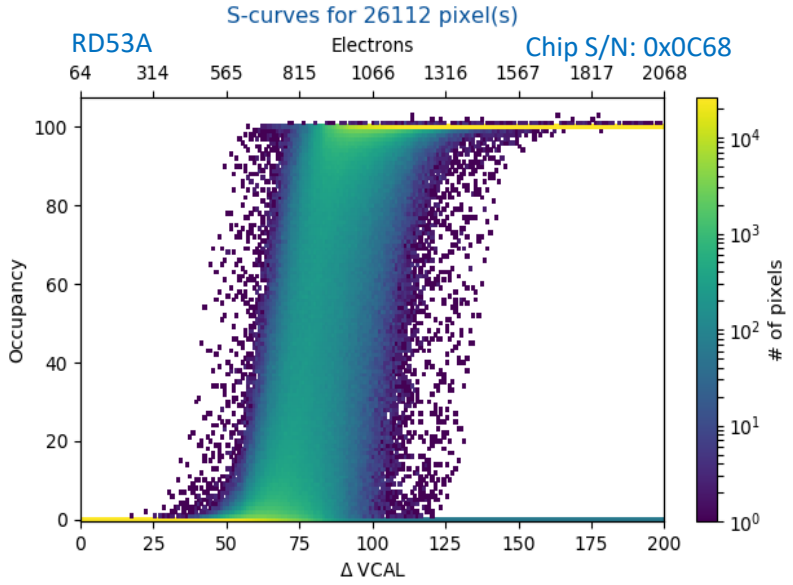


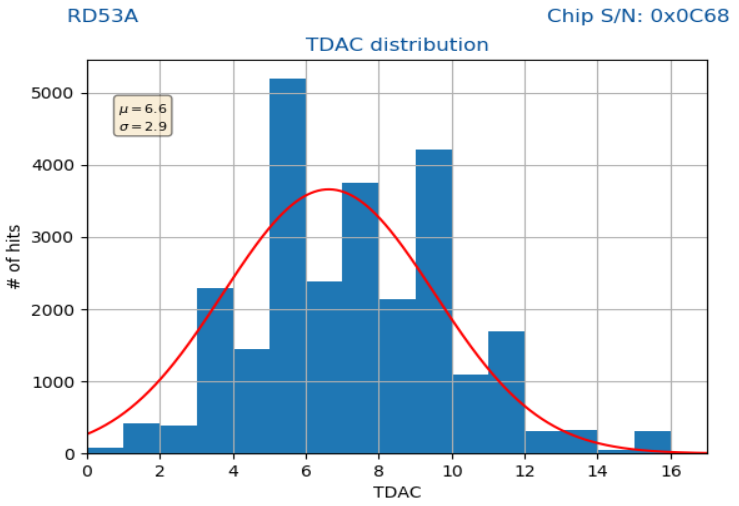


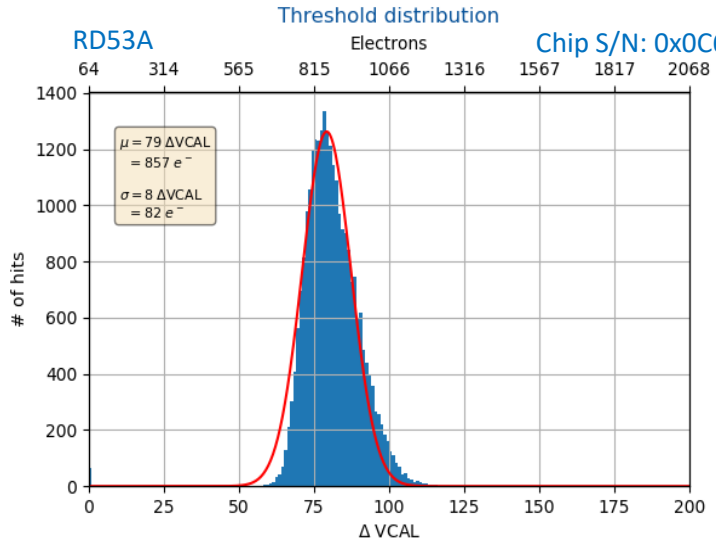
- **Single amplification stage** with **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- Asynchronous, low power **current comparator**
- **4 bit local DAC for threshold tuning**

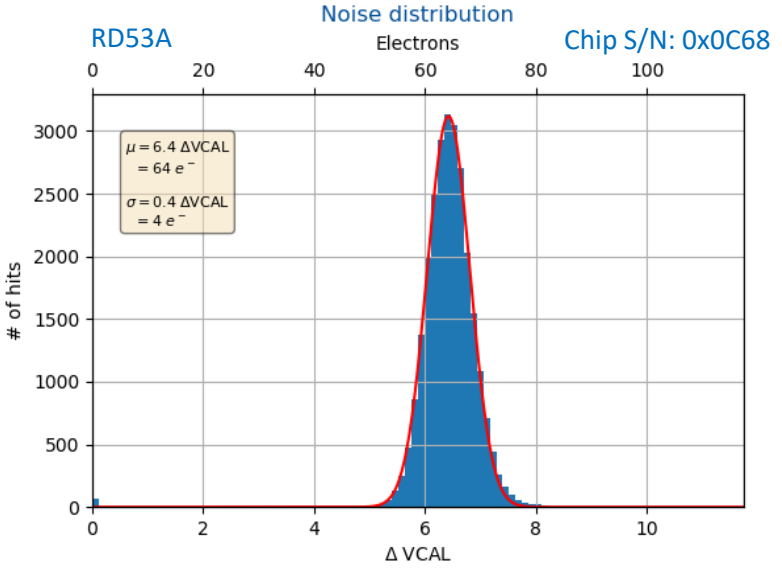


Linear FE (after noise-based tuning)





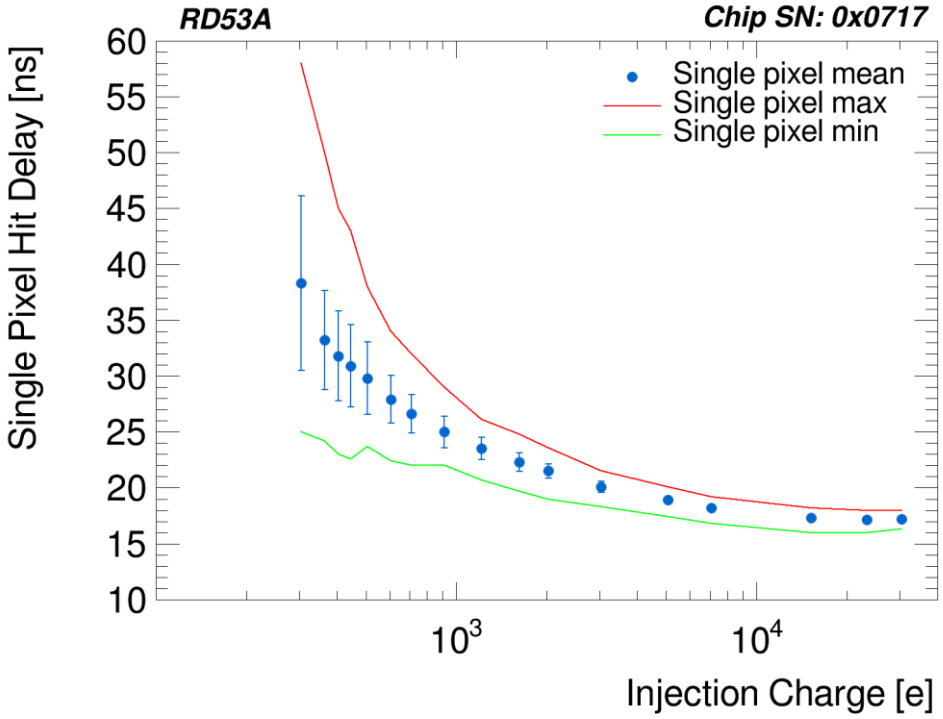




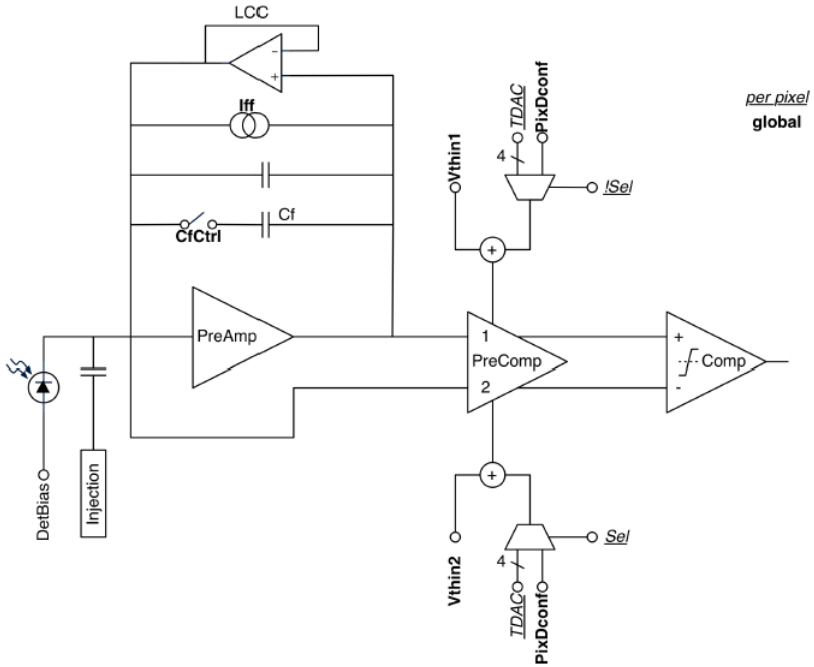
- Linear FE is fully functional
- Tuning procedure under optimization
- ENC ~ 64 e- rms

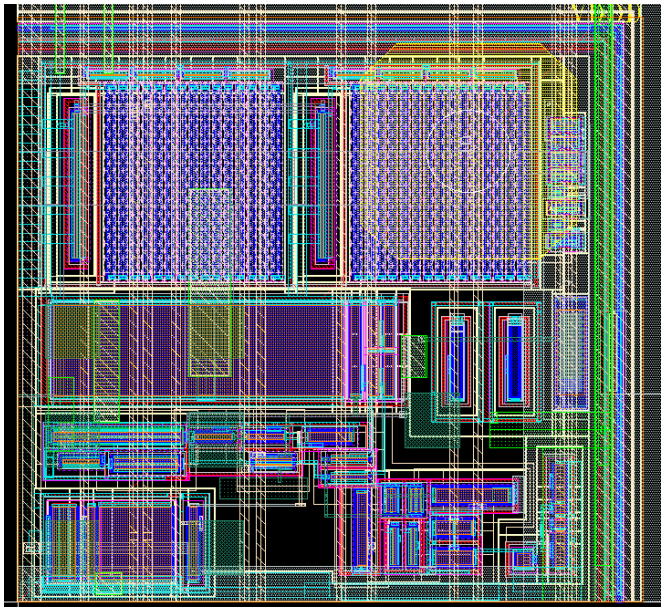
Time Walk of Linear FE

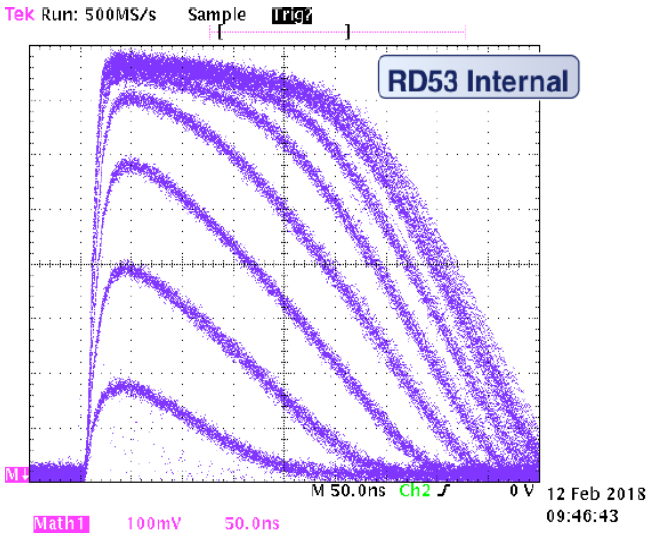
- Hit delay (timewalk) for one pixel in row 0 of the linear front end
- Delay is measured between the injection control signal (Cal_Edge) and the RD53A prompt hit output.
- The observed minimum delay of 17ns includes all internal chip signal propagation delays and scope probe delays, as well as the front end combined delay.
- Threshold for this single pixel ~ 300 e-



Differential FE





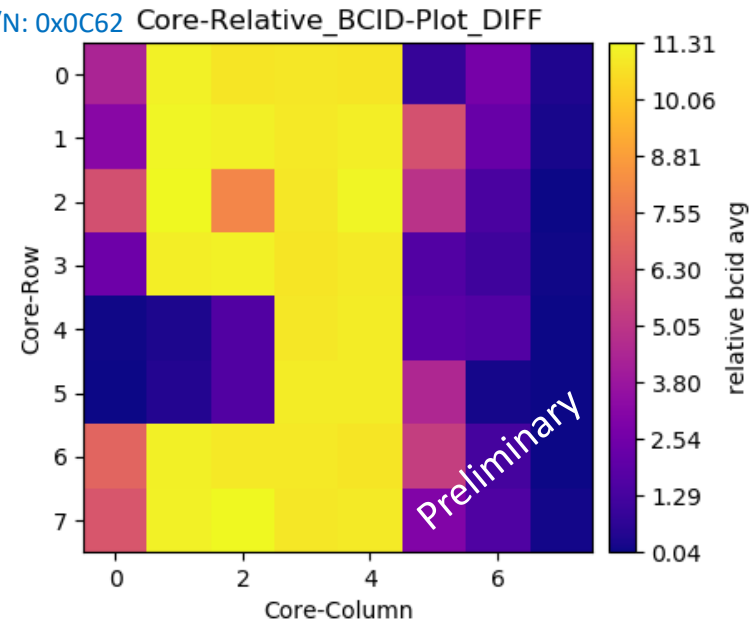


- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation**
- **4+1 bit local DAC for threshold tuning**

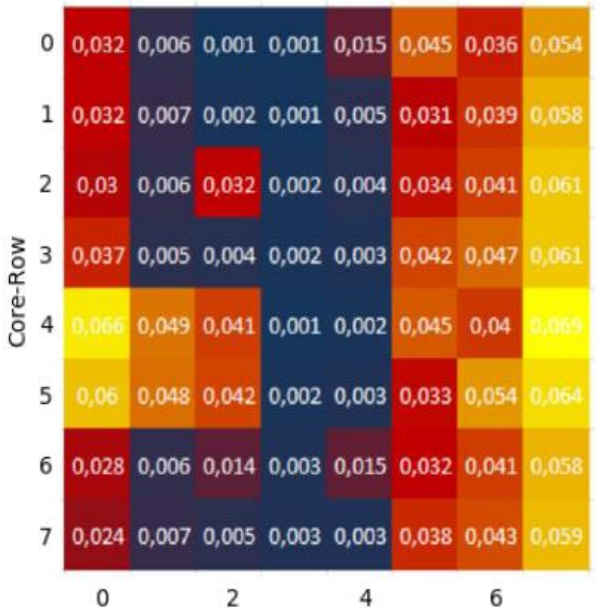
Differential FE

- Bug in the A/D interface: missing P&R constraint on the Diff. FE hit output → Varying load capacitance on comparator output → systematic variation of delay and ToT
- Will improve A/D verification strategy for production chips

RD53A
Chip S/N: 0x0C62

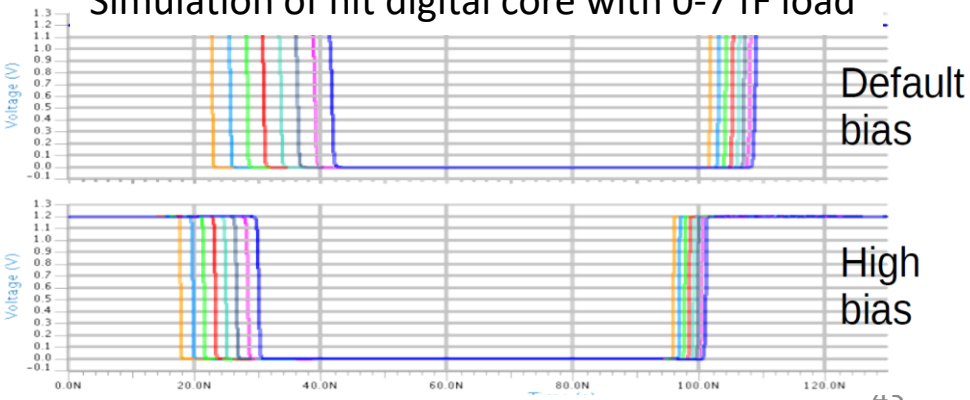


Extracted outdisc net load [pF]



- Partially recovered increasing comparator bias current and decreasing preamp discharge current
- **This bug does not prevent the Diff FE full characterization**

Simulation of hit digital core with 0-7 fF load

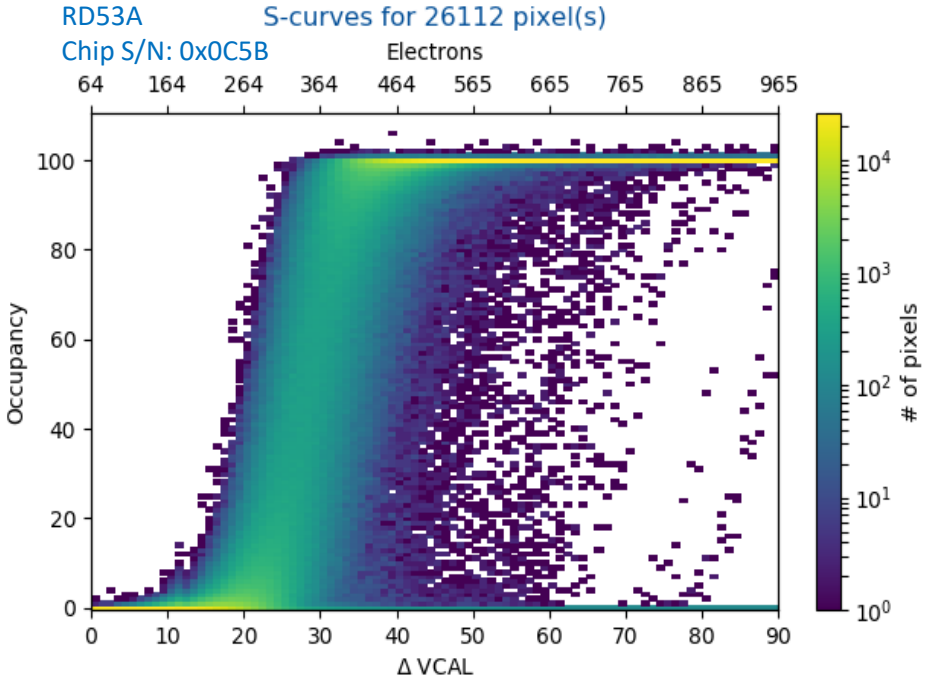


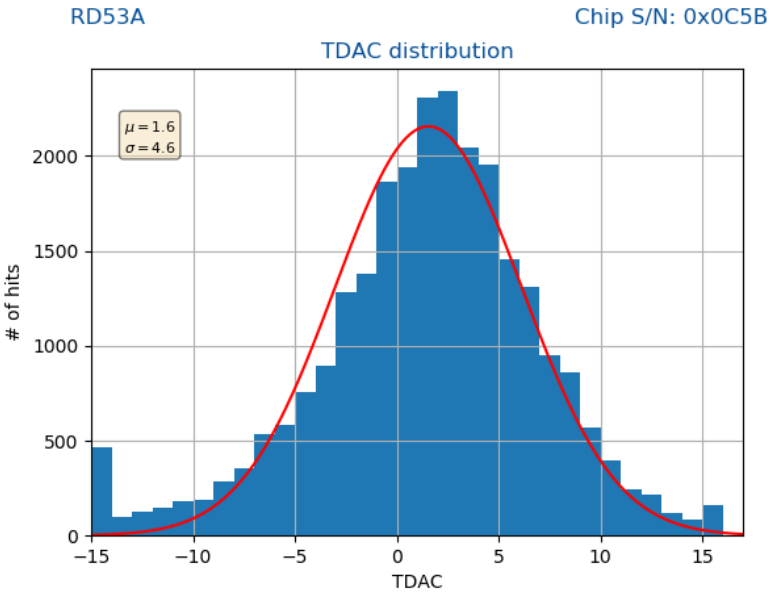
Differential FE (after noise-based tuning)

Non default parameters to minimize the effect of load capacitance:

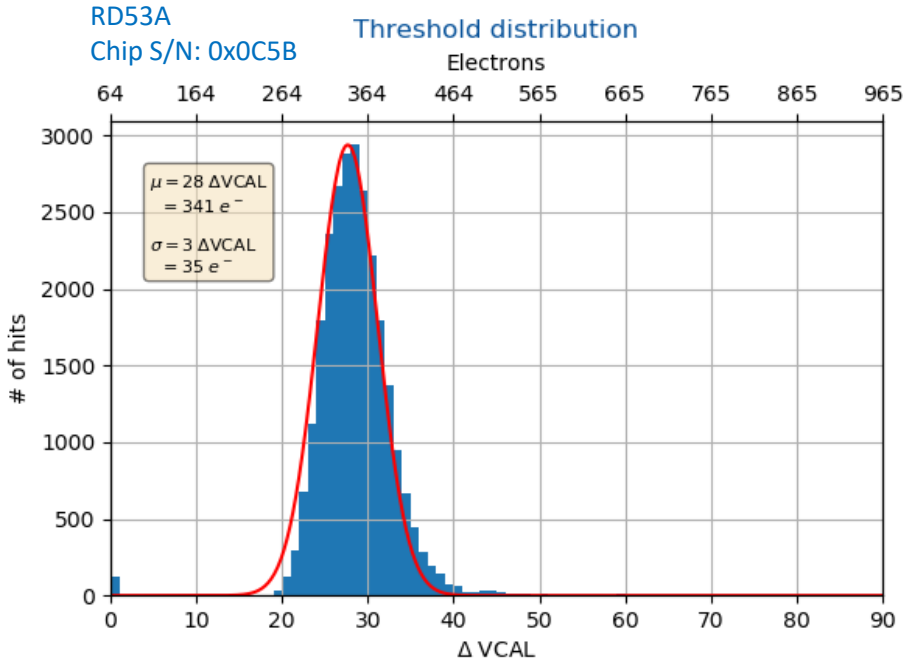
- Increased comparator current
- Decreased discharge preamp. current

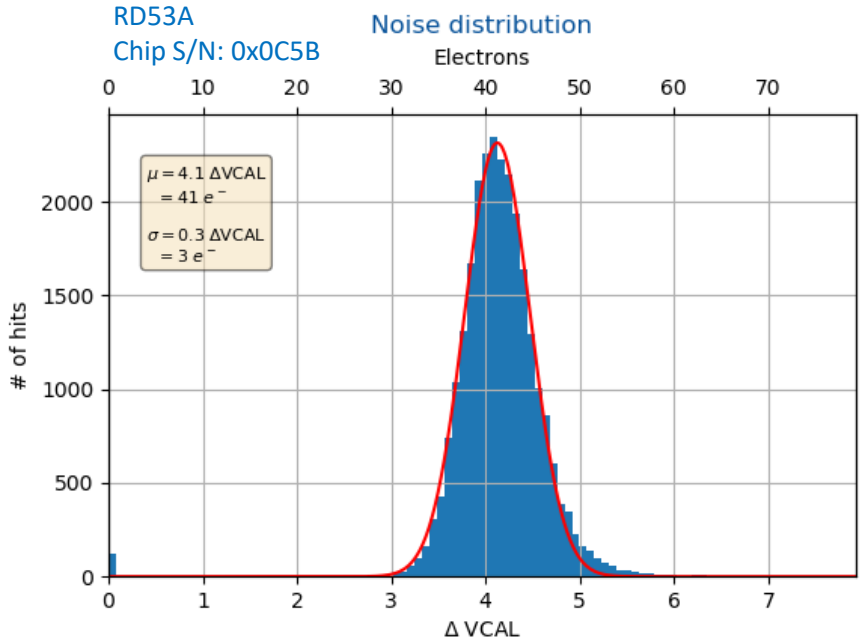
→(slower respect to nominal)





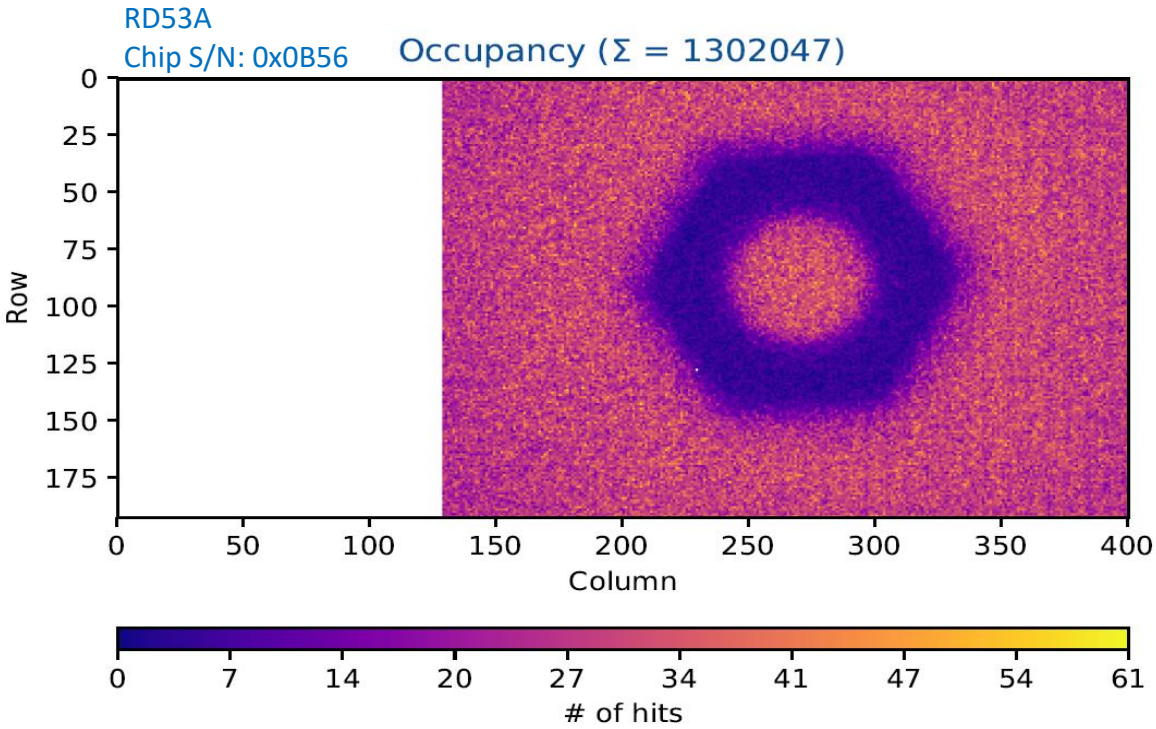
Differential FE (after noise-based tuning)





First signs of life of chip assembly

- 4 RD53A chips with sensor arrived in Bonn on 13 April 2018
- Image of a nut placed on the sensor backside, illuminated with Am241 source
- Hit-OR-trigger scan, LIN and DIFF FE, both set to 3 ke threshold, un-tuned
  - Need some more FW/SW development to implement auto-zero sequence for SYNC FE



Sensor ID W8S7: 50x50 µm, 150 µm , n-in-p planar (MPP)

ShuntLDO

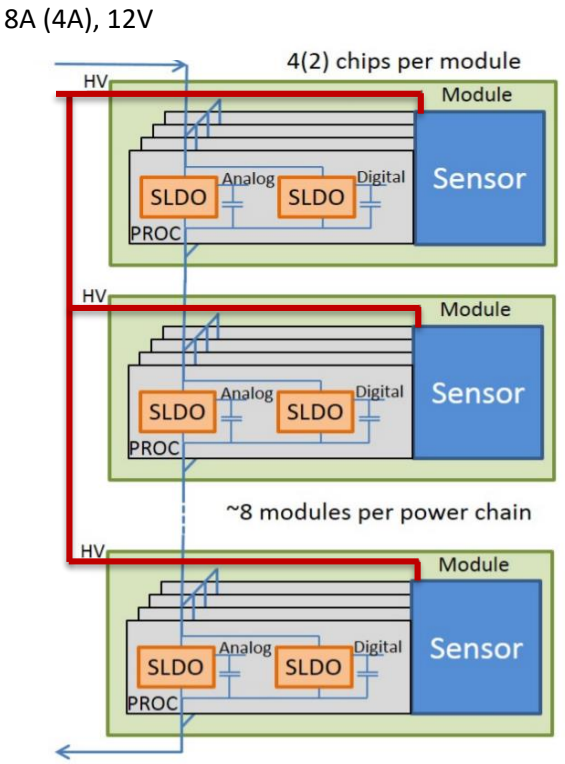
Thanks to:
Stella Orfanelli: dedicated talk at ACES 2018: https://indico.cern.ch/event/681247/timetable/?view=standard
Dominik Koukola: poster at ACES 2018: https://indico.cern.ch/event/681247/timetable/?view=standard

For an introduction to the Shunt-LDO circuitry see M.Karagounis paper:
https://indico.cern.ch/event/72160/attachments/1036621/1477145/Shunt-LDO_Regulator.pdf

Serial Powering Concept

Serial powering is the baseline choice for powering the ATLAS and CMS HL-LHC pixel detectors

- Pixel detector modules serially powered
- The power supply current (I_{in}) "re-used" among multiple loads connected in series
- Up to four chips per module powered in parallel
- Modules/ sensors grounds differ inside a chain
- Enough current injected in the power loop to satisfy the highest possible load current.
- Total current constant: **independent of the actual current in the load**



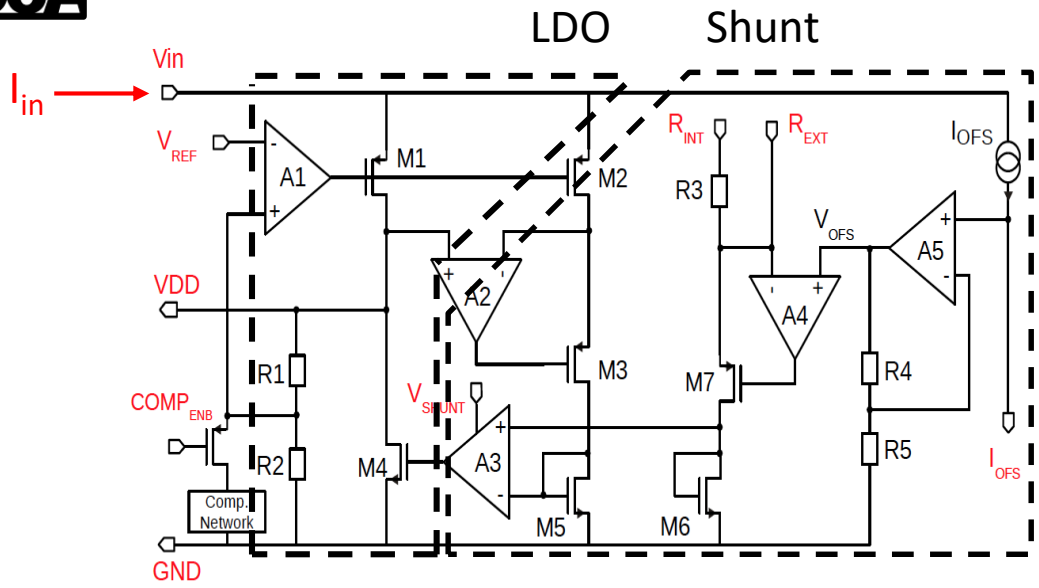
PROs

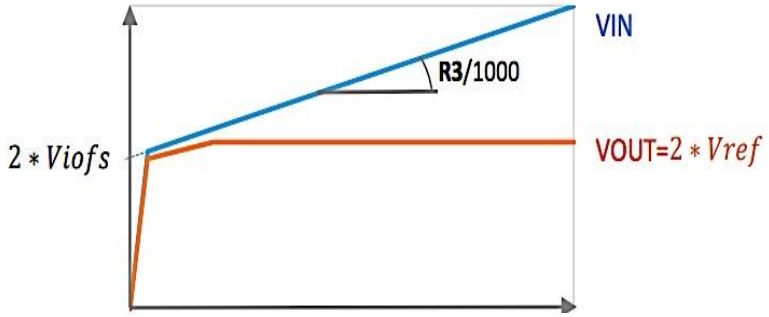
- ✓ **Low mass**
  - ✓ power cabling reduction ∝ length of chain
- ✓ **On-chip integrated solution**
- ✓ **Radiation hard**
- ✓ **Not sensitive to voltage drops**
  - ✓ Could reduce even more the cabling material budget

CONs

- ✓ Single failure could affect the full chain, if not properly taken into account during design

RD53A ShuntLDO regulator





$$VIN = 2 * Viofs + \frac{R3}{1000} * IIN$$

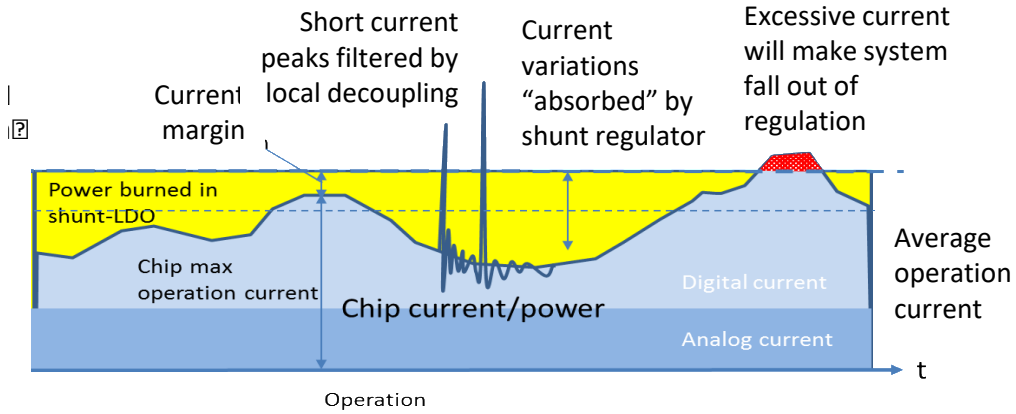
$$Viofs = 2\mu A * Riofs$$

Three operation modes:

1. ShuntLDO: constant input current I_{in} → local regulated VDD
2. LDO (Shunt is OFF) : external un-regulated voltage → local regulated VDD
3. External regulated VDD (Shunt-LDO bypassed)

ShuntLDO mode:

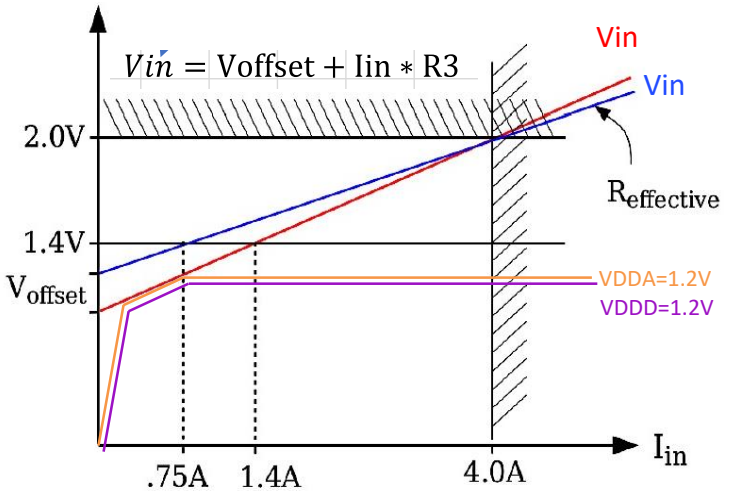
- Power consumption variations inside chip not "visible" from outside
- Shunt current dynamically regulated to keep chip current constant
- Dimensioned for production chips: **I_{in}= 2A**



ShuntLDO Resistive model

ShuntLDO makes power load look like resistor with voltage offset.

- Critical for appropriate current sharing between parallel chips and stable operation of serial powering

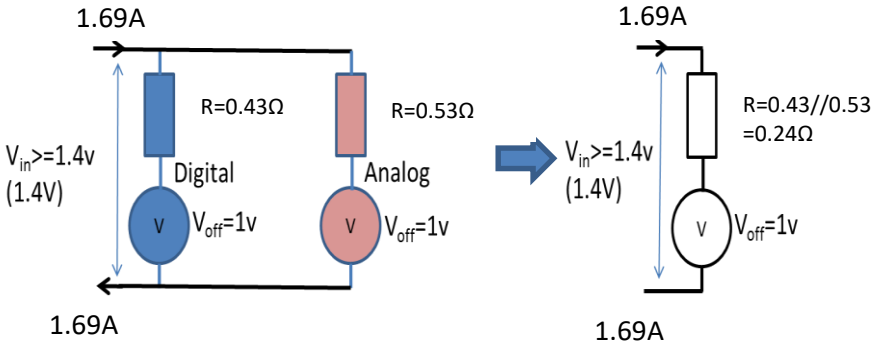


ShuntLDO parameters:

- Drop-out voltage ≥ 0.2V
- **Configurable resistive behavior** allows for well-defined current sharing, determined by their effective resistance
- **Configurable V_{offset}** (internal bandgap + external resistor), for an optimization of the power consumption
- **Configurable V_{ref}** (internal bandgap + trim bits)
- Extra headroom is user's choice (10%, 20%, etc.)
- **Off-chip decoupling capacitors** (uF) needed for LDO stability at the input and the output of the circuit

Nominal operation of full size chip (400x328 pixels):

- Drop-out voltage of ~0.2V => **Vin=1.4V**
- **V_{offset}=1V**
- Current headroom **~25%**
- R3 adapted such that Vin(4A/chip)=2.0V
  - R_{digi} = (1.4V – 1.0V) / (0.75A *125%) = 0.43Ω
  - R_{ana} = (1.4V – 1.0V) / (0.6A *125%) = 0.53Ω
  - Total chip Req = 0.24Ω

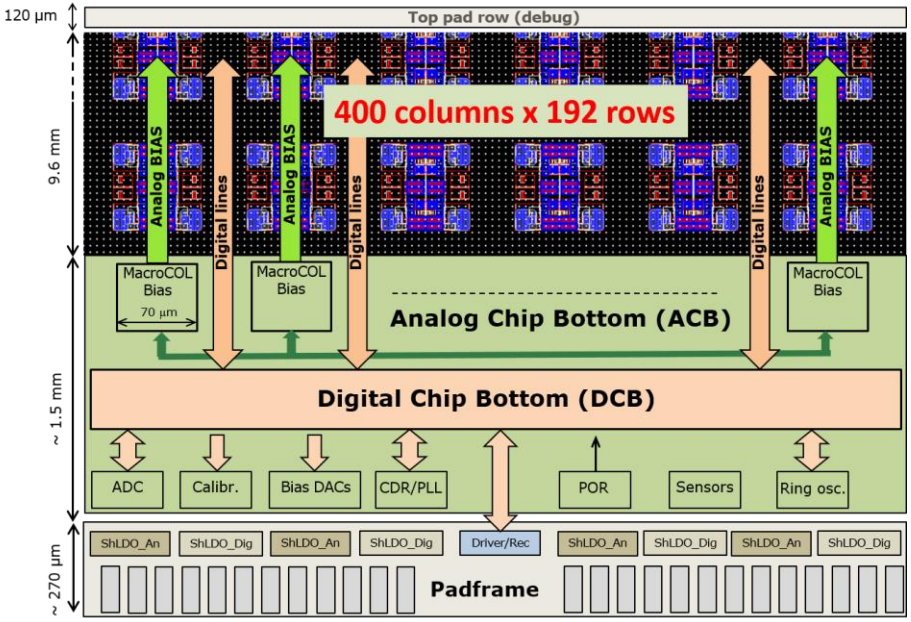


ShuntLDO integration

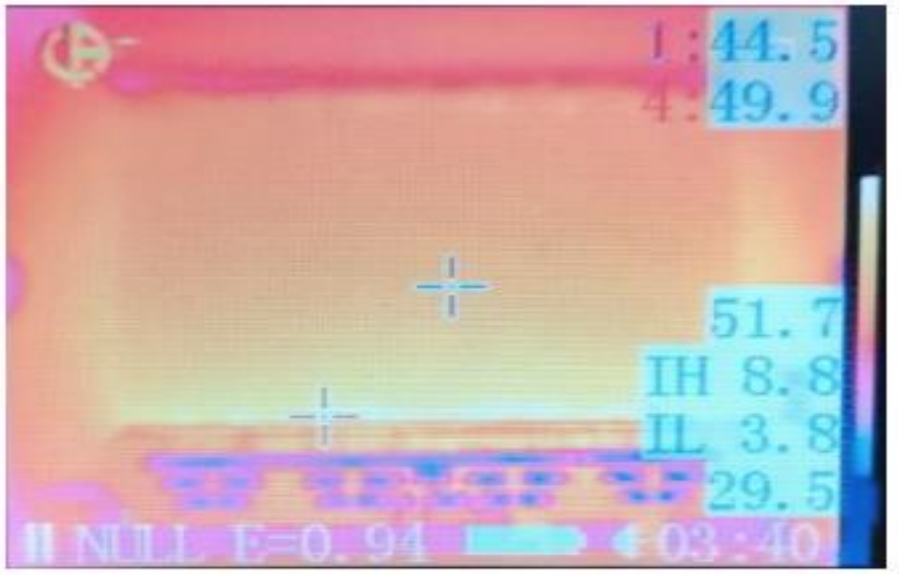
Two Shunt-LDO of 2.0 A (one per power domain) operating in parallel designed and integrated as in the final chip

- Almost 100% current margin could be burnt by the Shunts
- Split in 4*0.5A blocks for heat distribution and reliability

RD53A functional floorplan



Picture with thermal camera for Iin=2.0A, Vin =1.45V (2.9W)



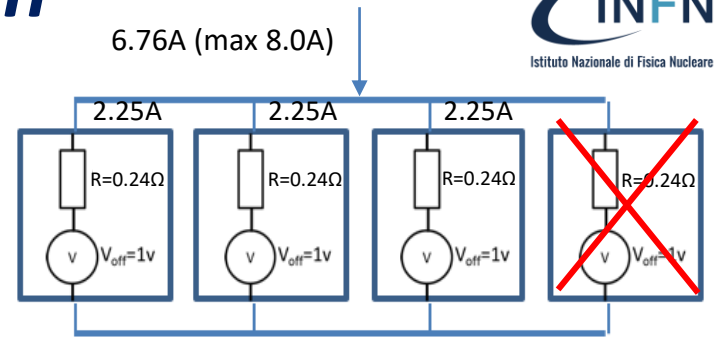
Failures & protection

Open circuit:

Collapse due to load or fast start-up

➔ current transients & power increase for remaining chips

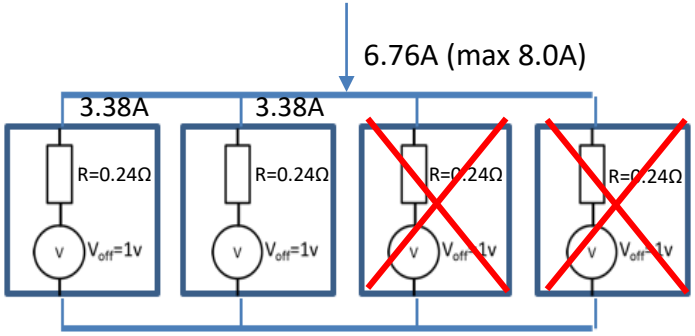
➔ over-voltage transients at Vin



45% power increase

Possible protection mechanisms:

- Voltage clamp to limit the input voltage for increased I_{in} (under study)
- **Operation with high offset voltage and low value of Req**
- Connect double-chip modules in parallel (if geometry permits)
- Use of PSPP chip (ATLAS) to bypass modules



150% power increase

Overload / Short circuit:

Physical short or over consumption due to failure/misconfiguration:

➔ shorted ShuntLDO takes most of the module current

➔ input voltage decreases (1.1V) but not fully collapsing

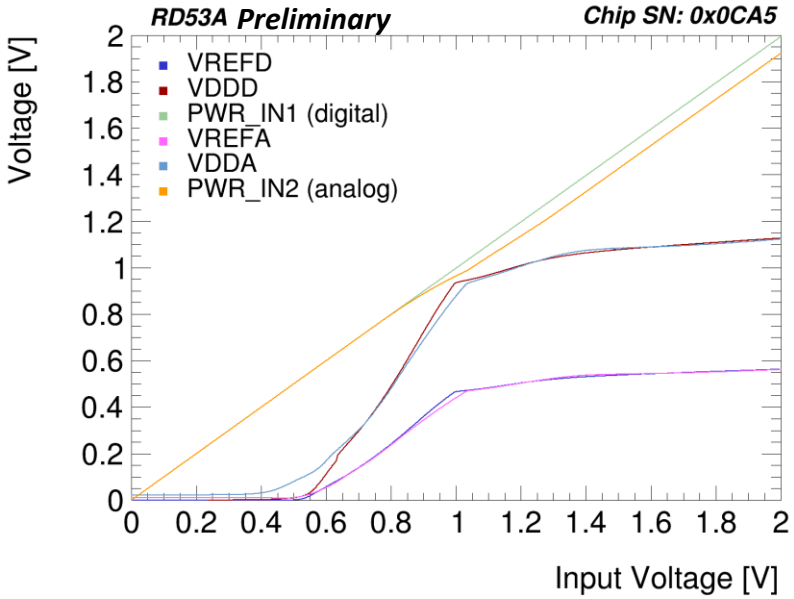
➔ rest of the chips underpowered

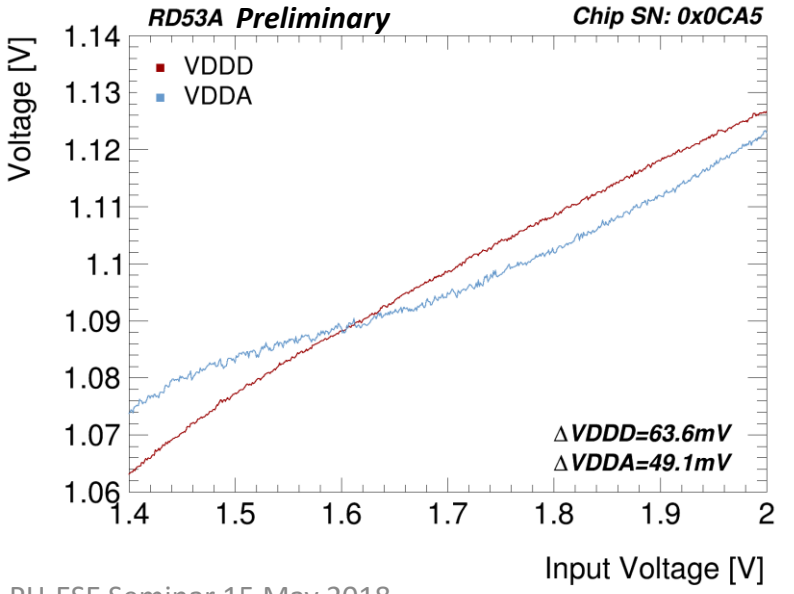
Possible protection mechanisms:

- Passive or active fuse
- Overcurrent protection (under study)
- Use of PSPP chip (ATLAS) to bypass modules

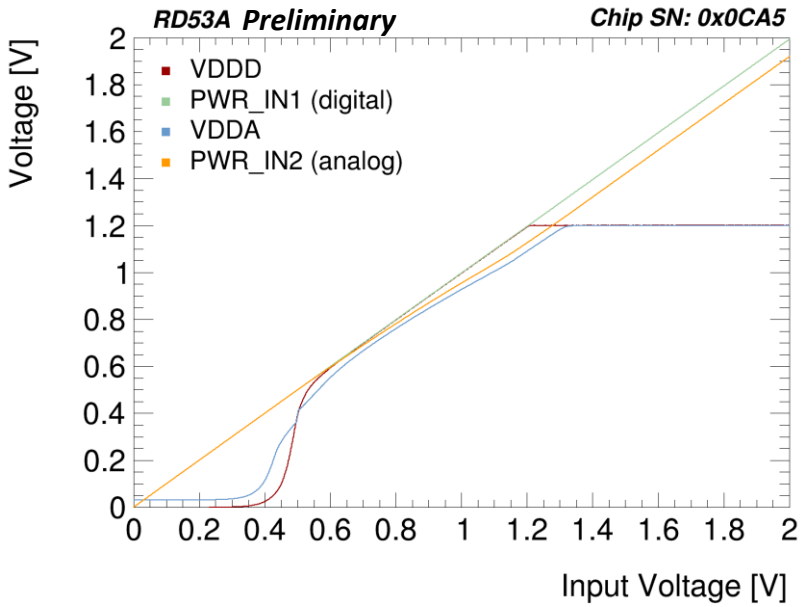
LDO mode - Line Regulation

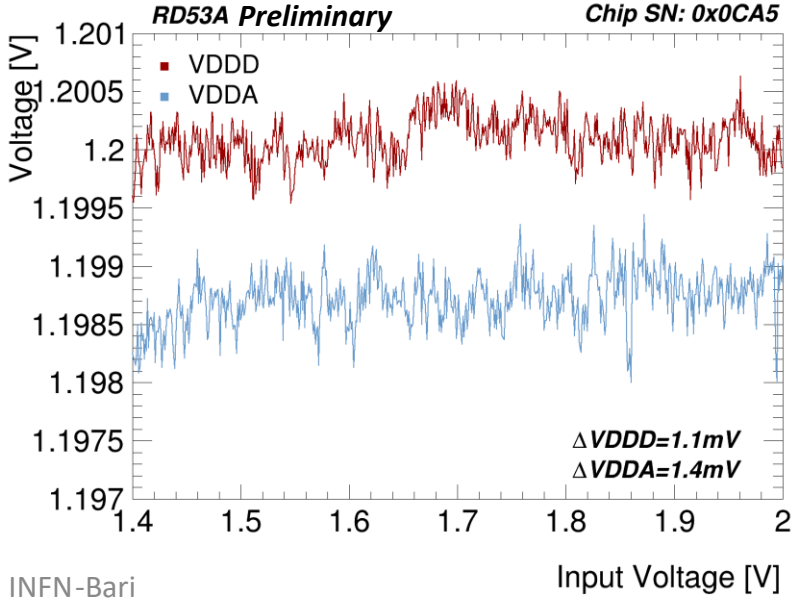
- Internal V_{ref} from BGR





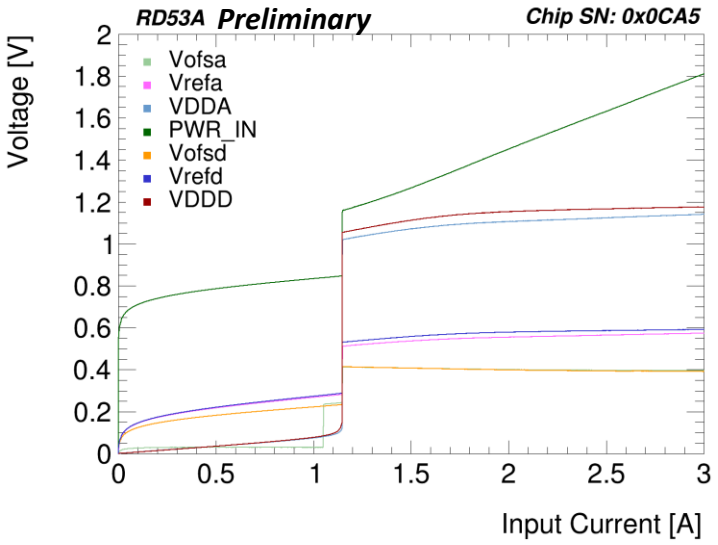
- External V_{ref} = 0.6 V

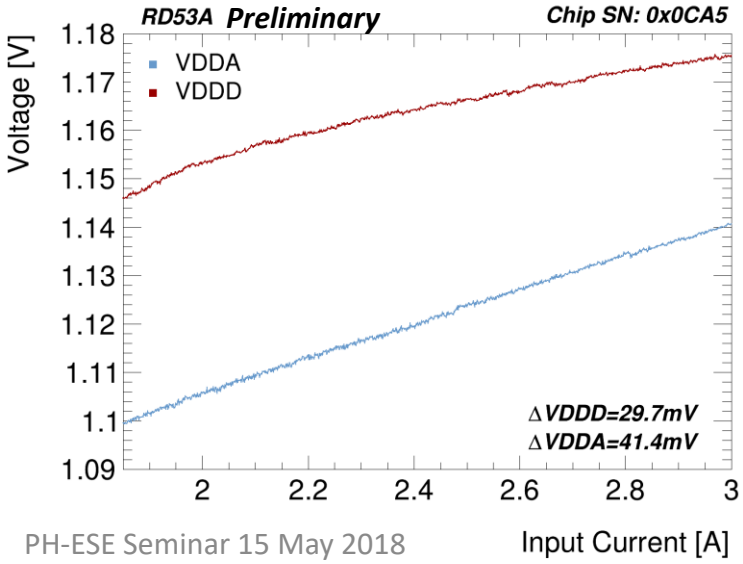




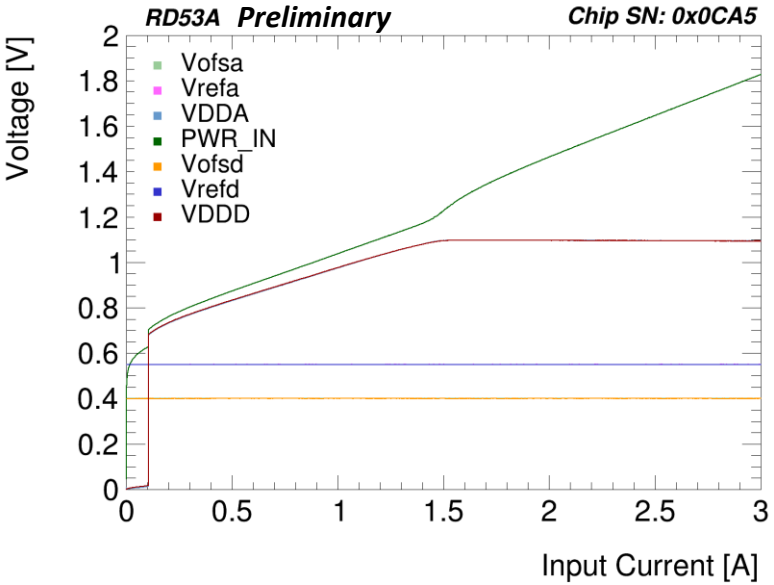
ShuntLDO - Line Regulation (parallel; Rint ~600 Ohm)

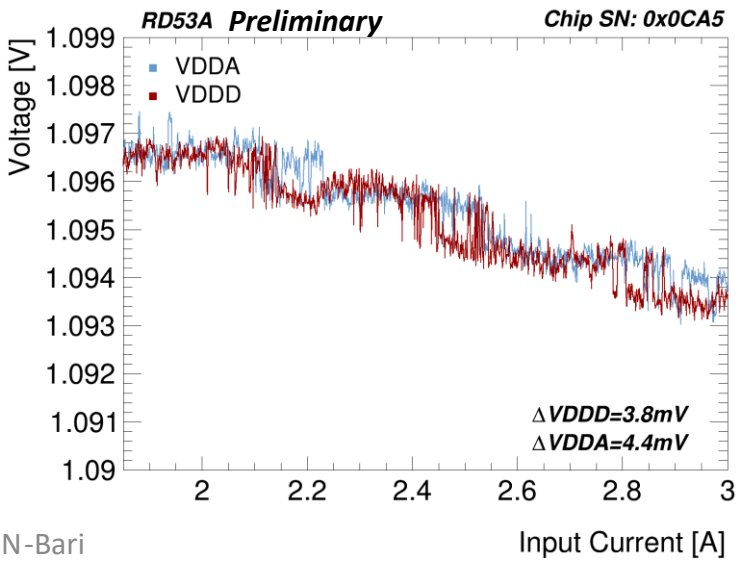
- Internal V_{ref}
- Internal V_{ofs}





- External V_{ref} = 0.55V
- External V_{ofs}= 0.4V → V_{offset} = 0.8V

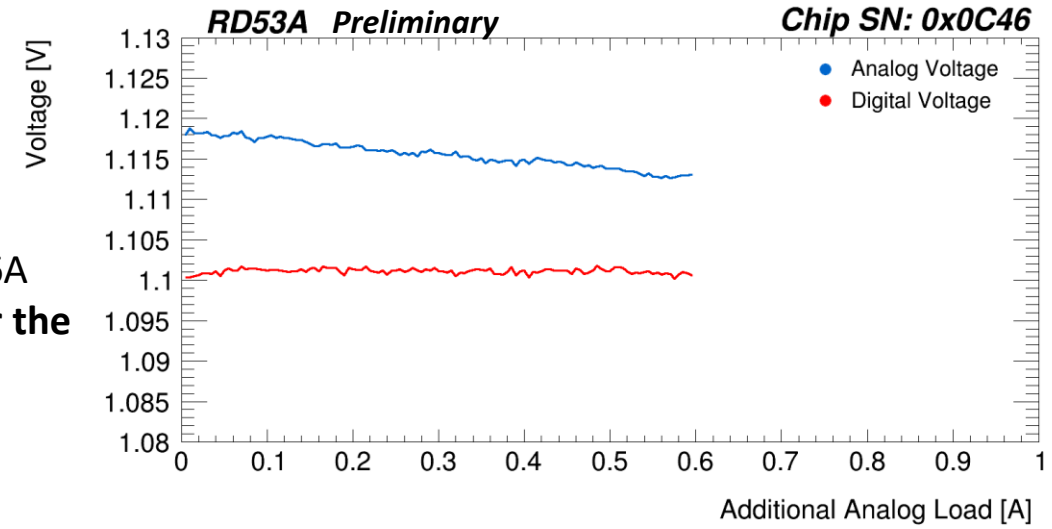




ShuntLDO - Load Regulation (parallel; Rint ~600 Ohm)

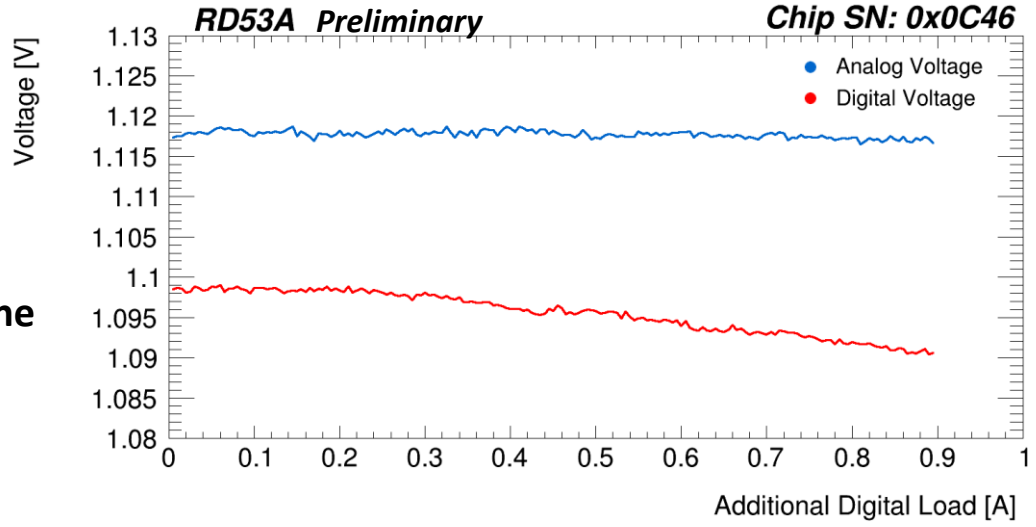
Load regulation of the analog ShuntLDO

- Drawing additional current from VDDA
- After power-up, $I_{Load} \sim$ 400mA
- Maximum additionally drawn load was 0.6A
- **The analog voltage (VDDA) decrease over the additional load is ~5mV/0.6A**



Load regulation of the digital ShuntLDO

- Drawing additional current from VDDD
- After power-up, $I_{Load} \sim$ 100mA (no clock)
- Maximum additionally drawn load was 0.9A
- **The digital voltage (VDDD) decrease over the additional load is ~8mV/0.9A**



Summary of ShuntLDO test results

- **The chip can be operated both in LDO and ShuntLDO mode**
- Line regulation behavior dominated by V_{REF} (Bandgap) as expected by simulations → to be improved in next version
- Load regulation is good
- Lots of measurements are still on-going:
  - Climatic chamber and radiation tests
  - Study impact of powering scheme to minimum threshold operation
  - Transient/Noise/Failure propagation studies
  - Decide on protection schemes, configurability, HV distribution
  - System tests using current source+ long cables and chains of pixel modules+prototypes structures
  - Study SP chains with 3D sensors
- New prototype submission in summer for:
  - New V_{ref}/V_{offset} scheme to improve the line regulation
  - Low-power mode for module testing without cooling (under study)
  - Output current limitation (under study)
  - Overvoltage protection (under study)
  - Improve monitoring capability

RD53B library development

RD53B library design activity started → ATLAS/CMS production chips

- Small prototype submission in summer for some blocks requiring major changes
- Choice of AFE (in autumn)
- Known features left out of RD53A but needed for prod. chips:
  - Bias of edge and top “long” pixels
  - Large pixels for outer layers (TBC)
  - 6 to 4 bit dual slope TOT mapping
  - 80 MHz TOT counting
  - Design for test scan chains
  - SEU hardening
  - Serial power regulator updates
  - ATLAS 2-level trigger scheme
  - Optimal data formatting and compression
  - Date aggregation between pixel chips (CMS)
  - Co-simulation/verification with LPGBT
  - Cable driver optimization/verification with final cables
  - …

Conclusions

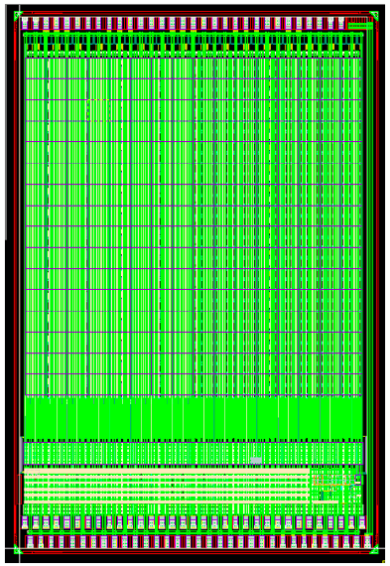
RD53A is fully functional and test results are very promising

- No major problems so far, but some “features” require proper Single Chip Card configuration and firmware/software optimizations
- First X-ray test at CERN done: some promising results but for next campaigns we are improving testing routines and setup
- New X-ray campaign on-going with un-biased chip to verify it survives during sensor rad test
- First production lot of 25 wafers submitted
- ATLAS/CMS plans to test different pixel sensors types (~10) and variants (2 - 4 for each type) with RD53A in the coming months
- Pixel modules (2x1 and 2x2) being designed with RD53A chip in both ATLAS and CMS pixel communities
- Large scale serial powering tests being planned with RD53A based pixel modules
- Design activity for production chips already started

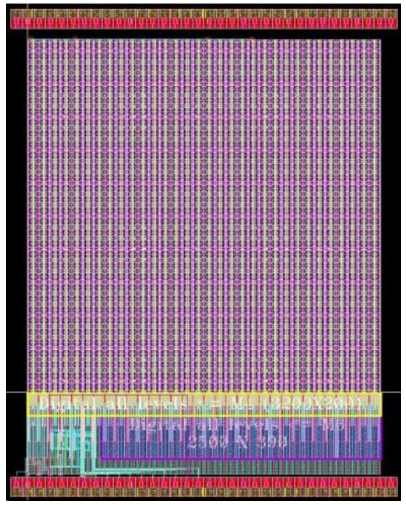
BACKUP

Small scale demonstrators

- **FE_SYNC** and **FE_LIN** included in the **CHIPIX65 demonstrator** (64x64) submitted at end of June 2016

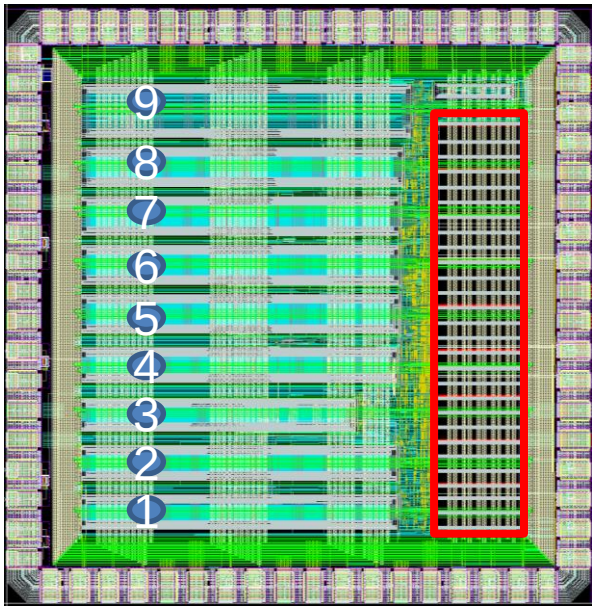


- **FE_DIFF** is included in the **FE65-P2 demonstrator** (64x64),

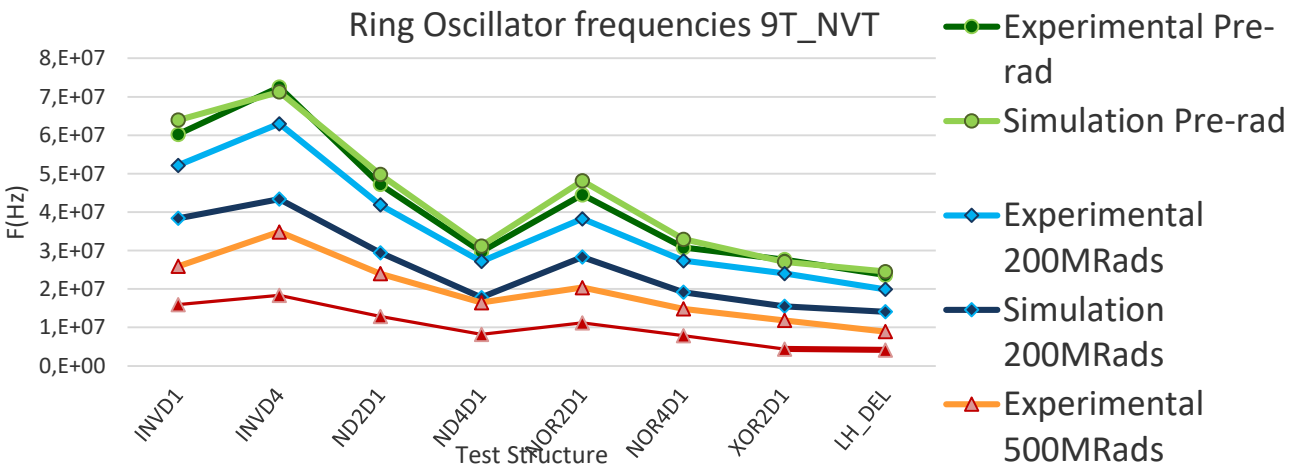


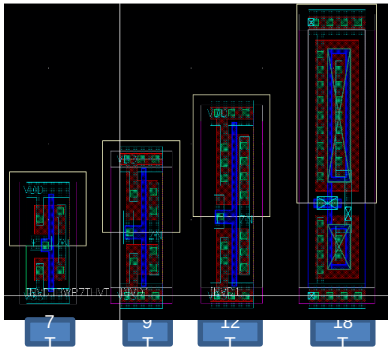
DRAD Chip : Test chip for digital design

- DRAD chip is designed at CERN :
- To study the effect of radiation on digital standard cells for the 65nm technology
- To test the efficiency and the validity of the digital simulations with the irradiation corner model
- Simulation results goes in the same direction than irradiation tests but the model overestimates the TID damage level
  - Models were done for worst case of biasing
- NOR gates should be avoided since show a strong degradation



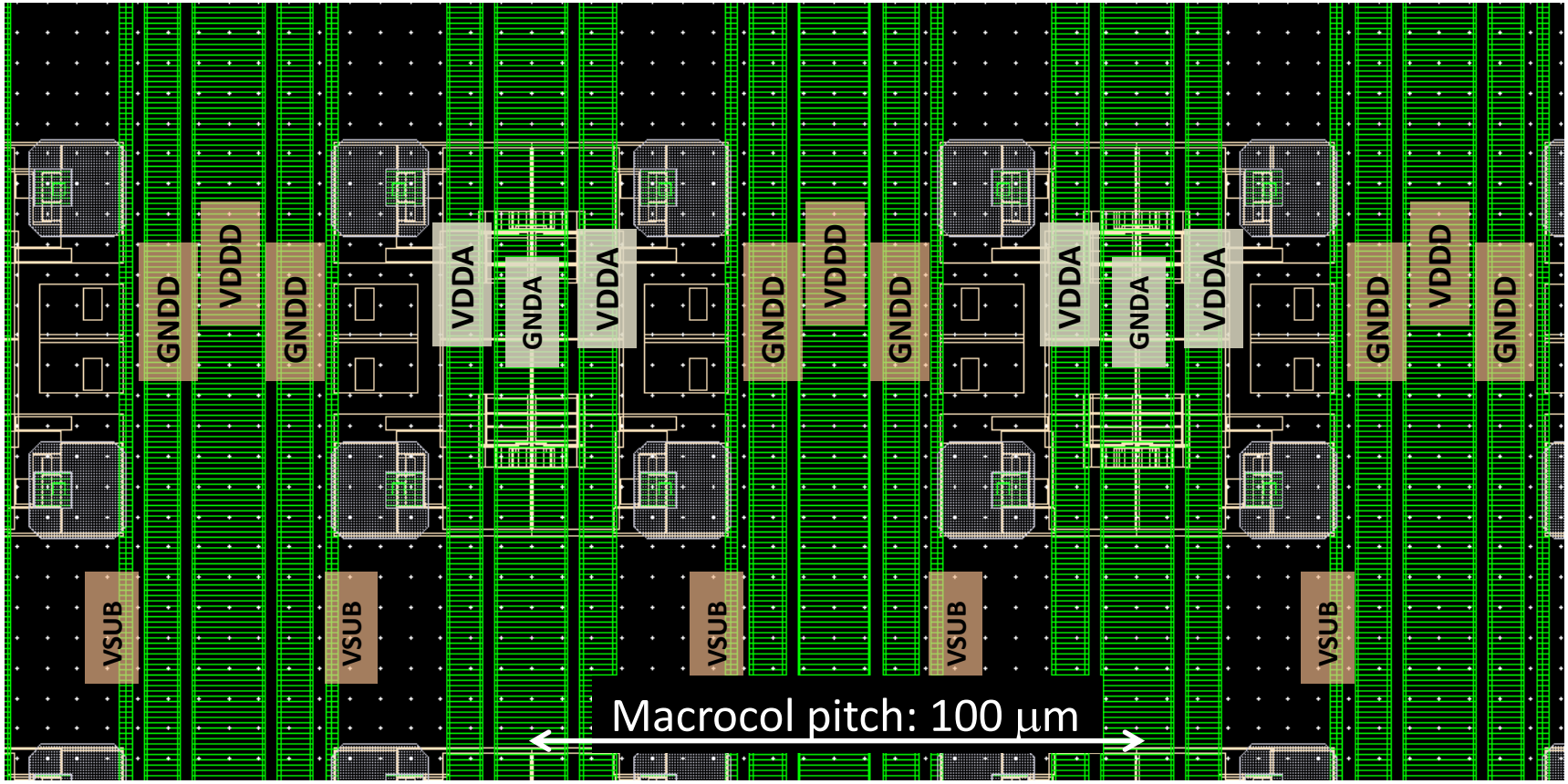
ANNEALING NOT INCLUDED IN THE MODELS





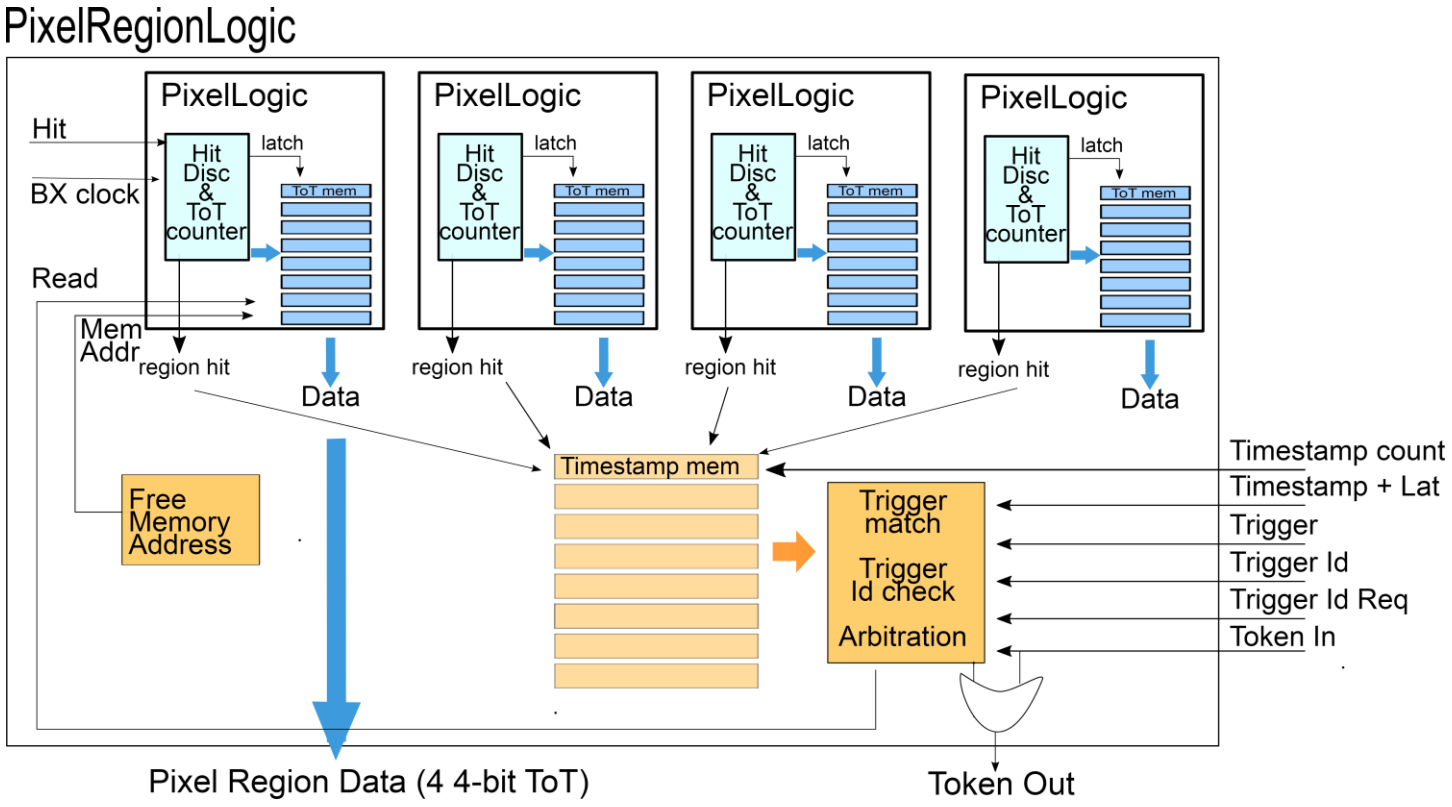
CELL HEIGHT
7 Track: 1.4 uM
9 Track: 1.8 uM
12 Track: 2.4 uM
18 Track: 3.6 uM

Array power distribution



- Power lines come (only) from chip bottom: use M8//M9//AP
- 1 quad = 2x2 pixels → 96 quads/macrocol → 384 pixels/macrocol
- Limited width for power busses:
  - ❑ 1 analog pair/ macrocol (VDDA, GNDA)
  - ❑ 1 digital pair/ macrocol (VDDD, GNDD)
  - ❑ 1 VSUB to bias the substrate (between the DNW regions)

Pixel region 1x4 in DBA



- 8 ToT memories (4-bit each) per pixel
- 8 shared latency timer (9 bit → up to 511 BX)

Pixel region 4x4 in CBA