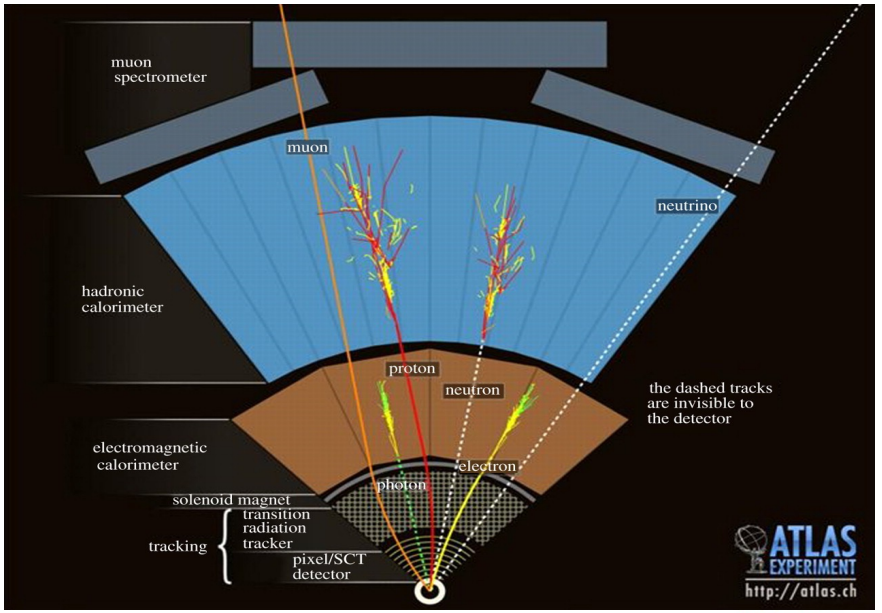
A PCI Express board proposed for the upgrade of the ATLAS TDAQ read-out system

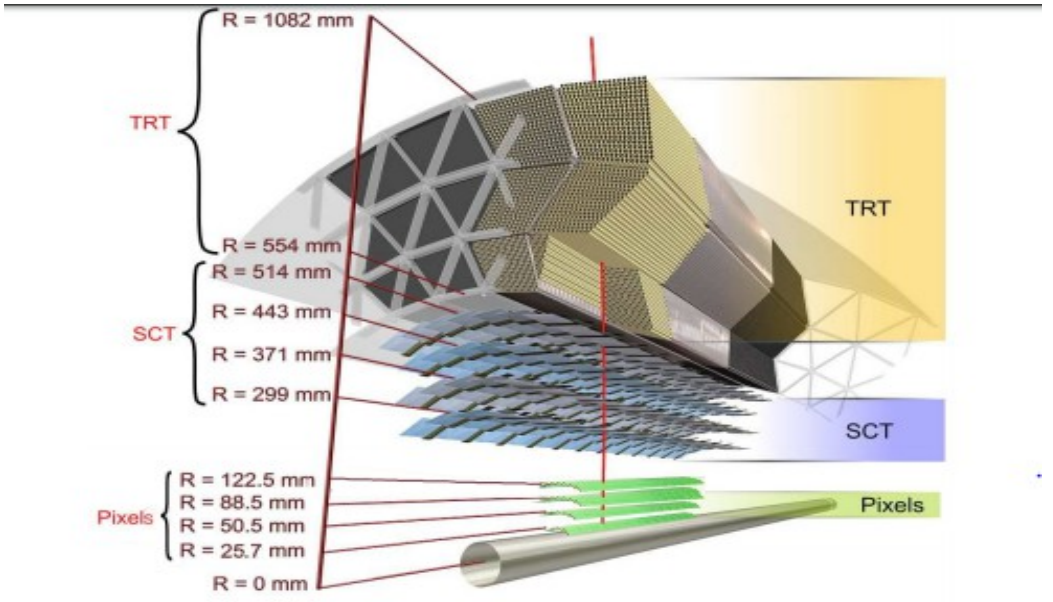
The ATLAS Experiment

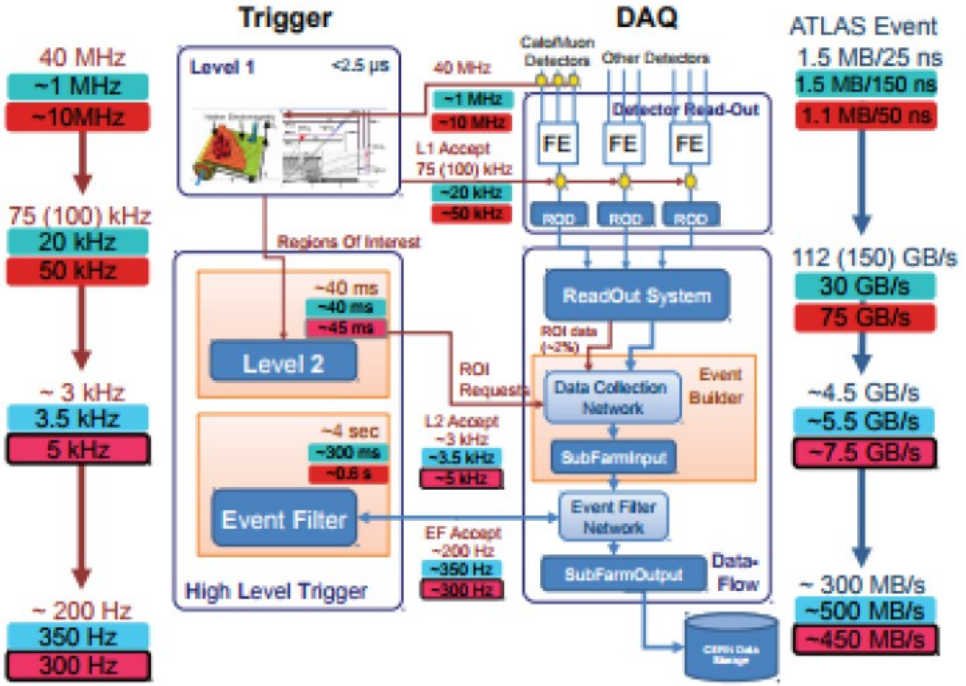
The importance of DAQ upgrade

Hardware proposed for the ATLAS Upgrade
(Hardware features)
(Low and High level control system)

The ATLAS Experiment

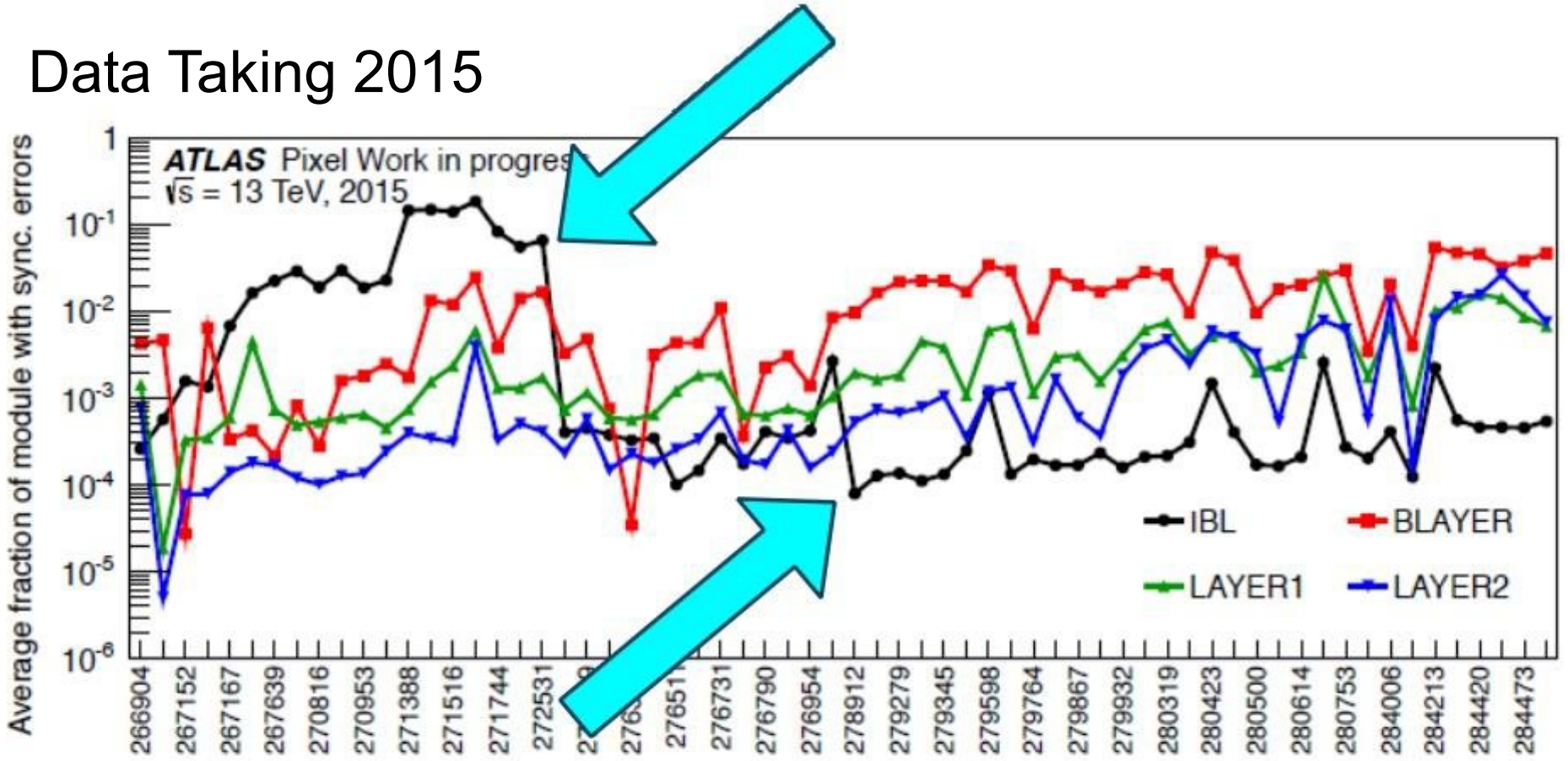






The Importance of Data Aquisition System Firmware

Data Taking 2015



The black plot show how the synchronization errors goes down after the firmware upgrade of the IBL's ROD. Now the sync errors are below the other ROD's layer that were not yet upgraded

Hardware proposal for the ATLAS upgrade (PILUP)

3 Flash Memories (2x16 MB, 1x128 MB), 3 Clock Generators (1 Phase-Locked Loop).

FMC CONNECTORS (400 PINS+4 TRANSCEIVERS (50 Gb/s),128+1(12,5 Gb/s), 128)

JTAG PROGRAMMER PORT MICRO-USB

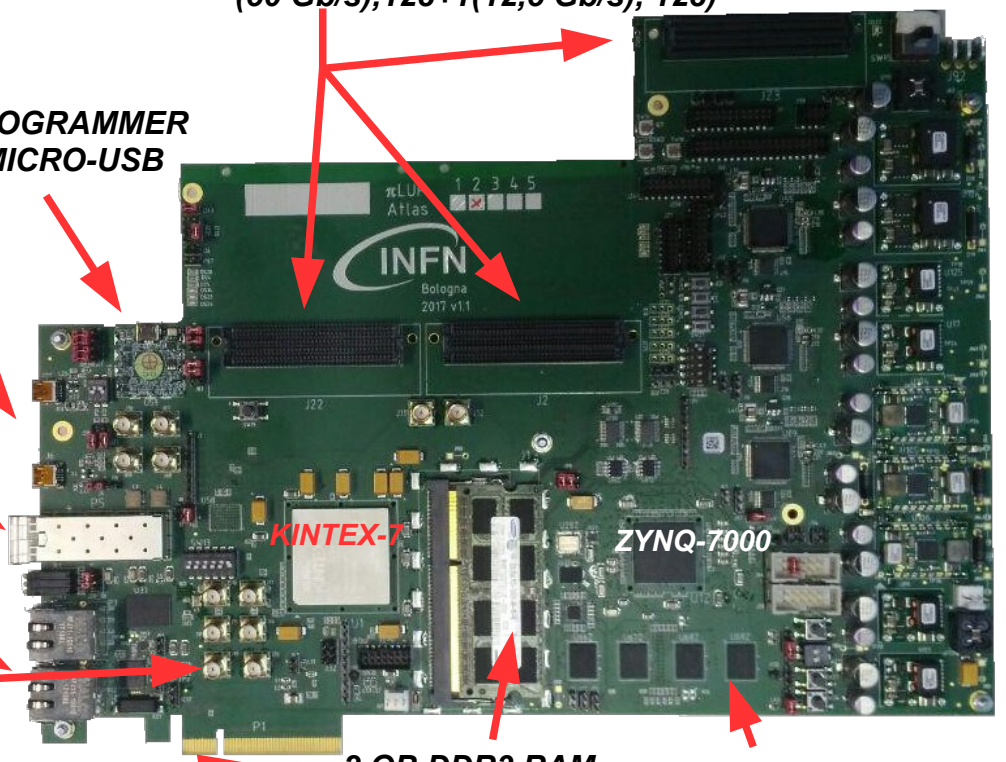
2xUART PORTS (115200 BR ZYNQ-7000, 9600 BR KINTEX-7)

SFP+ (10 Gb/s) OPTICAL FIBRES CONNECTORS

2xETHERNET PORTS (1 Gb/s ZYNQ-7000, 10 Gb/s KINTEX-7)

SMA CONNECTORS (12,5 Gb/s)

PCI Express Gen2 PORT (8 TRANSCEIVERS->100 Gb/s)



2 GB DDR3 RAM KINTEX-7

1 GB DDR3 RAM ZYNQ-7000

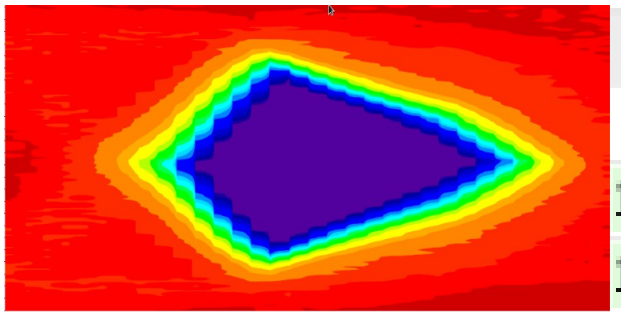
- **28 nm** FPGAs (xc7z020-1clg484c & xc7k352t-2ffg900c);

- **21 differential bus at 200 MHz DDR** between the FPGAs;

- **Zynq-7000**=>Master with an **ARM Cortex-A9 Dual-Core** processor;

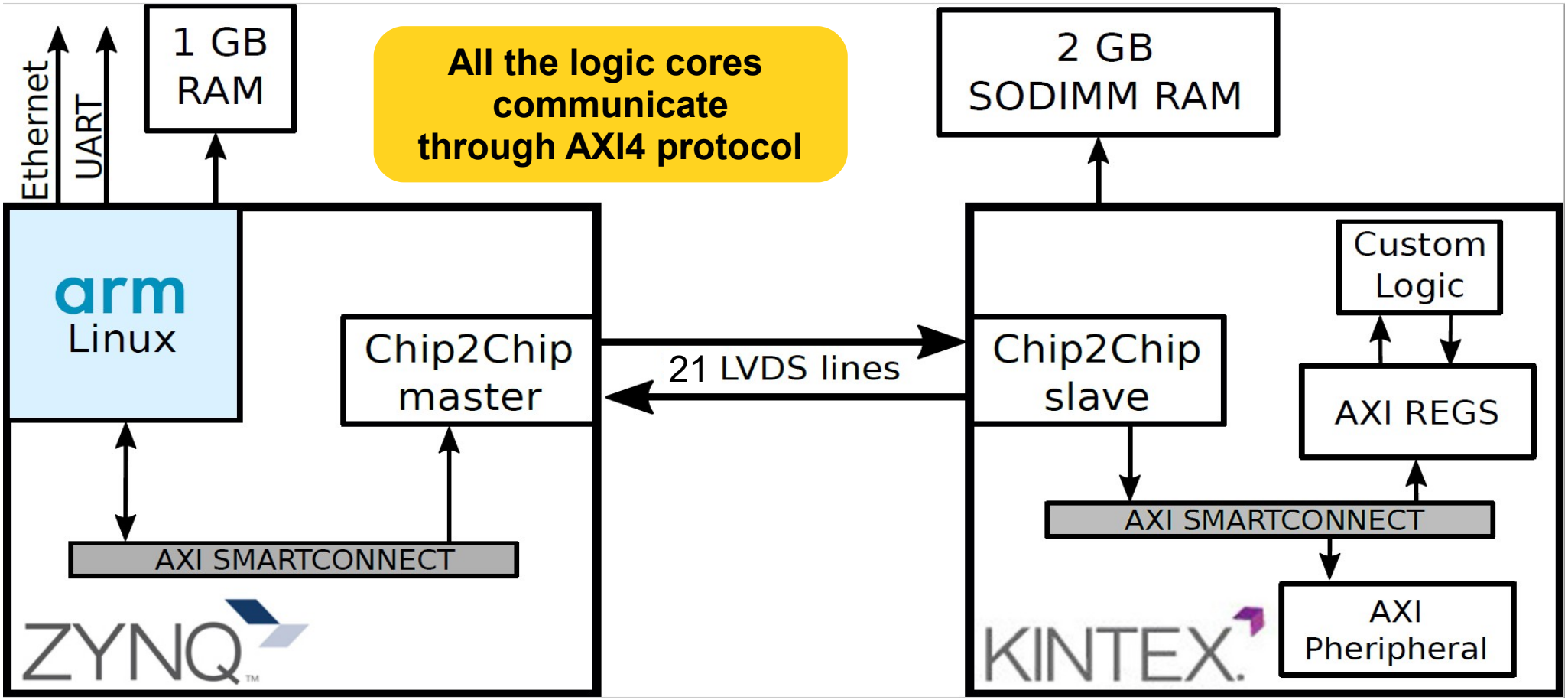
- **Kintex-7**=>Slave with **16 fast links transceivers up to 12,5 Gb/s.**

Bit Error Rate of the transceivers I/O (includes the PCI Express Gen2) down to 10^{-14} (10 hours of run)



Status	Bits	Errors	BER
10.000 Gbps	7.621E13	0E0	1.312E-14
10.000 Gbps	7.619E13	0E0	1.313E-14

Structure of the control system



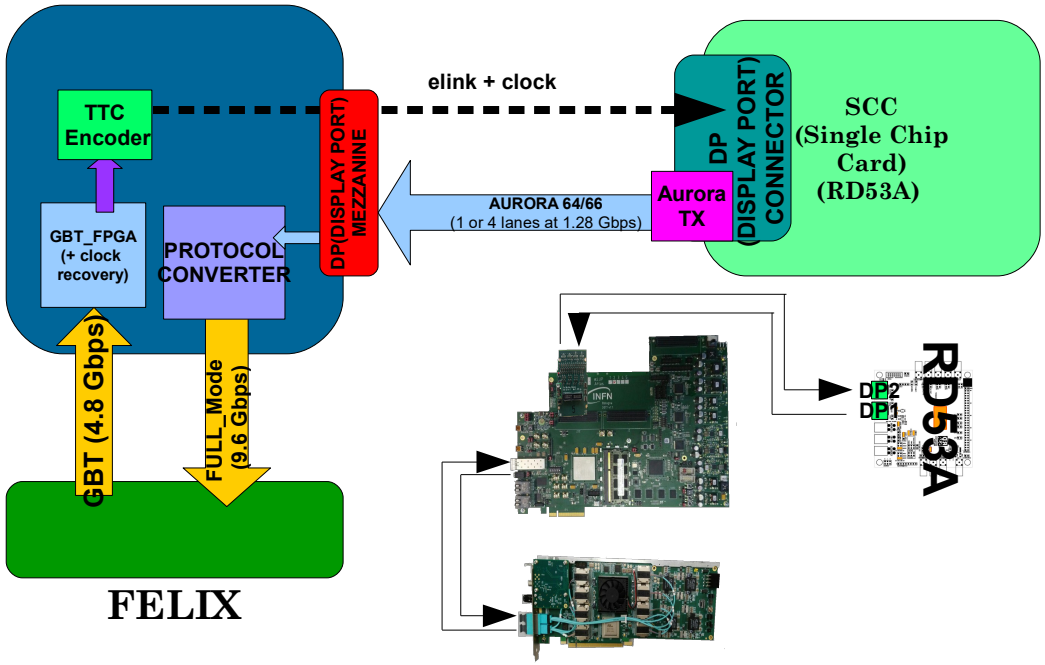
- **Embedded Linux system** running on the ARM processor;

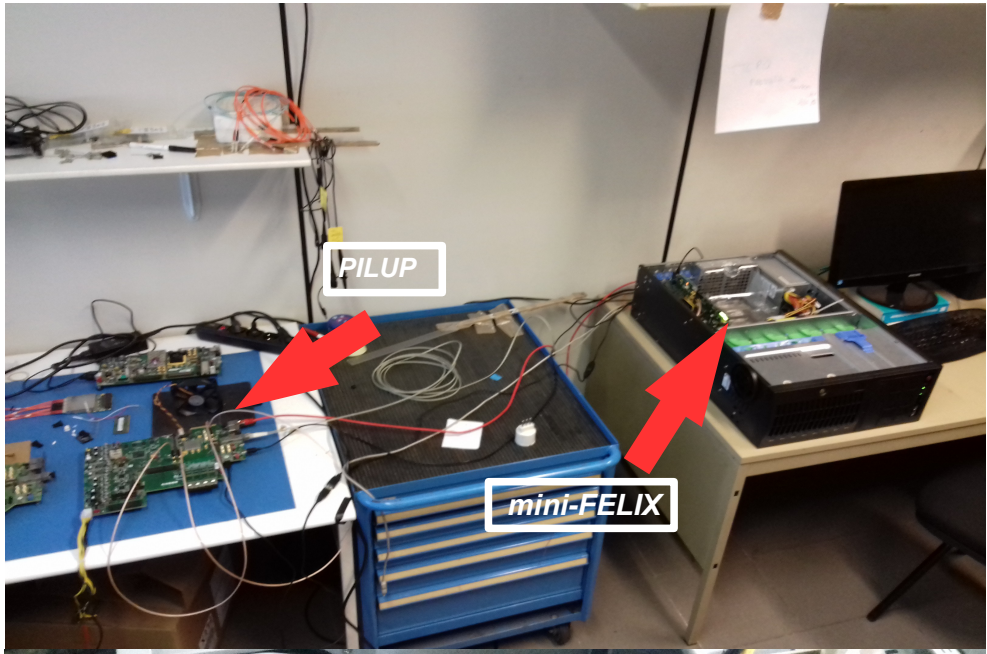
- Complete **low-level control** from the Zynq-7000 and **high-level management** of the system from external interfaces;

- **AXI4 addressable register block** to control custom logic without AXI4 interface.

Actual Tasks

Protocol Converter





FPGA fabric is great for irregular (and regular) computation