ETH zürich

TID effects at 130nm pixel electronics at low dose in ATLAS

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** now ETH Zürich, CMS. Previously CERN, ATLAS.*

Outlook

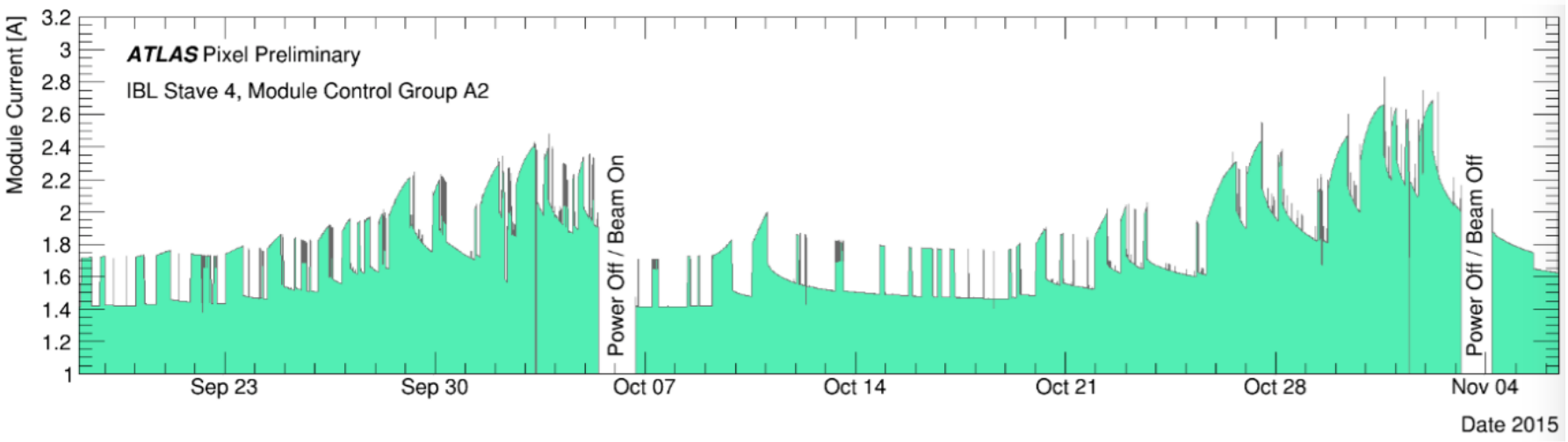
- Observations in early operation: 2015
- Investigation program and task force
- Boundary conditions
- Previous measurements and microscopic origin
- Expectations
- Reproduction and characterization in the laboratory
- Parametrization of macroscopic observation
- Derived detector operation guidelines
- Observations after 2016
- Summary / Lessons learned

Bibliography

- Public results of ATLAS IBL low voltage current task force:
  https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIX-2015-008/
- ATLAS IBL low voltage current task force - public note:
  ATL-INDET-PUB-2017-001
- ATLAS IBL distortion task force - public note:
  ATLAS-INDET-PUB-2015-001
- Parametrization model of radiation induced current increase:
  M. Backhaus *2017* JINST **12** P01011
- Radiation-Induced Edge-Effects in Deep Submicron CMOS Transistors:
  F. Faccio et al. *IEEE Trans. Nucl. Sci.* **52** (2005) 2413
- Production and Integration of the ATLAS Insertable B-Layer
  The ATLAS collaboration *arXiv:1803.00844*
- Irradiation induced effects in the FE-I4 front-end chip of the ATLAS IBL detector
  A. La Rosa et al. *arXiv:1611.00803v1*
- Private communication:
  CMS CIC chip results
- Private communication:
  ATLAS ABC chip results

Observations in 2015

[ATL-INDET-PUB-2017-001]

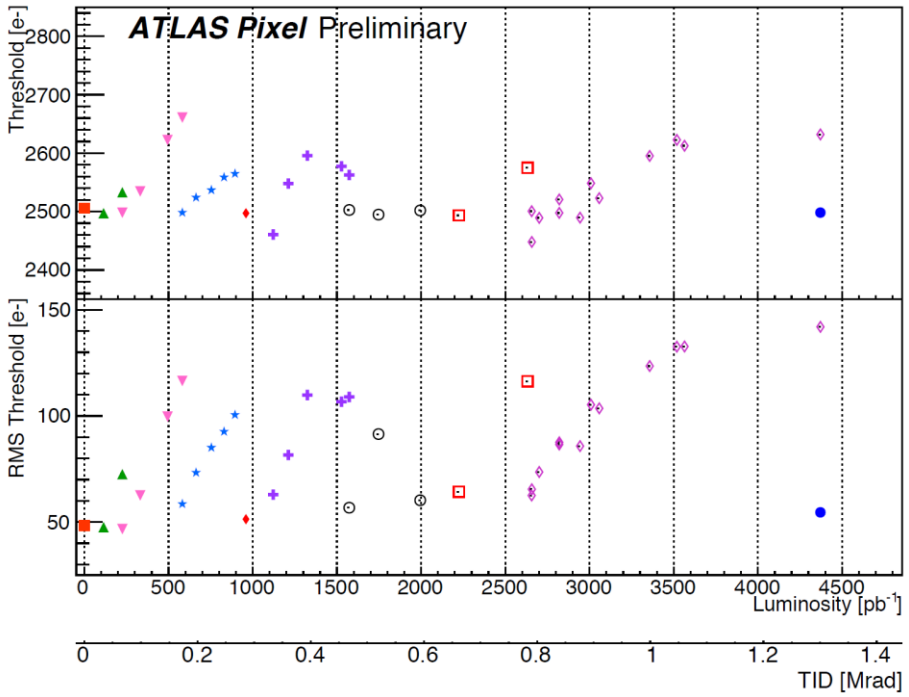


- Two levels due to preamplifier off without stable beams
- Increase of supply current during collisions, recovery between fills
- Safety power off on 6th of October and 4th of November
- Complete recovery after power off periods, similar increase during operation after off

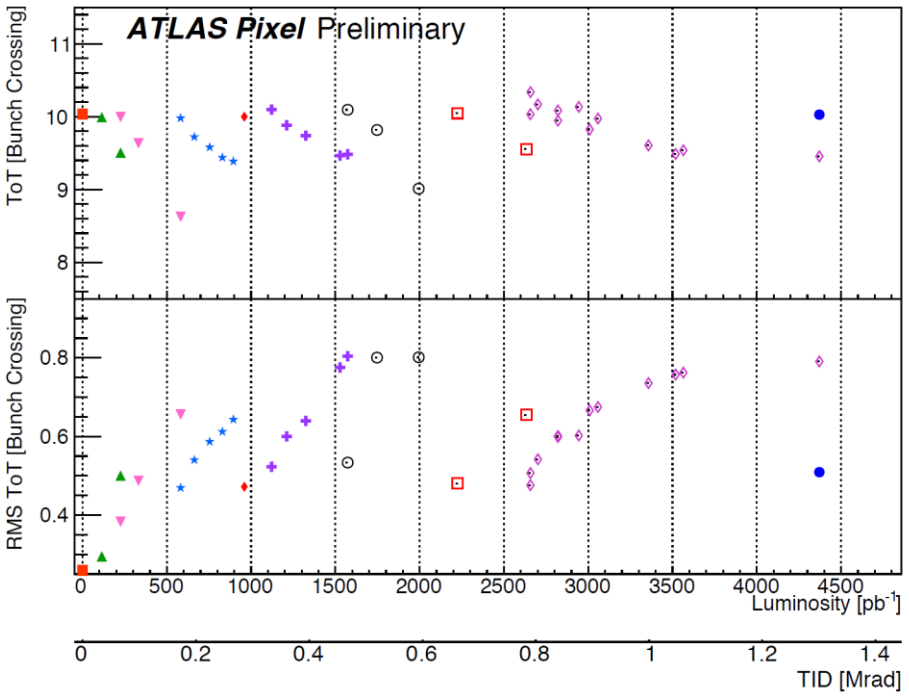
- Note: FE-I4b chips fully functional at all times without performance decrease. Observed current increase problematic at the detector system level.

Observations in 2015

[ATL-INDET-PUB-2017-001]



[ATL-INDET-PUB-2017-001]



- A drift of the calibration parameters during collisions observed (threshold and return to baseline time)
- Frequently retuned to original value

Task force and investigation program

- Task force created to:
  - Study the observations on FE-I4b and understand the effect, its perspective and impact on the detector system.
  - Characterization program:
    - Temperature
    - Dose rate
    - Mixed field irradiation in the experiment
    - Detector powering
    - Calibration parameter shift
    - Model the effect and extrapolate to future operation
  - Provide guidelines for safe operation.
  - Document and communicate the experience to outside the IBL/Pixel community.

Boundary conditions: IBL services

- Current increase not included in the system design
  (services, cooling, module wire bonds)

- FE-I4b maximum input current 1A:
  Maximum current per group 4A, not yet observed

Section	Resistance (Ω)	Voltage Drop (V)
Module	0.017	0.038
Stave flex	0.170	0.381
Intermediate flex	0.035	0.078
Cable board	0.033	0.074
Type 1 inner cable	0.139	0.311
Type 1 outer cable	0.091	0.204
LV regulator crate	0.046	0.103

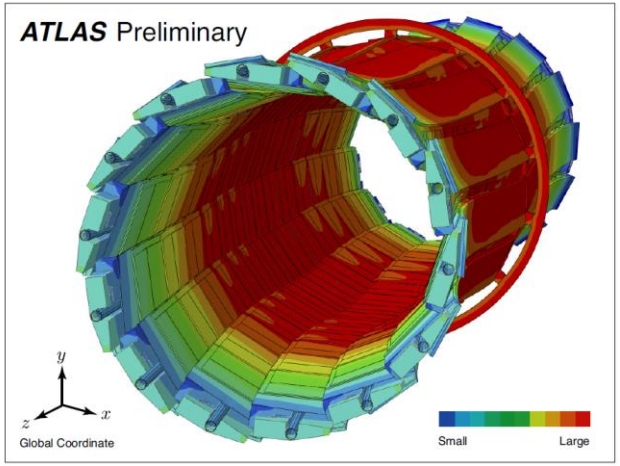
Table 20: Room temperature resistance and voltage drop for a single LV channel serving four FE-I4B chips at the maximum current of 0.56 A per chip (2.24 A per LV channel).

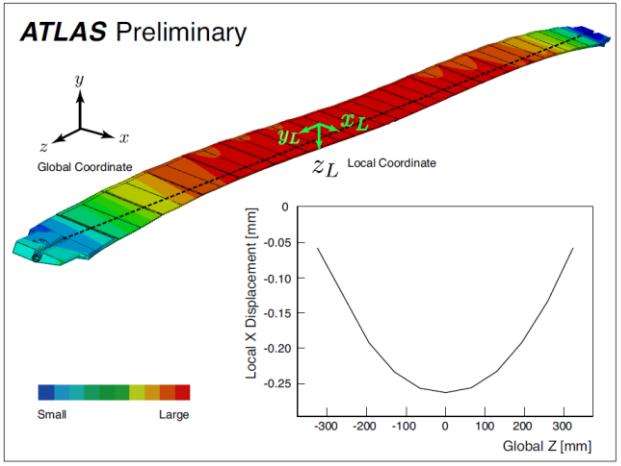
- Wire bond fusing
  25um aluminum wires fuse at 500-600mA. Two LDOs per chip, some chips with only two wires per LDO, but non-equal current sharing expected. Current per chip should not exceed ~750mA.

- Voltage transients
  Transients above 2.5V letal for chips. Power supply output voltage of 2.1V, but cables have resistance and voltage drop. Transients in case of current variation (configuration, trigger, etc.) must not exceed 2.5V.

Boundary conditions
IBL distortion

[ATLAS-INDET-PUB-2015-001]





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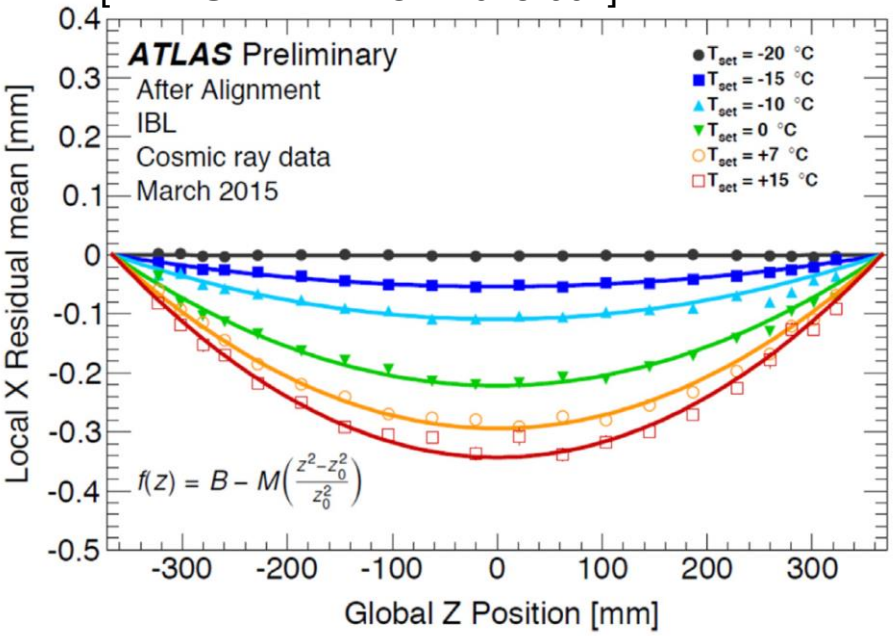
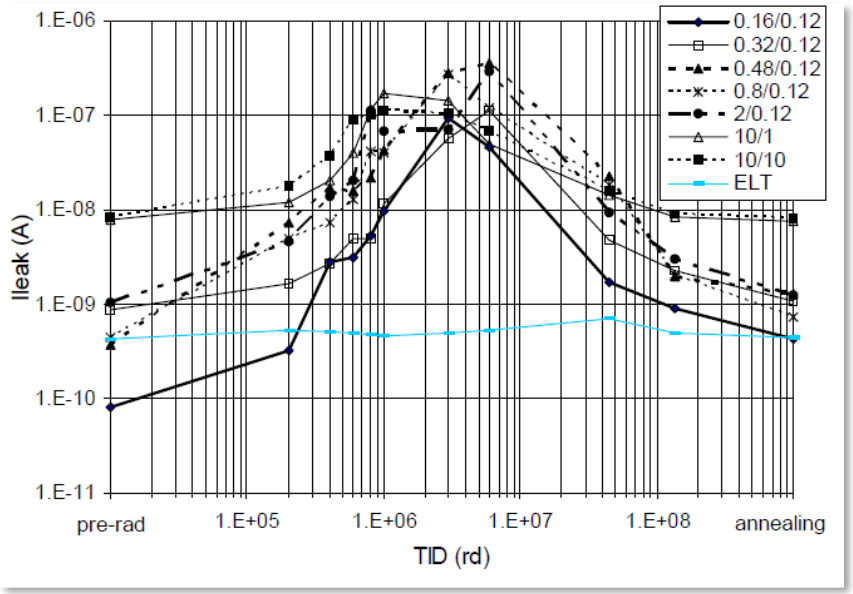


- ~10um/K local x displacement
- <2um displacement with negligible effect on data quality
- Temperature variation due to current increase to be kept below 0.2K

Previous Measurements

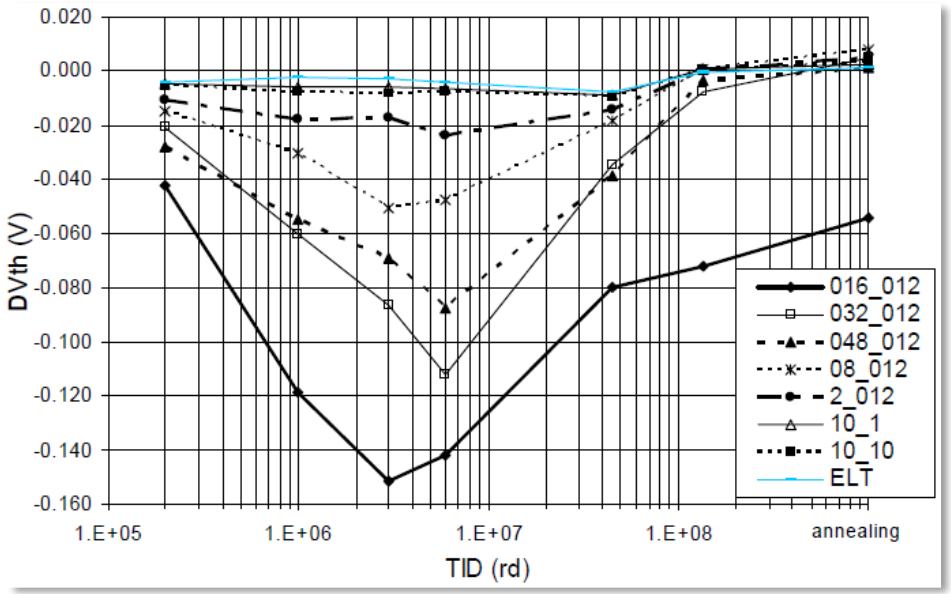
[F. Faccio et al. *IEEE Trans. Nucl. Sci.* **52** (2005) 2413]

Single Transistor Leakage current vs. TID



[F. Faccio et al. *IEEE Trans. Nucl. Sci.* **52** (2005) 2413]

Single Transistor Threshold Voltage vs. TID



Further information:

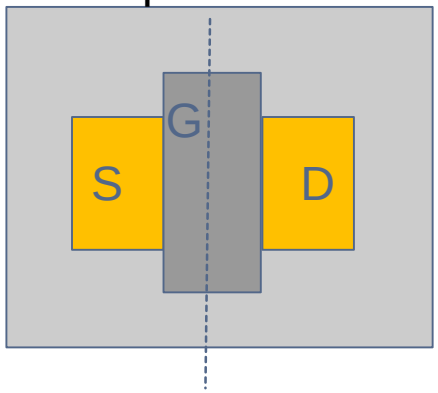
- Oxide charges are movable and can anneal as well at relatively low temperature and relatively fast. Powering OFF (no electrical field in oxide) increases annealing.
- Interface traps can be annealed, but due to their energy level only at high temperature (above 100 degrees Celsius in IBM 130nm).

→ Design recommendation: “Probably enclosed transistors not needed, but transistor leakage current to be considered”

NMOS radiation damage at low TID

Profound understanding thanks to very informative discussions with F. Faccio

Top View

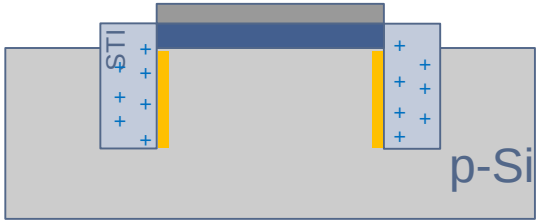


Top view of a NMOS transistor, Channel formation from S to D.

Cross section

Cross section at indicated line, including STI and channel below gate (in case transistor is switched ON).

Low TID



Cross section after ionizing irradiation if transistor is OFF. Channel formation due to electrical field of positive charges trapped in silicon oxide of the STI.
→ leakage current and threshold voltage shift.

→ With TID the leakage current increases due to positive oxide charge (and threshold voltage decreases).

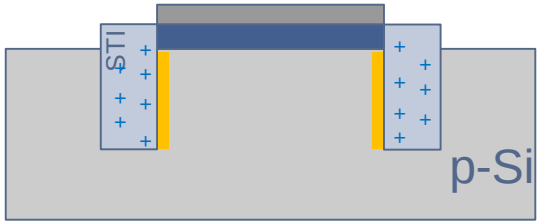
NMOS radiation damage at high TID

Profound understanding thanks to very informative discussions with F. Faccio

Before Irrad

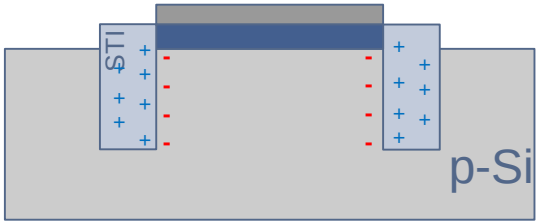
Si to SiO2 interface transition from crystalline to amorphous material
→ dangling atomic bonds.
Dangling bonds are charge carrier traps.
Depending on Fermi Level (n/p type silicon) electrons or holes are trapped.
Dangling bonds filled by manufacturer with hydrogen to achieve a good charge carrier flow.

Low TID



Cross section after ionizing irradiation if transistor is OFF. Channel formation due to electrical field of positive charges trapped in oxide along the STI
→ leakage current and threshold voltage shift.

High TID



Positive charge carriers move to SiO2-Si interface. The positive charge carriers release the hydrogen and the interface traps become active.
Electrons are trapped (p-type silicon) and compensate the electrical field of the positive charges in the STI.
→ Leakage current decreases and threshold voltage increases.

→ At high TID interface traps compensate the initial effect and the leakage current decreases.

Expectations

- Strong **temperature** effect:
  Higher diffusion at high temperature leading to lower transistor leakage current
- Strong **dose rate** effect:
  Lower dose rate providing more time for diffusion resulting in lower lower transistor leakage current
- Effect of **digital supply voltage**:
  Large majority of NMOS transistors in digital logic, only small fraction and large transistors in analog power domain
- Strong **annealing** whithout power:
  Quick diffusion without field in transistor
- **Return** to “no annealing curve” **after annealing**:
  Only oxide charges anneal at low temperature
- **Constant** increased current **at high dose**:
  No complete cancellation of space charge in oxide vs. interface
- Calibration parameter shift:
  Caused by single transistor leakage current curve
- No effect on powering mode:
  Not an LDO effect, not effecting DACs and reference current
- **Reproducable** with **Xrays** and in proton beam
  No additional effect in proton beam, pure TID effect

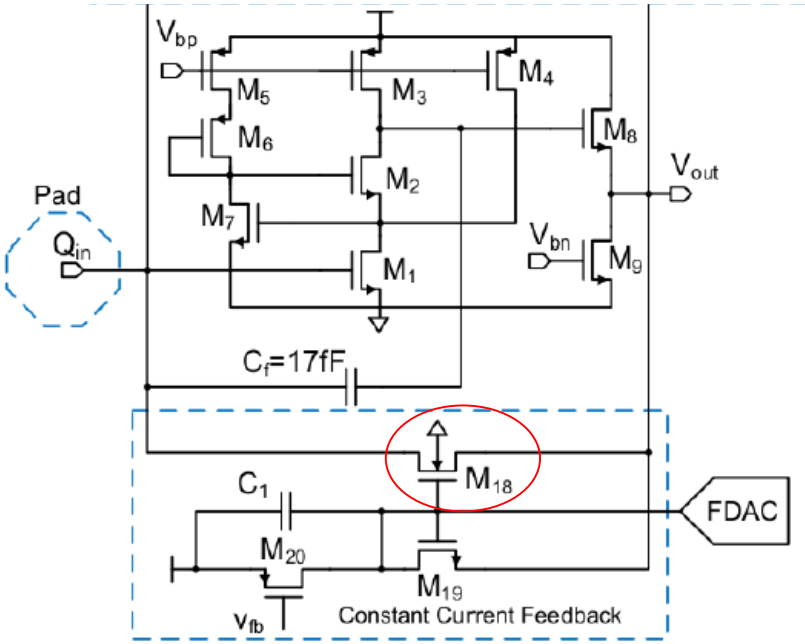
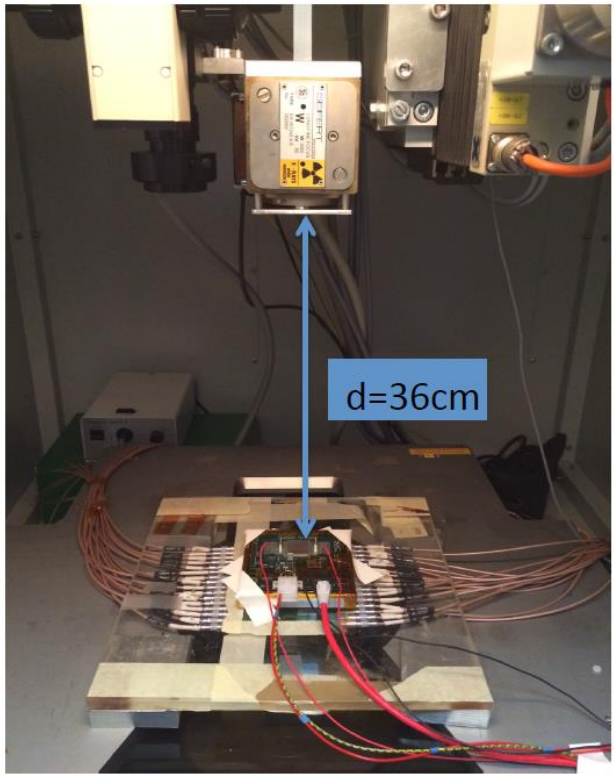
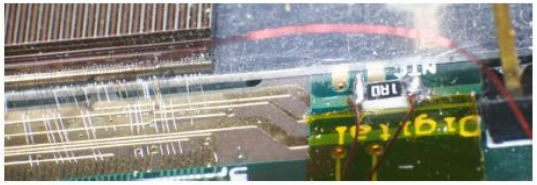


Figure 10: Analog front end preamp circuit schematic.

Reproduction in the laboratory

- **CERN PH-ESE X-ray machine**
  (thanks to F. Faccio)
  - X-ray tube using Tungsten target (peak 10 keV)
  - Operated at different dose rates
  - Exposed at different temperatures
- **Bare FEI4b onto PCB**
  - Show only results of IBL powering scheme
  - Chip in operation during irradiation
- **USBpix readout system**
  - Current monitoring
  - Permanent execution of measurement of threshold, noise ToT, etc.





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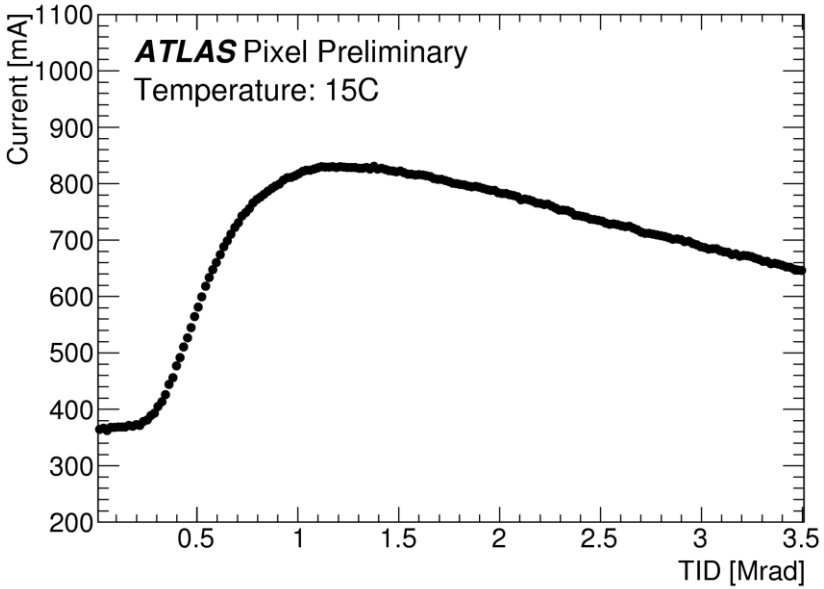
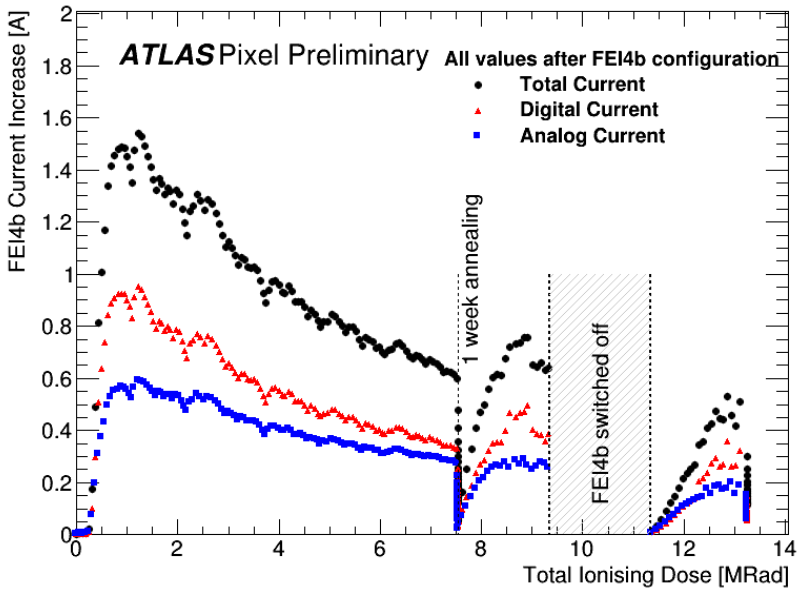
Reproduction in the laboratory

[https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIX-2015-008/]



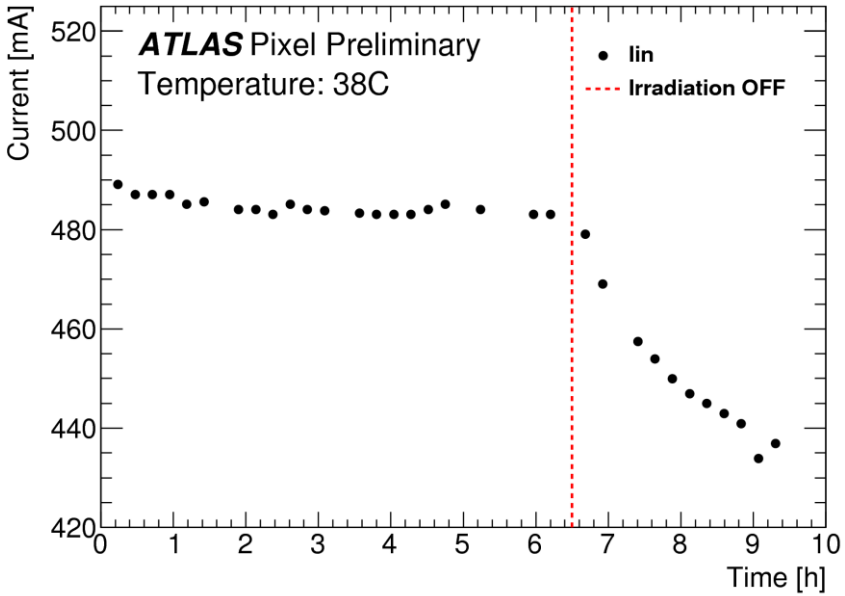
[ATL-INDET-PUB-2017-001]



- Left plot: current increase reproduced with Xray irradiation.
- Right plot: similar increase (and no additional effect) validated with proton beam University of Bern. Thanks for very flexible and efficient contribution.

Reproduction in the laboratory: Annealing

[https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIX-2015-008/]



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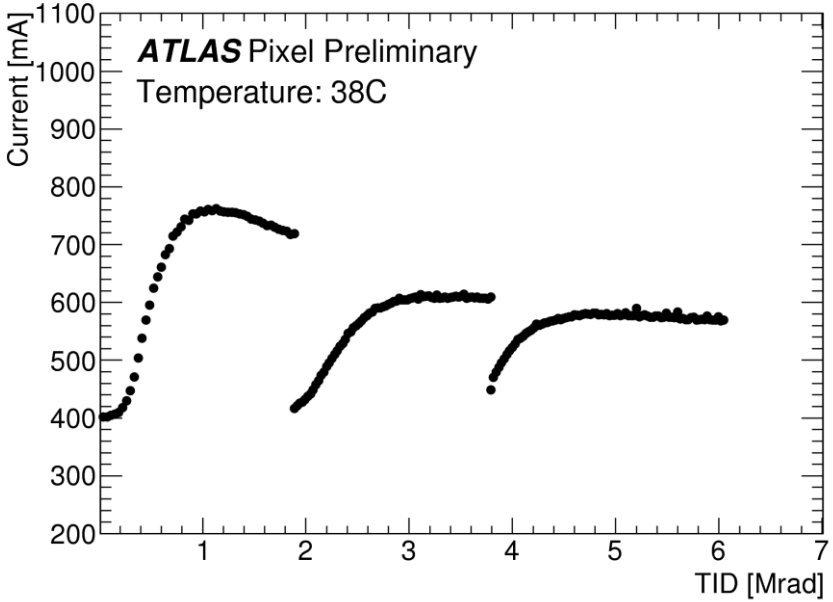
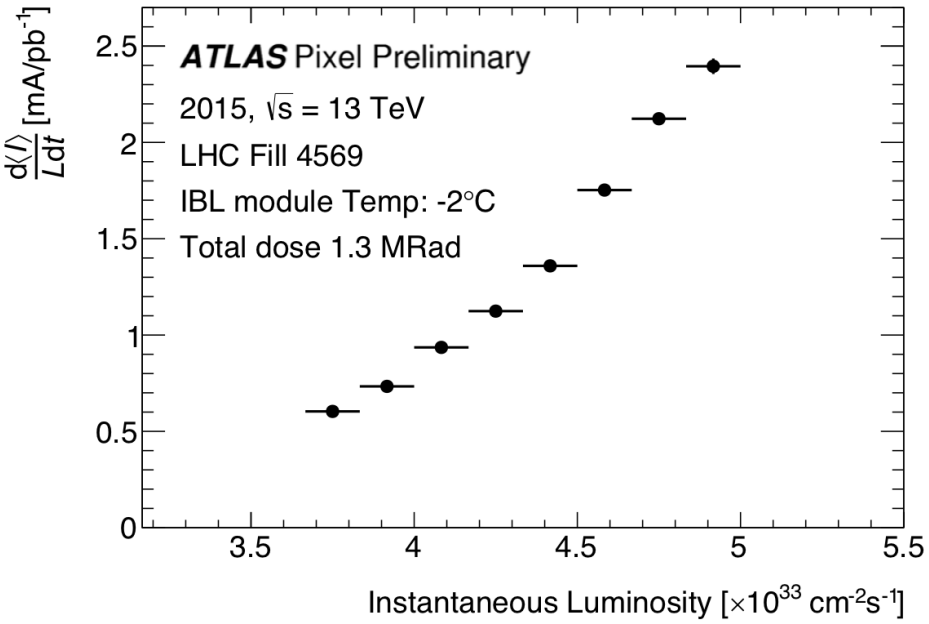


120 krad/h

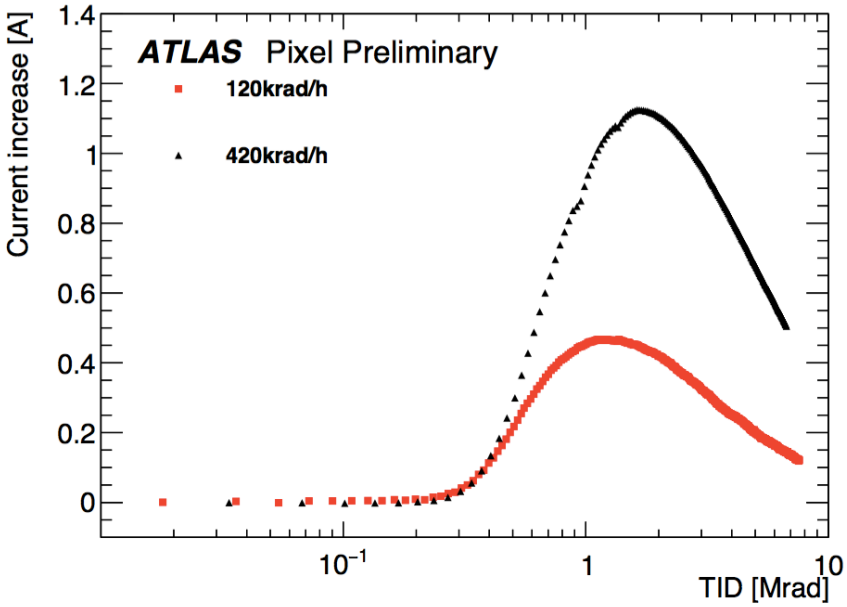
- Left plot: current curve after irradiation reproduces observed exponential behavior between LHC runs with power on.
- Right plot: Return to baseline and increase after long power off periods reproduced with Xray irradiation.

Reproduction in the laboratory: Dose rate

[ATL-INDET-PUB-2017-001]



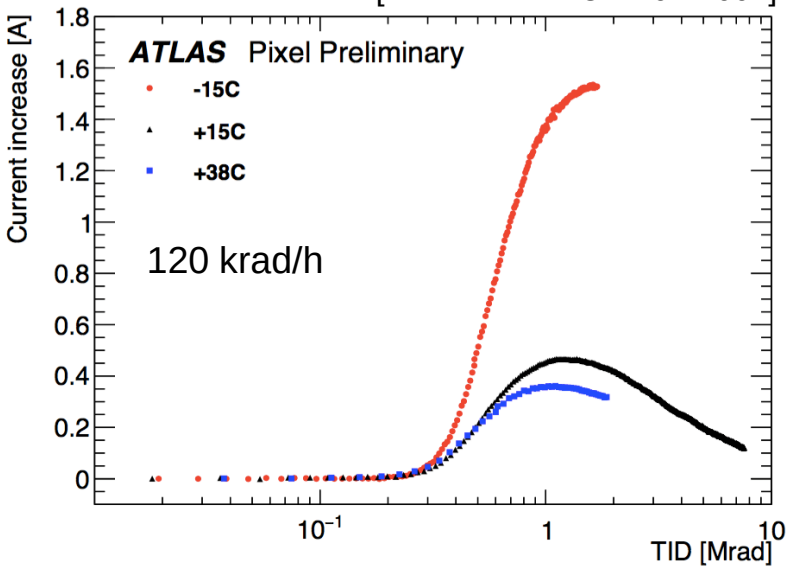
[ATL-INDET-PUB-2017-001]



- Left plot: „instantaneous“ measurement of the current increase slope in the detector as a function of luminosity (or dose rate).
- Right plot: Validation of expected dose rate dependence. Larger dose rate results in higher current increase.

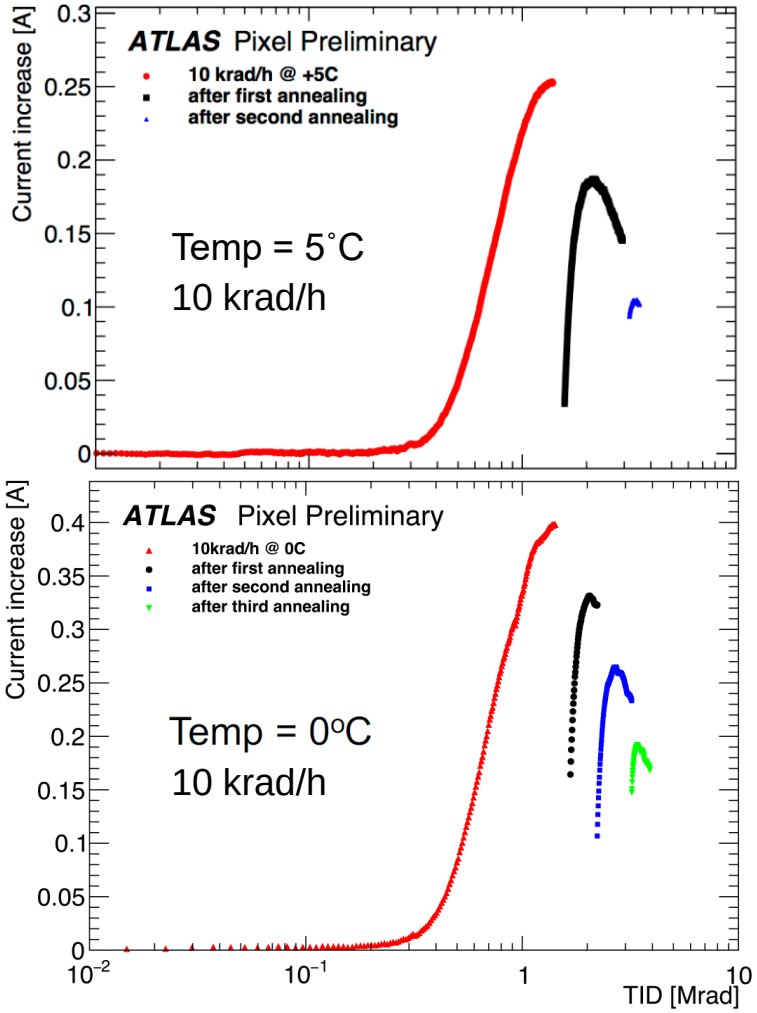
Reproduction in the laboratory: Temperature

[ATL-INDET-PUB-2017-001]



- Higher temperature
  → lower current increase amplitude
- Measured at low dose rate (10krad/h) temperature safe for IBL: 5˚C

[A. La Rosa et al. *arXiv:1611.00803v1]*



Reproduction in the laboratory: Calibration parameter shift

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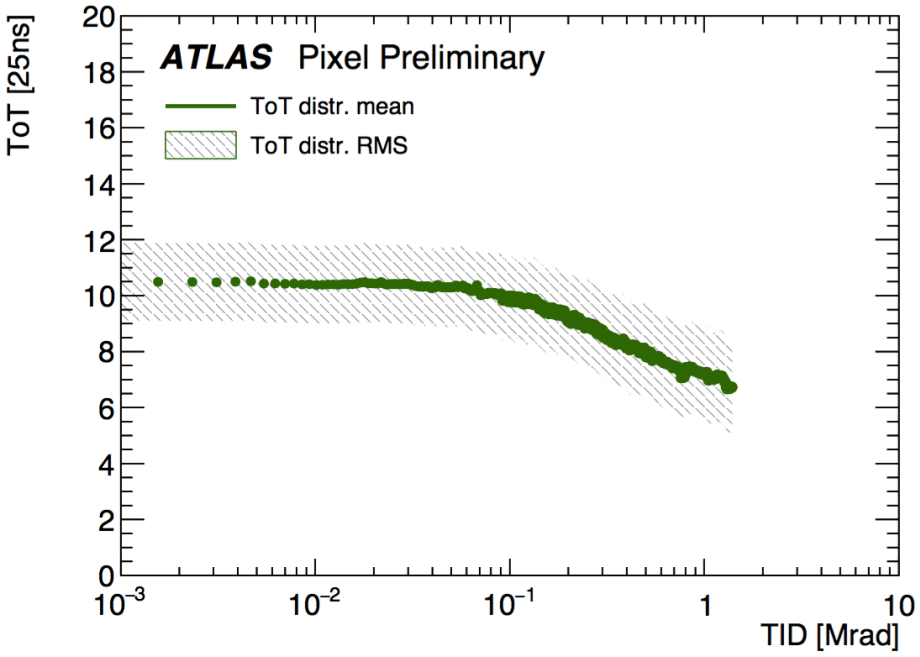

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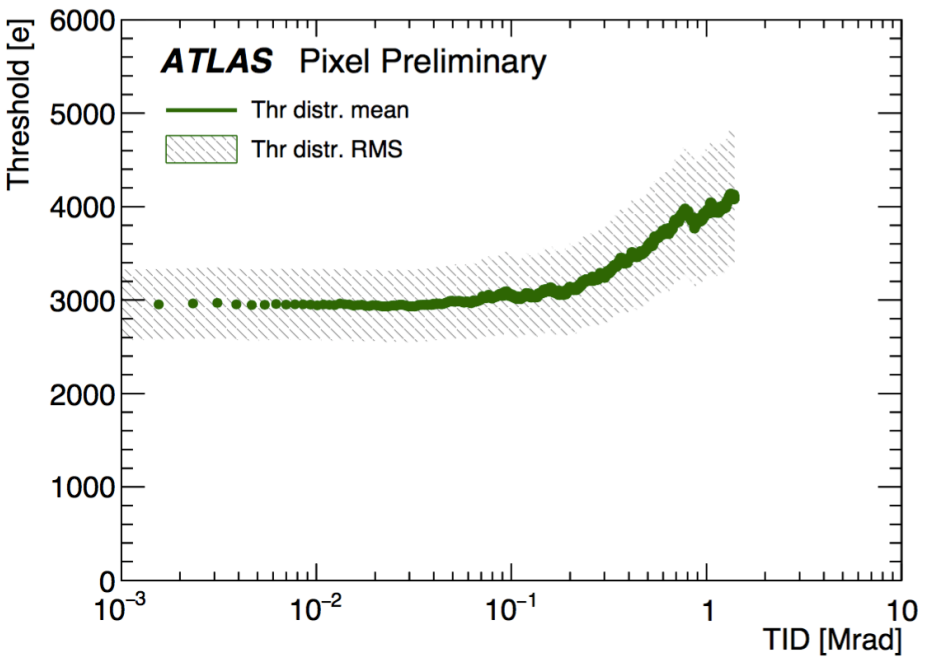


- „Amplifier return to baseline“ (left) and discriminator threshold (right) shift in Xray radiation as observed in detector. Same microscopic origin as current increase.

→ All detector observations and expectations reproduced with Xrays.
→ Work towards a model to predict behavior for future operation

Parametrization of effect

- Developed a model describing the macroscopic observation based on the microscopic physics.
- Use transfer characteristics of the parasitic transistor due to formation of space charges

Describe current increase by parasitic transistor:

$$I_D \approx K' \cdot (V_G - V_{\text{thr}})^2$$

$$I_D^{\text{par}} = K \cdot (N_{\text{eff}} - N_{\text{thr}})^2$$

Potentials replaced by „effective number of charges“

Derive number of charges as function of irradiation time *t* at dose rate D:

$$\frac{d}{dt} N_{\text{ox}}(t) = k_{\text{ox}} D - \frac{1}{\tau_{\text{ox}}} N_{\text{ox}}(t)$$

$$N_{\text{ox}}(t) = k_{\text{ox}} D \cdot \tau_{\text{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{ox}}}}\right)$$

Analog for radiation induced interface traps

Final parametrization:

$$I_{\text{leak}} = I_{\text{leak}}^0 + K \cdot \left[k_{\text{ox}} D \cdot \tau_{\text{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{ox}}}}\right) - k_{\text{if}} D \cdot \tau_{\text{if}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{if}}}}\right) - N_{\text{thr}}\right]^2$$

Measured temperature and dose rate dependence of constants

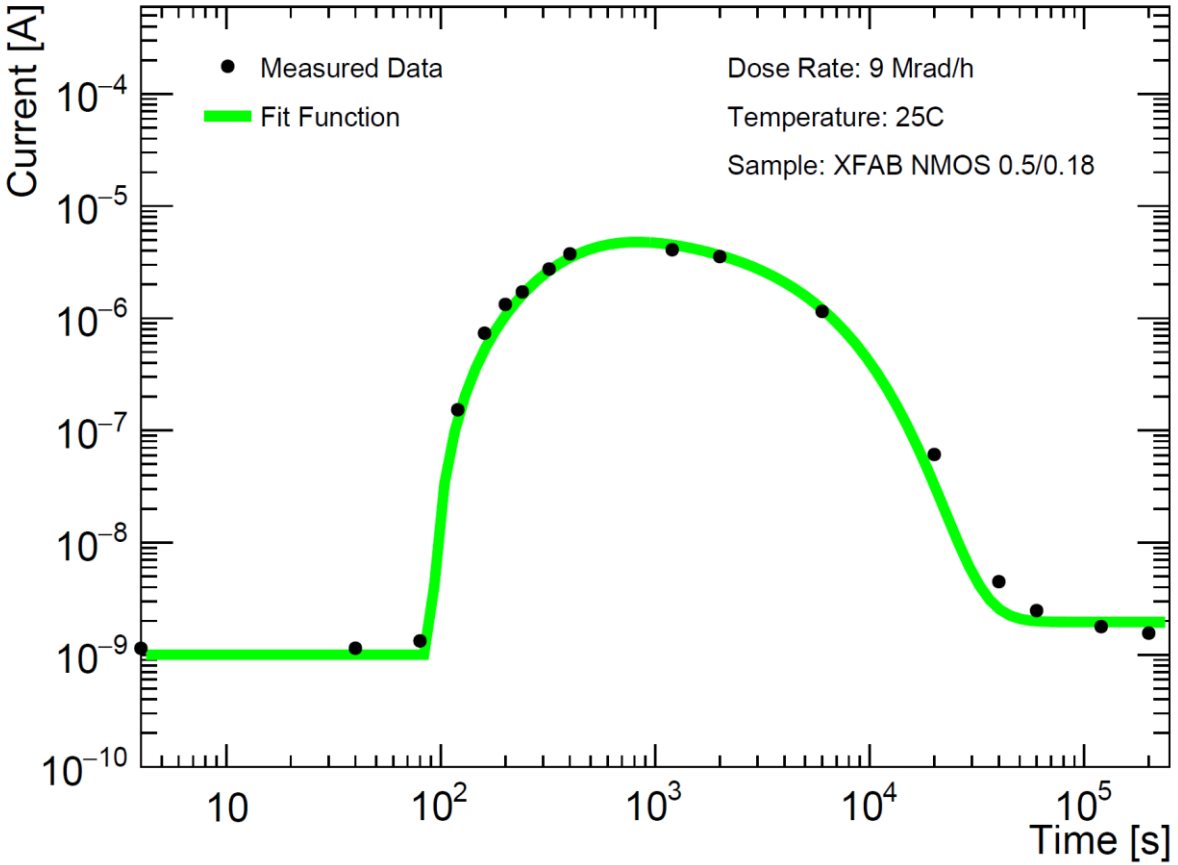
Name	Explanation
T[C]	Temperature of chip
k_{ox}/rad	Number of trapped holes per dose unit
k_{if}	Number of holes for interface activation per dose unit
N_{thr}	Number of threshold charges
D [rad/s]	Dose rate
τ_{ox} [s]	lifetime of oxide charges
τ_{if} [s]	lifetime of interface traps
K	proportional constant
I_0 [mA]	start current

Parametrization of effect: Fit to single transistor leakage current data

[M. Backhaus *2017* JINST **12** P01011]

- Model fits to single transistor leakage current data

→ Full chip current increase cummulation of this?



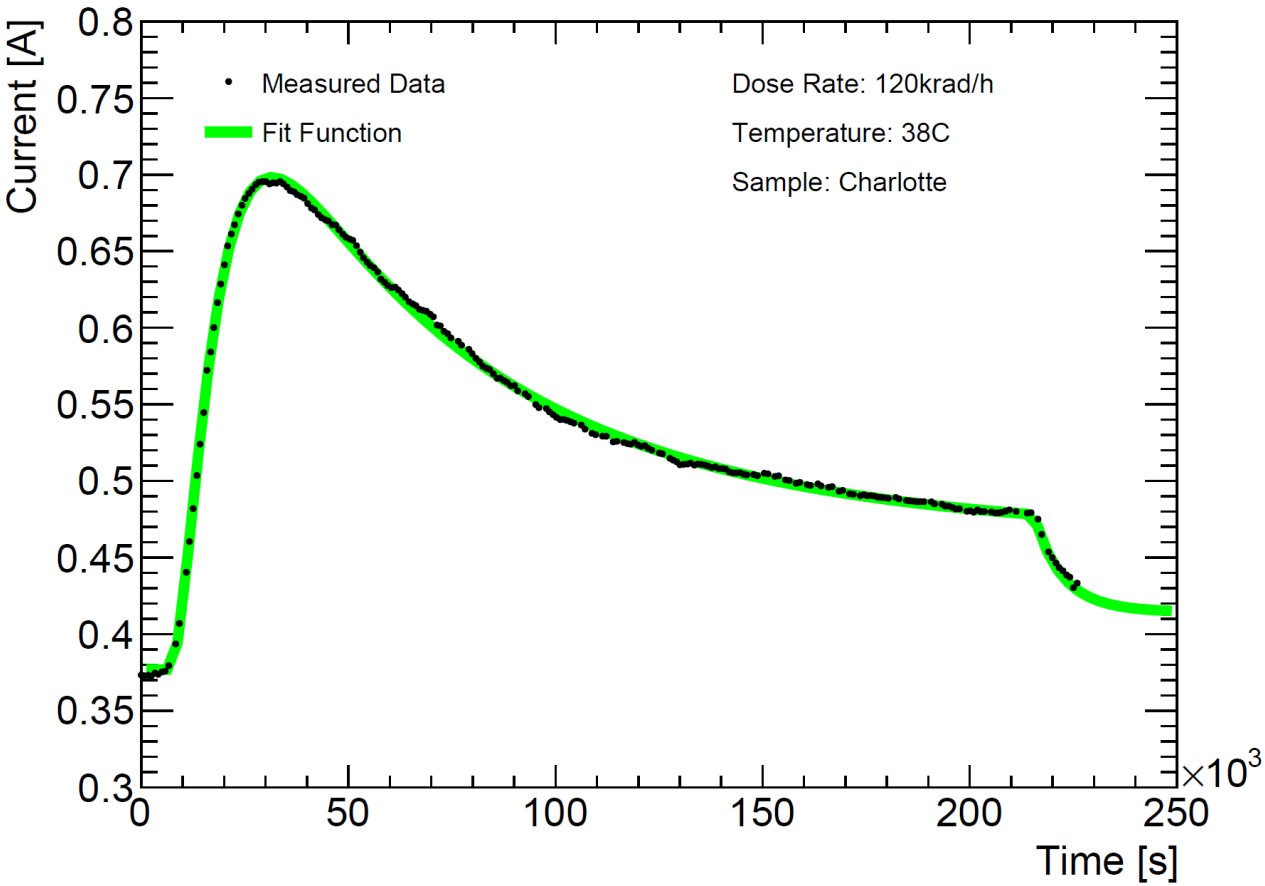
Data taken from: S. Fernandez-Perez et al.: Nucl. Instrum. Meth. A 796 (2015) 13.

Parametrization of effect: Fit to FE-I4b low voltage current

[M. Backhaus *2017* JINST **12** P01011]

- The same model fits to ASIC leakage current increase
  → same shape/origin
- Also annealing of oxide carges (but not interface traps) included

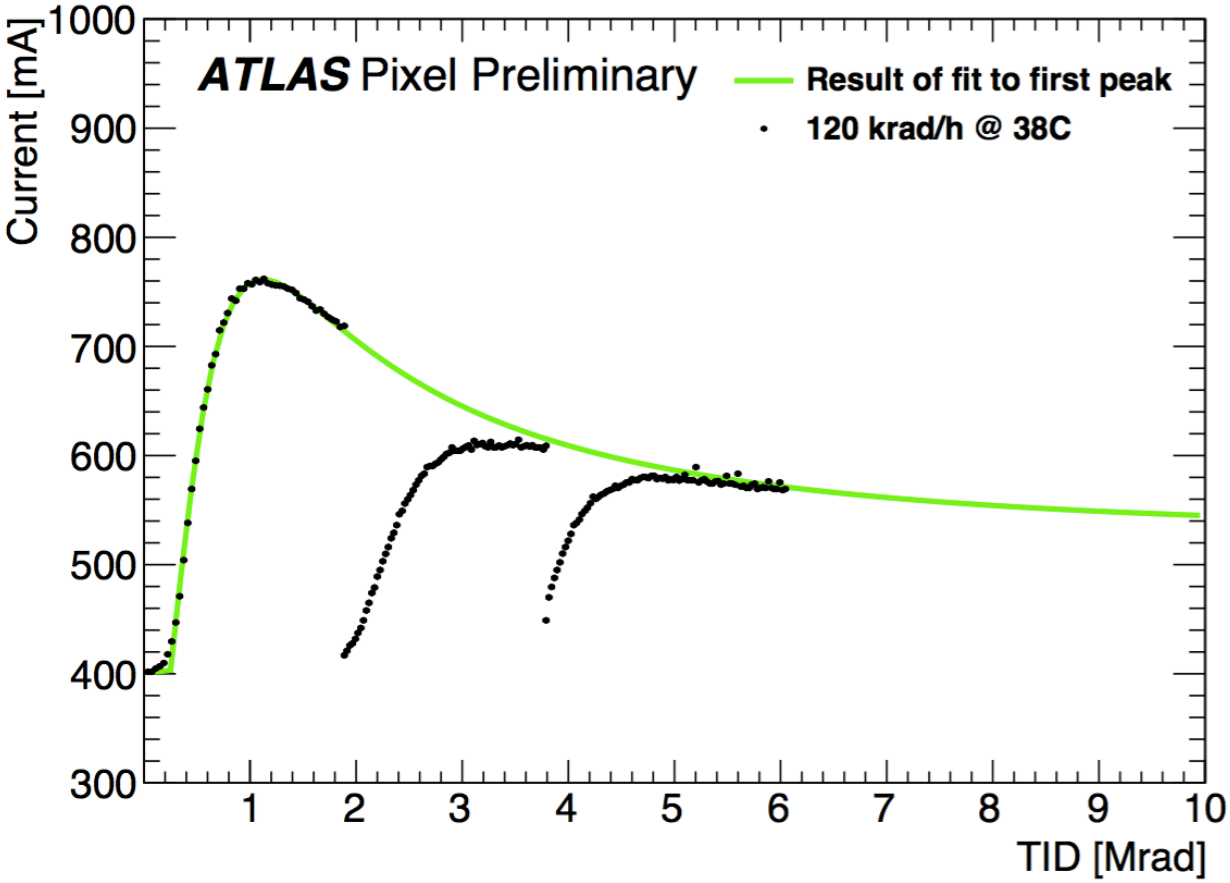
→ Does current after annealing period Approach this curve?



Parametrization of effect: Fit to FE-I4b low voltage current

- Fit model to first peak only
- Afer re-irradiation and steep rise the current follows again the same shape

[https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIX-2015-008/]



Parametrization of effect: Fit to FE-I4b low voltage current

- Model published: M. Backhaus *2017* JINST **12** P01011
- Used to derive the supply current of chips for future experiments
  → ASIC and detector system design constraints

Jinst

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Parametrization of the radiation induced leakage current increase of NMOS transistors

M. Backhaus[1]

Experimental Physics Department, CERN,

For FE-I4b:

$T[°C]/D$ [krad h^{-1}]	TID_{max}[Mrad]
38 / 120	1.05
15 / 120	1.18
15 / 420	0.45

$T[°C]/D$ [krad h^{-1}]	ΔI_{max}[A]	ΔI_{sat}[A]
38 / 120	0.321	0.111
15 / 120	0.470	0.111
15 / 420	1.117	0.111

ATLAS IBL operation guidelines

In YETS 2015/2016 the following operation guidelines for 2016 were developed based on the presented results:

1) Immediate highest priority: lower current increase while operating the detector efficiently and safe

- Low voltage current limit increase: from 2.8A to 3.0A (current per chip up to 750mA)
- Operation temperature increase: from -10C to +15C
- Digital supply voltage decrease: from 1.2V to 1.0V
- Regular tuning of calibration parameters

  Result: immediate and large decrease of the current increase

2) Avoid long term damage for sensors (mainly increase of full depletion voltage)

- Asap. decrease of temperature: from +15C to +5C

  Result: Negligible to no current increase

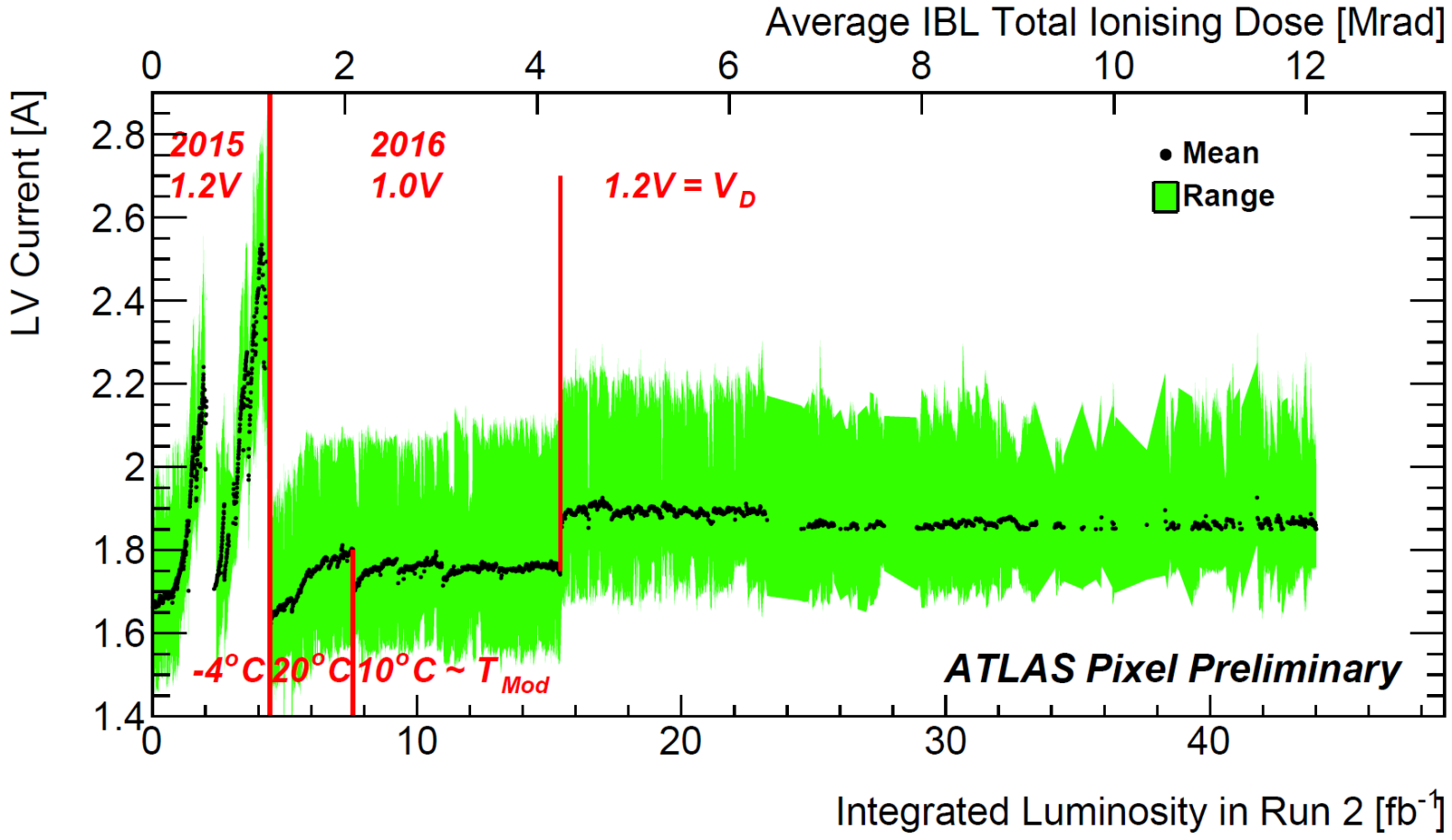
3) Additional measurements during 2016 secure operation at nominal voltage and +5C

- Return to nominal digital voltage: from 1.0V tp 1.2V

  Result: slight increase of current, but reduction of SEUs and readout errors

→ Peak of increase passed without damage and stable low voltage currents achieved

Observations after 2015



Lesson learned for Phase 2 detectors!

- Although IBL succesfully operated without damage and with full efficiency, the increase was a serious challenge for the detector.
- FE-I4b chips operational full time.
- Supply current increase due to transistor leakage current was not included in detector system design
  → impressive work being done for ATLAS and CMS strip upgrades for phase 2:
  - Both experiments use chips in 130nm technology
  - Developed model extended by measurements in the dose rate vs. temperature parameter space
    → can extrapolate to lower dose rates as expected in the experiment
    → able to predict the maximum supply current of the detector
    → design the system for the maximum current
- ATLAS and CMS pixel upgrades in 65nm technology
  → transistor leakage current increase measured → negligible
  → „this problem“ not expected, but must be verified on large chips