SEU in ATLAS FE-I4 electronics

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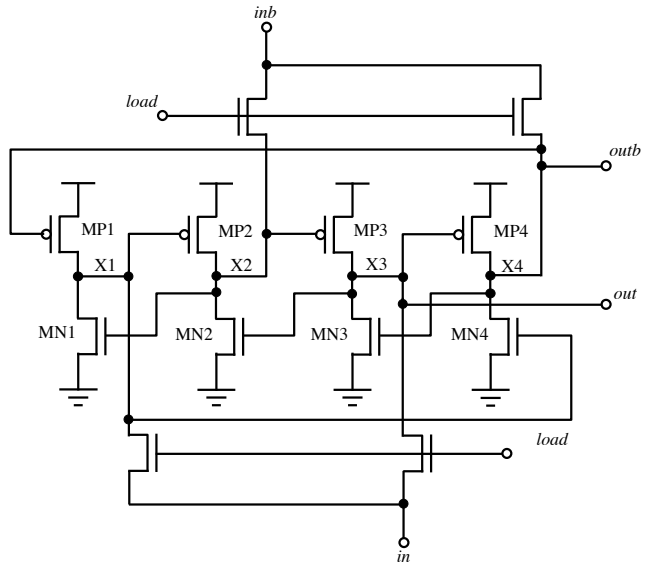
Introduction

- During 2016/2017 data taking campaign LHC delivered in total 87fb^{-1} of integrated luminosity, reaching 2.09×10^{34}cm^{-2}s^{-1} of peak stable luminosity
- The ATLAS Pixel detector operated in an unprecedented high-radiation environment, and in particular the Insertable B-Layer (IBL) being the closest layer to the interaction point
- The FE-I4 has specialised electronic circuits designed to be very SEU-hard, which stores both global and pixel configuration in Dual Interlocked CElls (DICE) latches, arranged in a special layout
- We present a series of observations and measurements of the effects of both the global and pixel registers corruption due to SEU using 2016 and 2017 data delivered by LHC

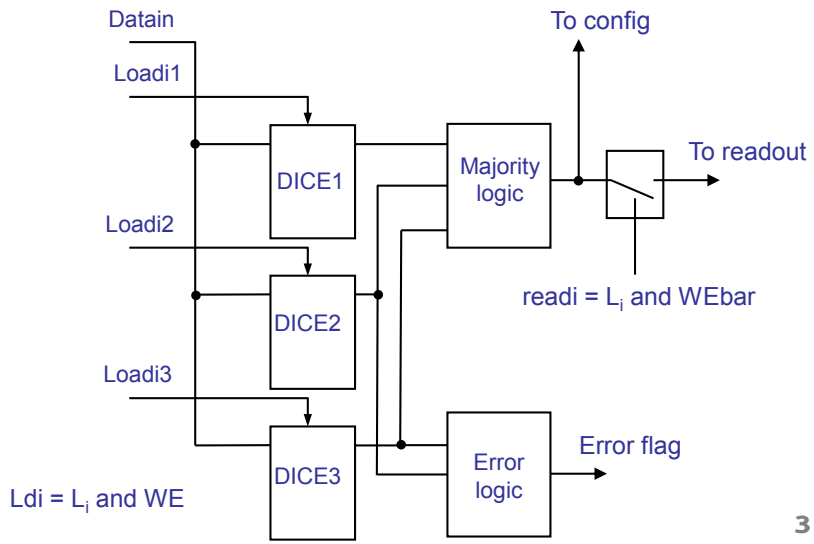
FEI4 - DICE Latches and global configuration

- FE configuration memory is stored in Dual Interlocked CElls (DICE)
- SEU tolerant memory
- X1-X4 store data as 2 pairs of complementary values
- If, for example, X1 $0 \rightarrow 1$, MP2 (MN3) is blocked avoiding perturbation to X2 (X3)
- If X1 and X3 are upset, then memory is corrupted



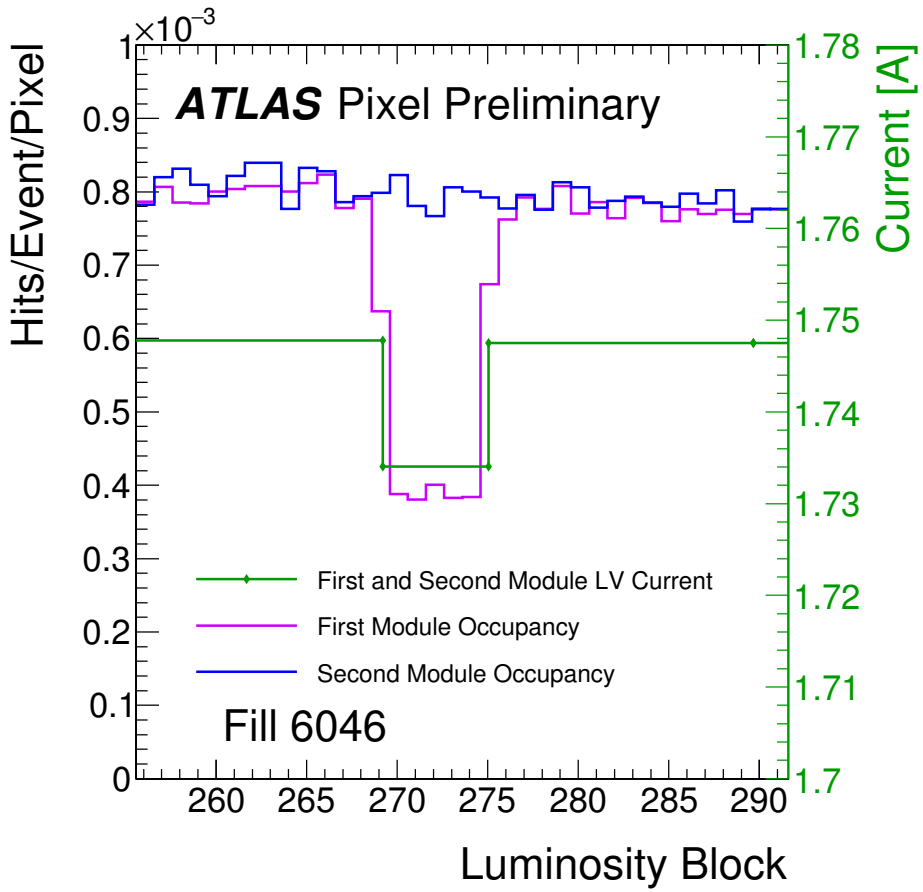
Global Configuration

- 32 16-bit words (512 bits total)
- Control general operation of the chip
- Triple DICE latches redundancy
- SEU-hardness measured in CERN-2008-008, JINST 8 C02026, FE-I4B Manual.



Global Registers SEU effects

- Global Registers corruption has large impact on the correct module operation
- The Low Voltage (LV) current consumption and the Hits per Event per Pixel per Front-End show both a drop is often observed when a front end global configuration gets corrupted
- The LV measurement has only 4 FEs granularity
- Corrective actions (re-send of global configuration) taken at the event counter reset signal (ECR) restores the proper function of the module



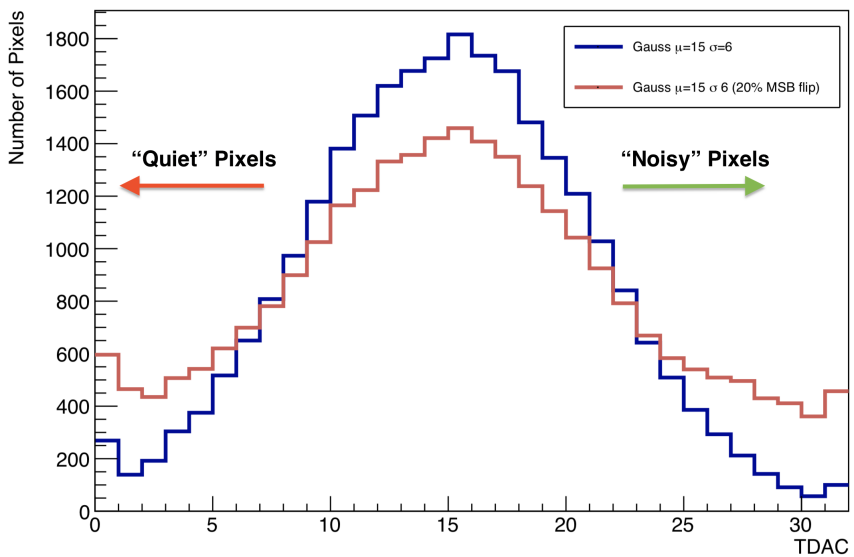
FEI4 Pixel Configuration

Pixel Configuration

- 13 bits per pixel
- output enable, TDAC (5-bits) analog threshold, FDAC (4-bits) for feedback current

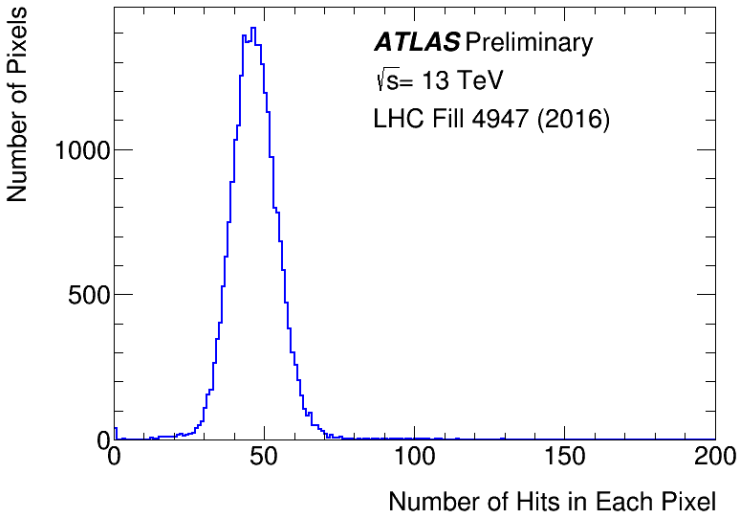
PxStrobes	Latch controlled in the pixel
[0]	Output enable. Must be set to 1 to see hits through the normal readout path.
[1:5]	TDAC value [1]=MSB
[6]	Large injection capacitor. Must be 1 to inject charge through this capacitor.
[7]	Small injection capacitor. Must be 1 to inject charge through this capacitor. In parallel with large capacitor.
[8]	Imon and Hitbus out. Must be 1 to monitor leakage current or 0 to include pixel in hit bus.
[9:12]	FDAC value [12]=MSB

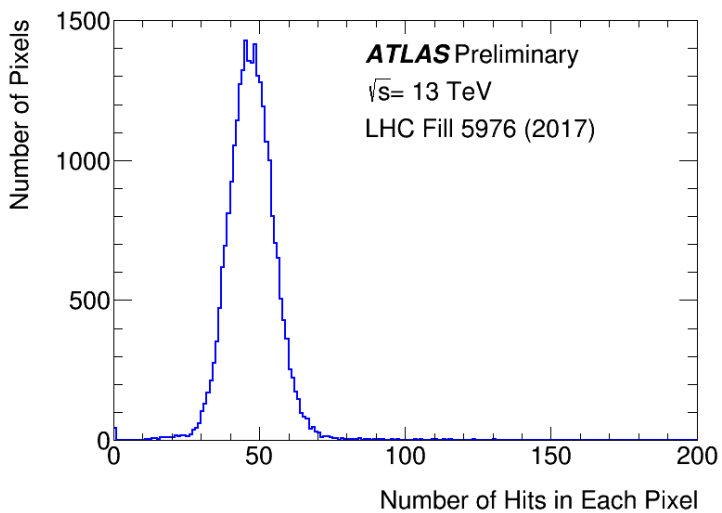
- In data-taking configuration:
  - Output enable mostly stores 1s
  - TDAC is centered around 15
  - FDAC is centered around 7
  - Charge injection capacitor selection and hit-bus are at 1
- SEUs during data taking corrupt pixel configurations leading to:
  - Quiet pixels
  - Noisy pixels
  - General detuning



Quiet Pixels observation 2016/2017

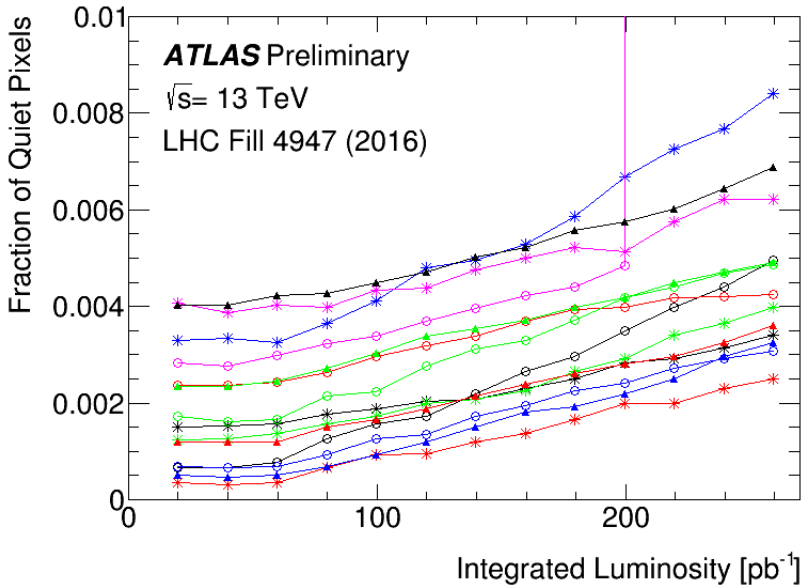
- Study of the fraction of pixels that get quiet during a data-taking in 3D modules
- In 2016 (2017) the average occupancy **in the most forward 3D module** in the C-Side is measured to be about 46 (47) in a pre-defined integrated luminosity range
- Only single pixels clusters in z-direction are taken and edge pixels are removed
- The average occupancy has been shown to be flat with respect to the pixel location on the sensor
- The probability that a normal pixel never fires in that period is 1.1×10^{-20} (3.9×10^{-21}) for 2016 (2017)
- **A pixel is considered quiet if it never fired during that time**

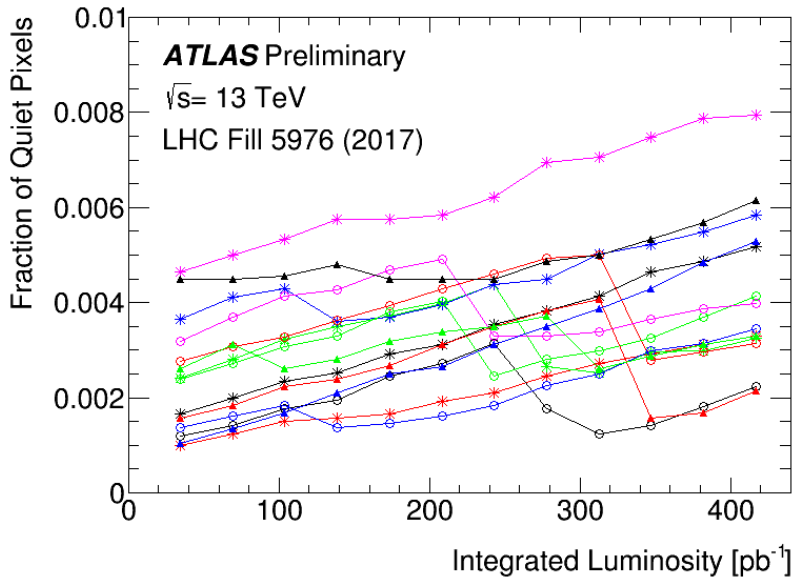




Quiet Pixels observation

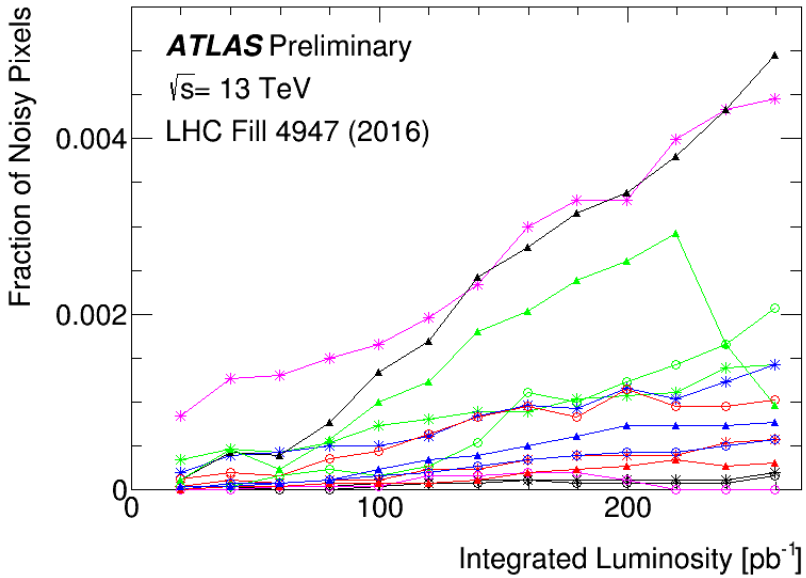
- The fraction of quiet pixels increases linearly with luminosity
- Similar slopes across the various modules
- Initial point corresponds to the initial disabled pixels in the module.
- 2016: One module got disabled $\rightarrow$ quiet fraction to 1
- 2017: Single modules auto-reconfiguration actions are active and show reduction quiet pixels $\rightarrow$ confirmation that is configuration corruption effect

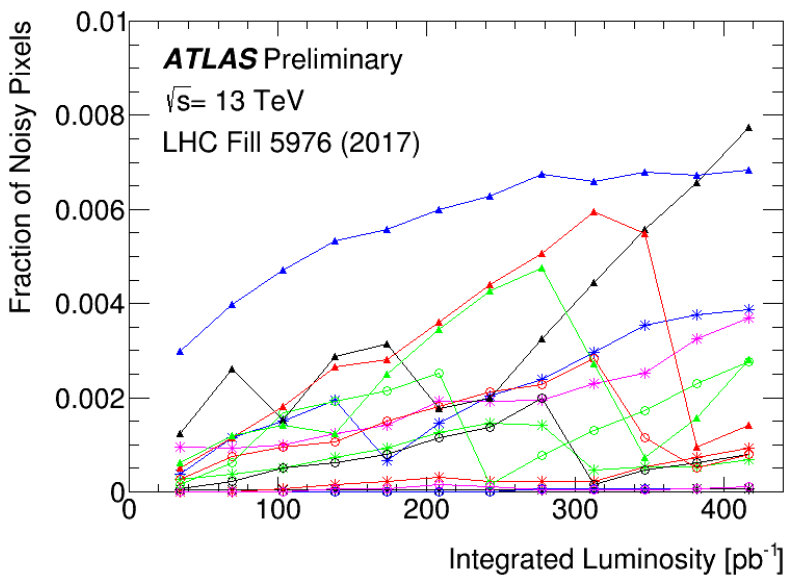




Noisy Pixels observation

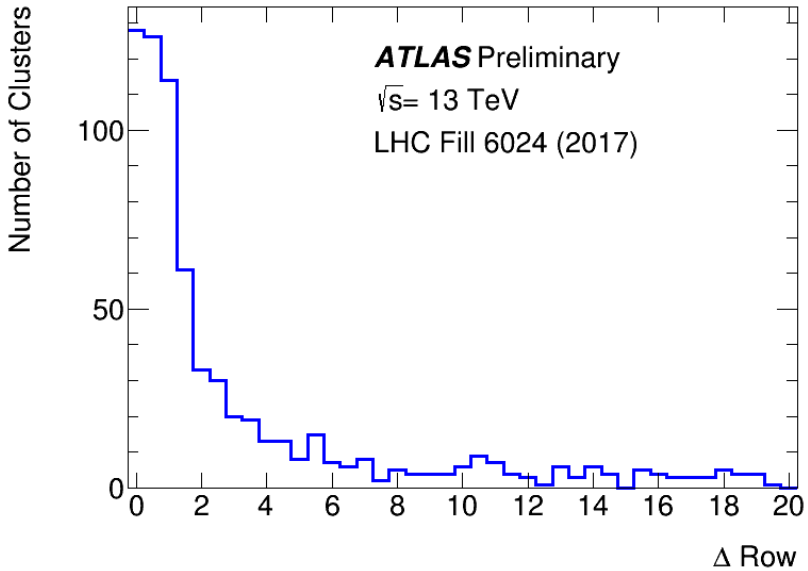
- Study of the fraction of pixels that get noisy in data-taking in 3Ds modules
- A **noisy pixel** is defined as a pixel that fires more than 300 times in a pre-defined integrated luminosity range
- A regular pixel has a probability to be noisy of 2.3×10^{-136} (5.4×10^{-134}) in 2016 (2017), under the previous definition
- An increase of the noisy pixels is observed in all the modules
- Reconfiguration actions restore the fraction of noisy pixels $\rightarrow$ confirmation that is configuration corruption effect
- Convolution of flips of various latches can cause a pixel to become noisy

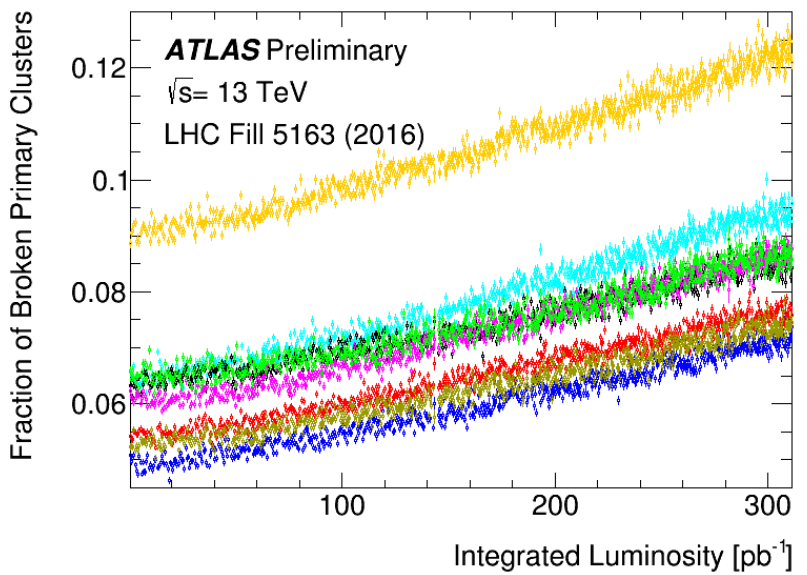




Broken Clusters

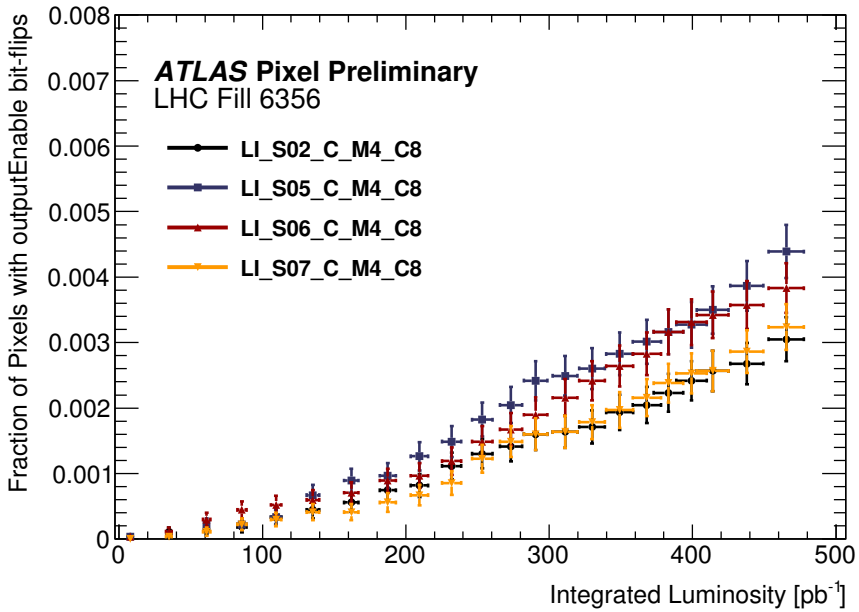
- Quiet pixels will lead to long clusters getting split by the clustering algorithm $\rightarrow$
- **broken clusters** $\rightarrow$ two clusters with 1-pixel gap along z-direction and $\Delta_{Row} < 3$
- With Δ_{Row} the center-to-center cluster distance in $r - \phi$
- Flat combinatory background, number of broken clusters from Δ_{Row} fit.
- Linear increase with integrated luminosity, starting point depends on the number of disabled/dead pixels





Output enable bit flip

- The output enable bit flip with integrated luminosity, which corresponds to a $0 \rightarrow 1$ transition was checked disabling all pixels of some 3D modules at the beginning of a LHC fill
- The number of pixels that fire at the passage of a charged particle indicate a SEU-induced flip of hit-enable DICE latch
- The neighbouring sensor is used to find a period of time such that the probability of non-illuminating a SEU-enabled pixel is $< 10^{-6}$
- Fraction of enabled pixels increases with integrated luminosty



Readback of the latches

- The FE-I4 provides the functionality to read back the content of the DICE latches
- The readback is done by copying the latches content in the Shift Register (SR) for each Double Column and transmitting it back to the RODs
- Such procedure allows for checking the content of each of the 13 latches/pixel independently
- Direct comparison with the configuration saved in the database

- Read-back cannot be performed while a FE receives trigger signals
- Only 2 read backs for planars at the beginning and end of the run, where no radiation is present
- Intermediate point using 3D

Read-back possible mistakes

- Bit-flips on Rx lines probability: $< 10^{-7}$ (10 multiple read-backs). Checked both in test-area and in without beam
- Bit-flips on the SR in beam presence probability: $< 2 \times 10^{7}$ (5 multiple-read backs)

Expected behaviour of the latches content

- The amount of upsets as function of integrated luminosity is given by

$$N_1(\mathscr{L}) = N_1(0)e^{-\gamma\mathscr{L}} + \frac{\sigma_0}{\gamma} N_{pix}\left[1 - e^{-\gamma\mathscr{L}}\right] \qquad (1)$$

$$N_0 = N_{pix} - N_1 \qquad (2)$$

- with $\gamma = \sigma_0 + \sigma_1$, σ_i is the probability of bit-flip from state i, N_{pix} total number of pixels in a Front End (=26880) and $\mathscr{L}$ is the integrated luminosity
- Considering only the evolution of the pixels in a definite state transitions it simplifies to

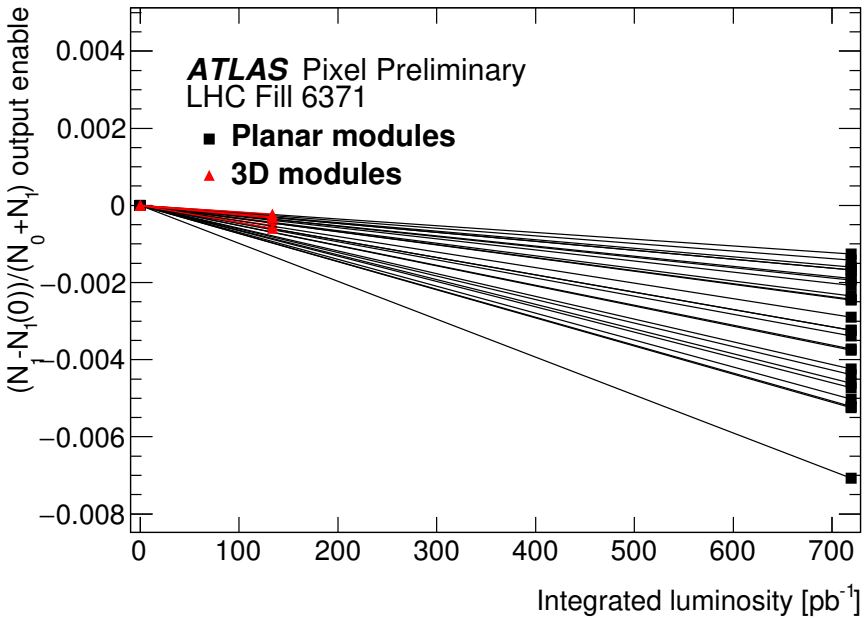
$$N_0(\mathscr{L}) = N_0(0)e^{-\sigma_0\mathscr{L}} \qquad N_1(\mathscr{L}) = N_1(0)e^{-\sigma_1\mathscr{L}} \qquad (3)$$

- Measurements of noisy and quiet pixels indicate that $\sigma_i\mathscr{L} << 1$, hence linear approx holds:

$$\sigma_i = \frac{N_i(0) - N_i(\mathscr{L})}{N_i(0)} \quad \text{with } i = 0,1 \qquad (4)$$

Readback of the pixel registers - output enable

- Read back results of the output enable latch
- The evolution depends on both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions, according to (1)
- Initially most of the pixels are enabled $N_1(0) \approx N_{pix}$
- Two readbacks for planars: before start of the collisions and after beam dump
- Intermediate point from 3D modules readback

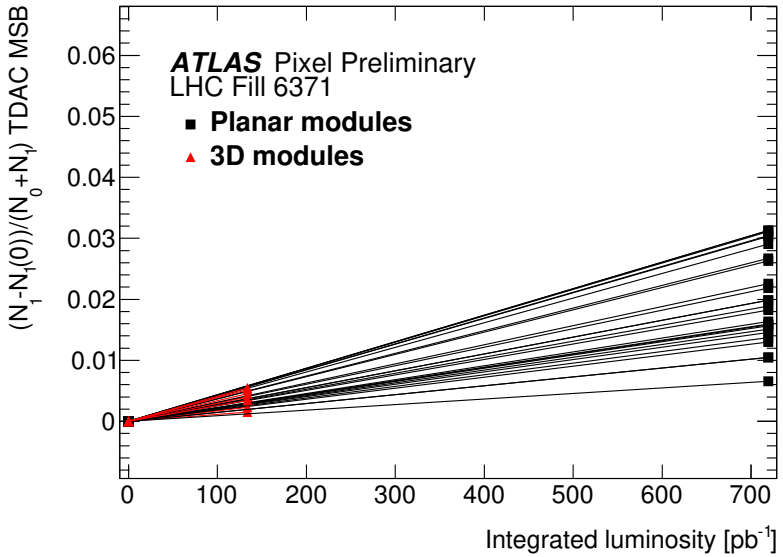


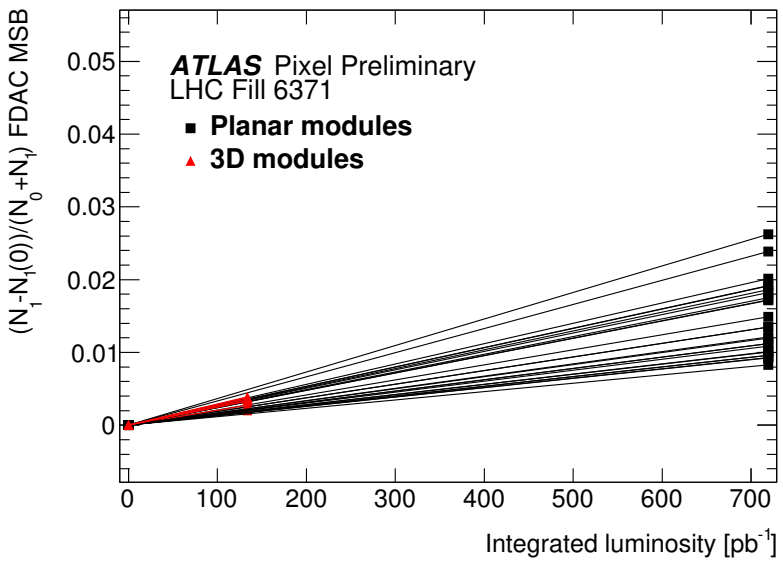
- Amount of output enable bit-flips compatible with amount of pixels getting disabled considering:
  - Module by module dependence
  - Quiet pixels can be due to TDAC bit-flips too

Readback of the pixel registers - TDAC and FDAC MSB

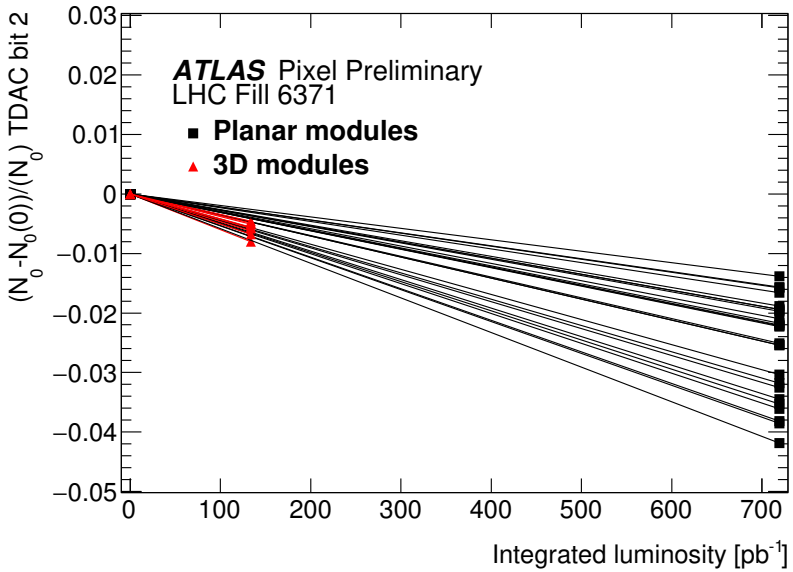
- Read back results of the most significant bits of TDAC and FDAC
- The evolution depends on both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions, according to (1), but also on the number of initial number of 0s (1s) actually present in the latches
- Two readbacks for planars: before start of the collisions and after beam dump
- Intermediate point from 3D modules readback

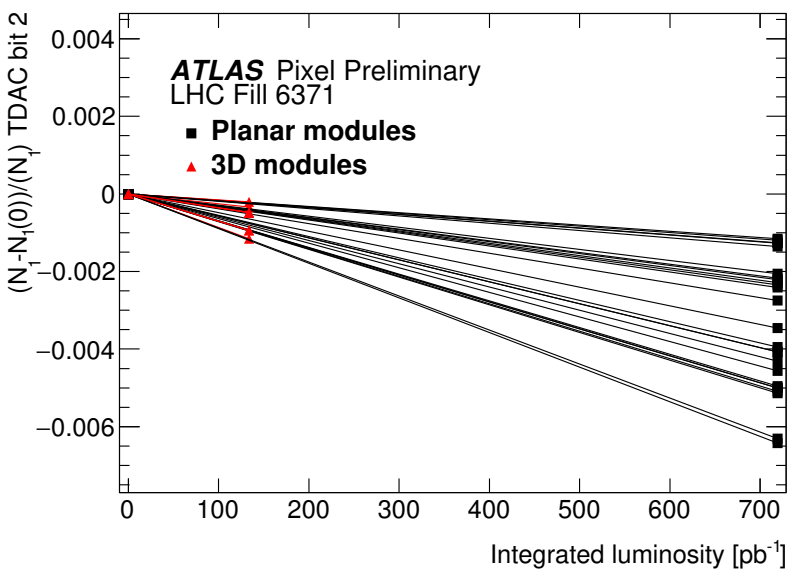
- The increase of the number of 1s stored in the latches is compatible with the observations of noisy pixels:
  - Noisy pixels are due to lowered pixel thresholds
  - The higher the TDAC, the lower the threshold
  - Highly noisy pixels are the result of the flip of the MSB of the TDAC





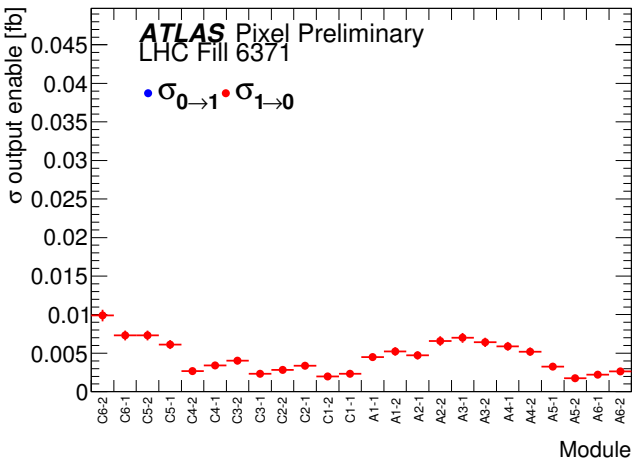
FEI4 Registers - Decoupled readback

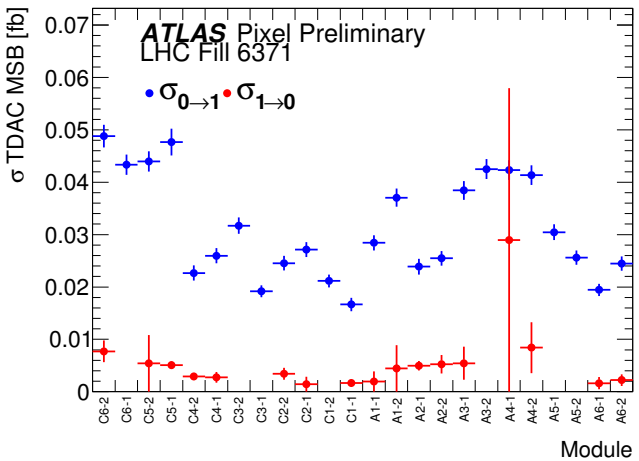


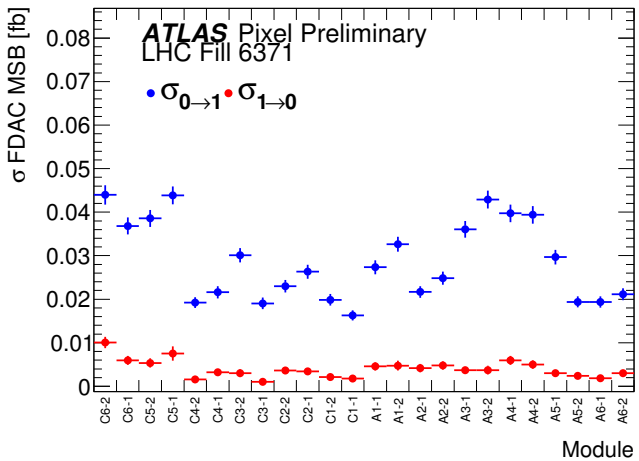


- Read back of the time-evolution of pixels in an initial definite state, which follows (3) and, in linear approx, (4)
- Two read-back before beam presence and after beam dump for planars and intermediate point for 3Ds
- Observed $\sigma_0 > \sigma_1$, compatible with increase of noisy pixels, while with output enable flips within module by module fluctuations

FEI4 Registers - transitions cross sections







- Measurement of the SEU transition cross-section for the various FE investigated
- Only reported for the latches most important for DAQ operations
- The output enable σ_0 has not been calculated as not enough 0s are stored in this latch for an accurate computation
- The $0\to1$ transition appears to be larger with respect to the $1\to0$ transition for all the front-ends investigated.
- No considerable latch-by-latch dependence is observed on these latches

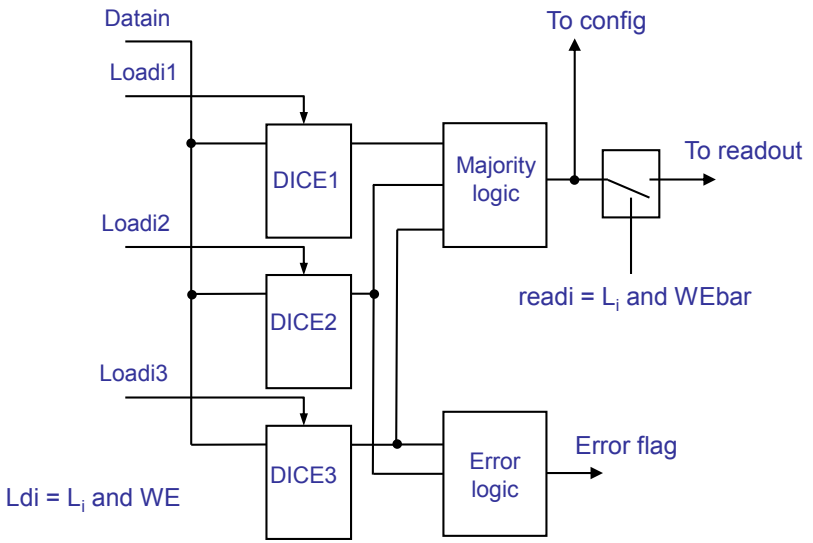
Conclusions

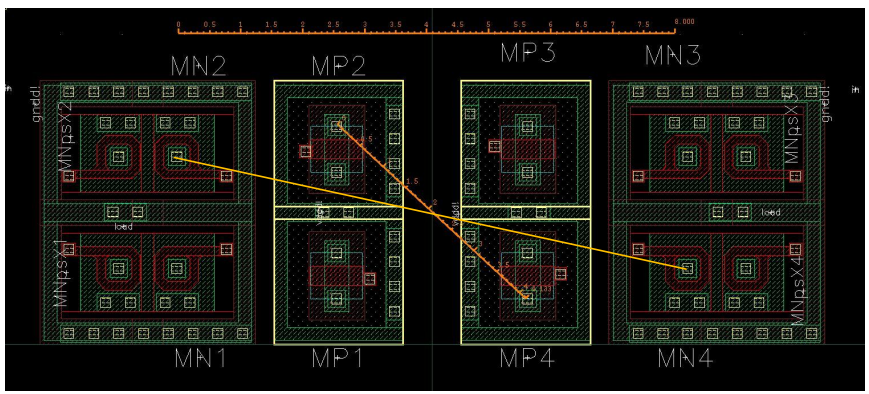
- During 2016 and 2017 LHC operated at very high luminosity where it is possible to study various radiation damage effects on the Pixel detector
- The study presented here shows the rate and effects of SEUs on global and pixel registers configurations for FE-I4
- Global configuration corruption leads to loss of occupancy and drops in the Low Voltage of the modules
- Pixel configuration corruption leads to noisy and quiet pixels that increase, in percentage, during data taking
- The global configuration is re-send to the modules every 5s during data taking. A similar mechanism of dynamic re-configuration of pixel registers is currently under development and will be used during 2018 data taking campaign

BACKUP

FE-I4 global configuration

- Global configuration is composed by 32 words of 16 bits - 512 bits
- Triple redundancy of the SEU-hard DICE latches
- Single DICE latch bit flips are signalled by error counter
- Measurement of the SEUs achieved by test beam with normally incident 24 GeV GeV protons
- Cross section: $2 \times 10^{-16} \mathrm{cm}^2$.
- Refs: CERN-2008-008, JINST 8 C02026, FE-I4B Manual





Latches evolution

- The number of 0s (N_0) and 1s (N_1) after a time T is given by:

$$\begin{cases} N_0(T) = N_0(0) + N_{1\to0}(T) - N_{0\to1}(T) \\ N_1(T) = N_1(0) - N_{1\to0}(T) + N_{0\to1}(T) \\ N_0(T) + N_1(T) = N_0(0) + N_1(0) = N_{pix} \end{cases}$$

  where $N_{i\to j}(t)$ is the number of pixels that transitioned from the bit value i to the bit value j and $N_{pix} = 26880$.

- The amount of $i \to j$ transitions per time unit is given by:

$$dN_{1\to0}(t) = \alpha_1(t)N_1(t)dt, \quad dN_{0\to1} = \alpha_0(t)N_0(t)dt$$

  where $\alpha_1(t)$ and $\alpha_0(t)$ are the probability that the SEU happens and can be written as

$$\alpha_k(t) = \sigma_k L(t) \qquad k = 0, 1$$

  with $L(t)$ being the instantaneous luminosity.

Latches Evolution

- We obtain:

$$\begin{cases} \dot{N}_0(t) = \sigma_1 L(t) N_1(t) - \sigma_0 L(t) N_0(t) \\ \dot{N}_1(t) = \sigma_0 L(t) N_0(t) - \sigma_1 L(t) N_1(t) \end{cases}$$

- Using $N_0 + N_1 = N_{pix}$ we have :

$$\dot{N}_1 = \left[\sigma_0 N_{pix} - (\sigma_0 + \sigma_1) N_1\right] L(t)$$

and defining $\tilde{N}_1 = N_1 - \frac{\sigma_0 N_{pix}}{\sigma_1 + \sigma_0}$ and and $\gamma = \sigma_0 + \sigma_1$ we have

$$\dot{\tilde{N}}_1 = -\gamma \tilde{N}_1 L(t)$$

which is easily solvable into

$$\tilde{N}_1 = A e^{-\gamma \mathcal{L}(t)}$$

with $\mathcal{L}(t)$ being the integrated luminosity.

- This leads to

$$N_1(t) = N_1(0) e^{-\gamma \mathcal{L}(t)} + \frac{\sigma_0}{\gamma} N_{pix} \left[1 - e^{-\gamma \mathcal{L}(t)}\right]$$

$$N_0(t) = N_{pix} - N_1(t)$$