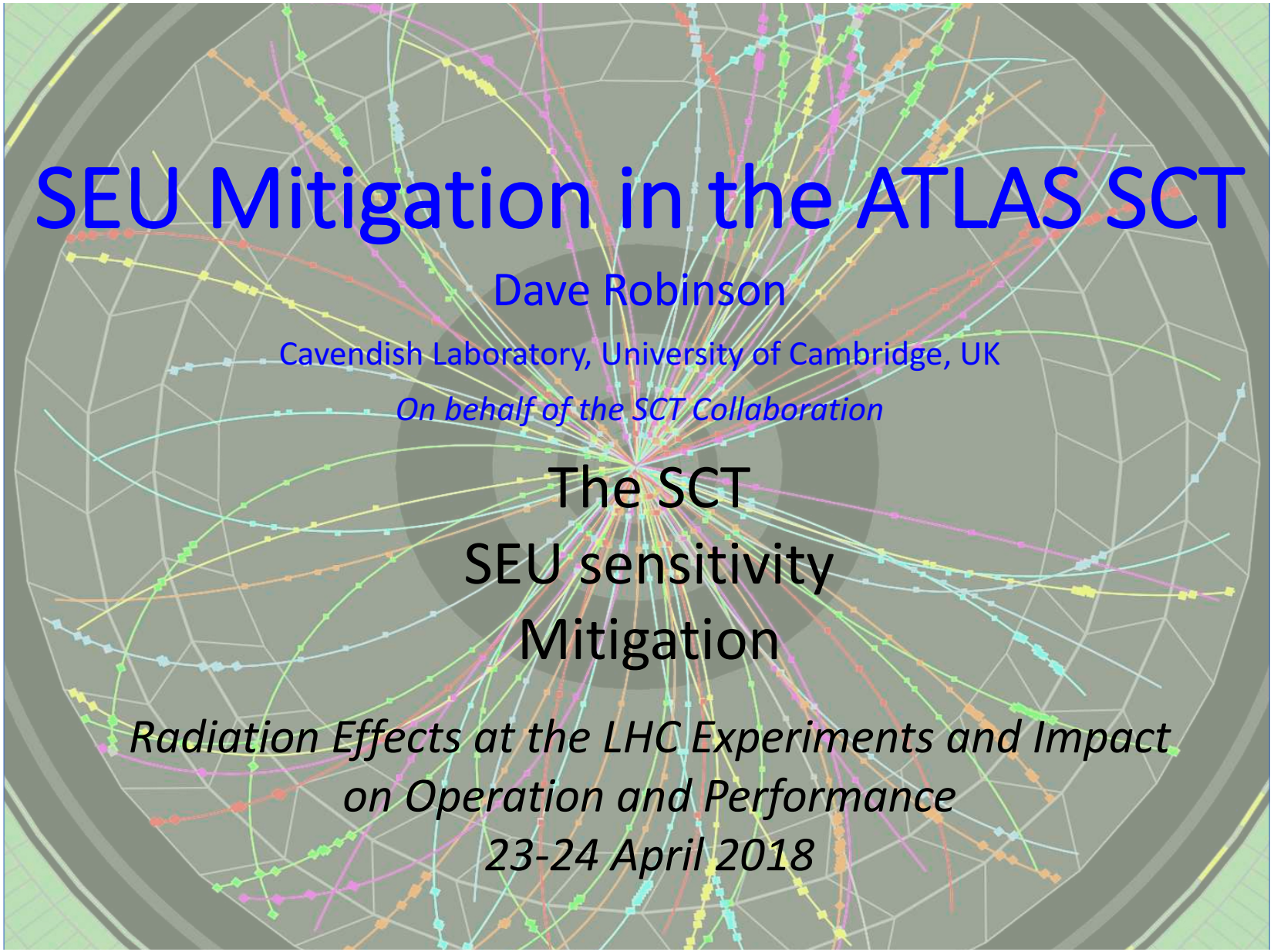

SEU Mitigation in the ATLAS SCT

Dave Robinson

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On behalf of the SCT Collaboration

The SCT

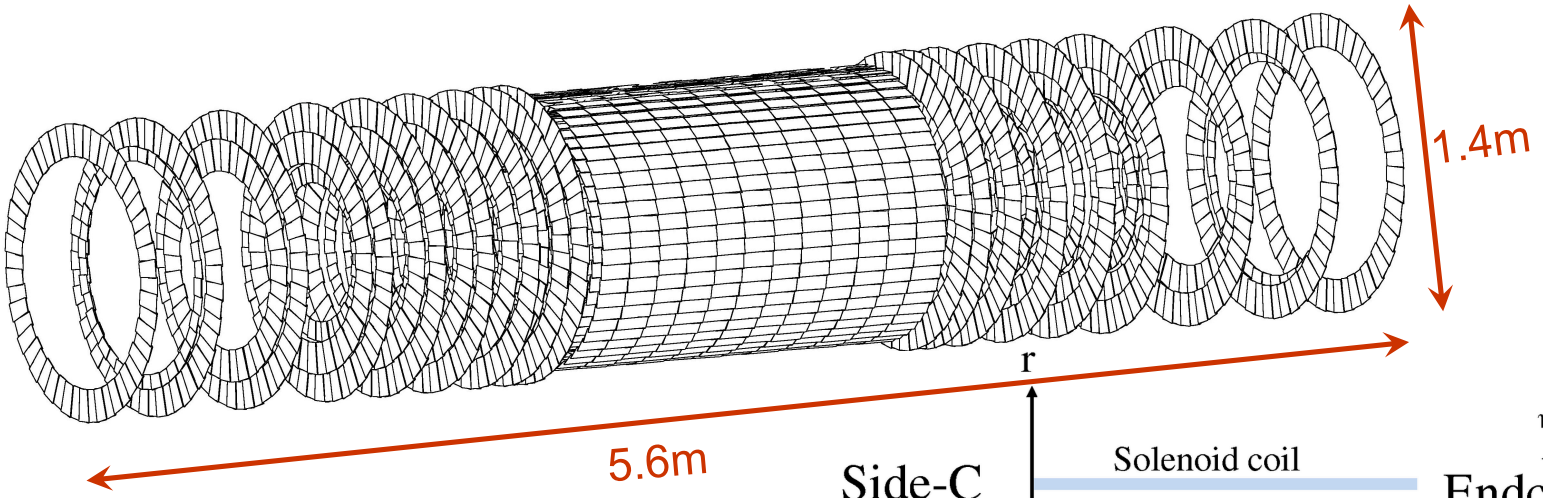
SEU sensitivity

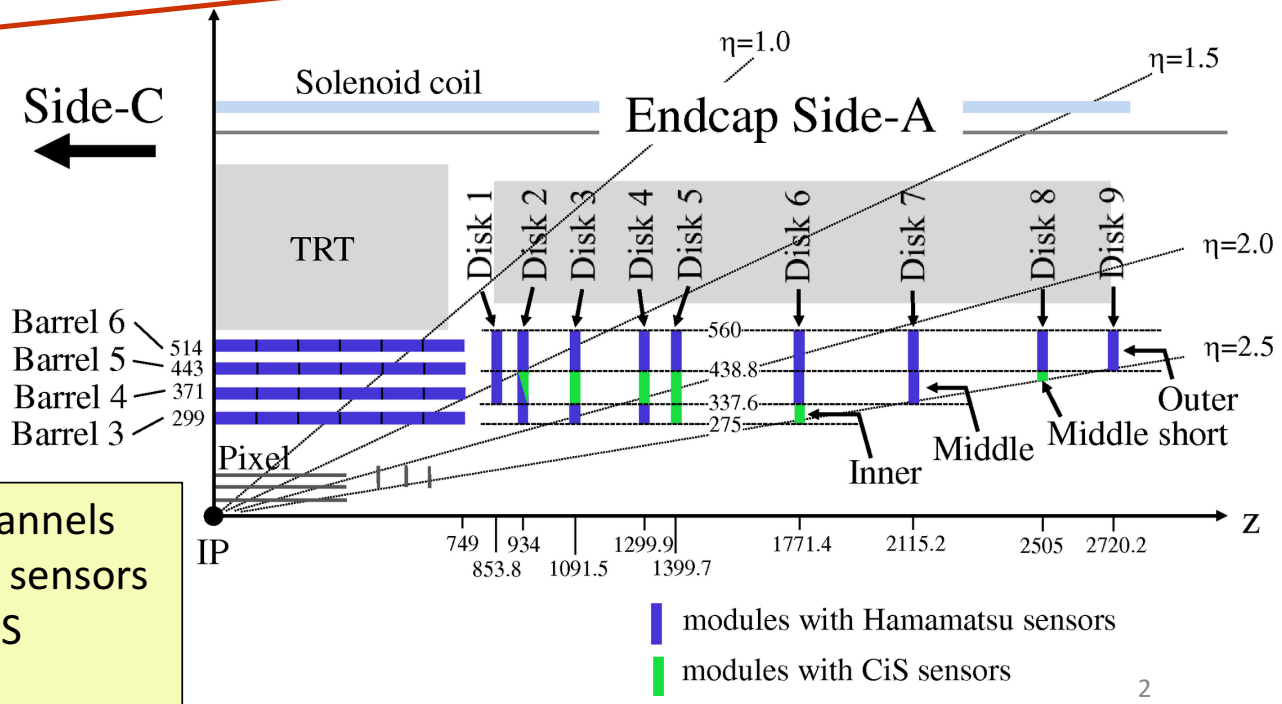
Mitigation

Radiation Effects at the LHC Experiments and Impact on Operation and Performance

23-24 April 2018

The Semi Conductor Tracker (SCT)

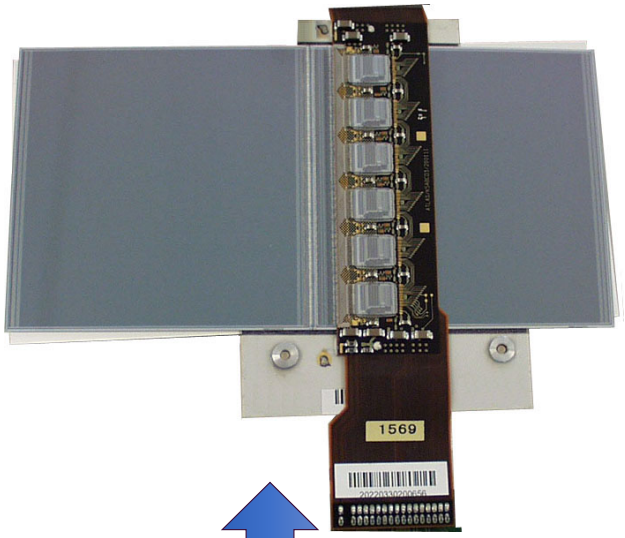




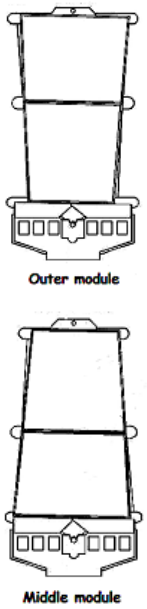
- 61 m^2 of silicon with 6.2 million readout channels
- 4088 modules assembled with HPK and CiS sensors
  - Barrels are all HPK, 17% of EndCaps use CiS
- C_3F_8 evaporative cooling

The SCT Modules

- Back-to-back sensors, glued to highly thermally conductive substrates for mech/thermal stability, wire-bonded to form ~12cm long strips
- 40mrad stereo angle between strips on opposite sides
- 6 FE chips (ABCD3TA) on each side
- One command stream, two data streams
- Nominal HV 150V (standby 50V)

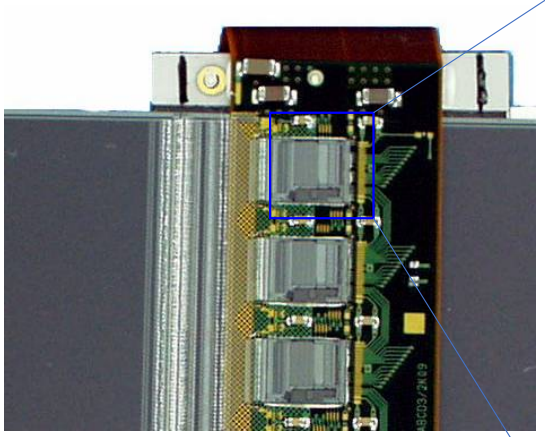


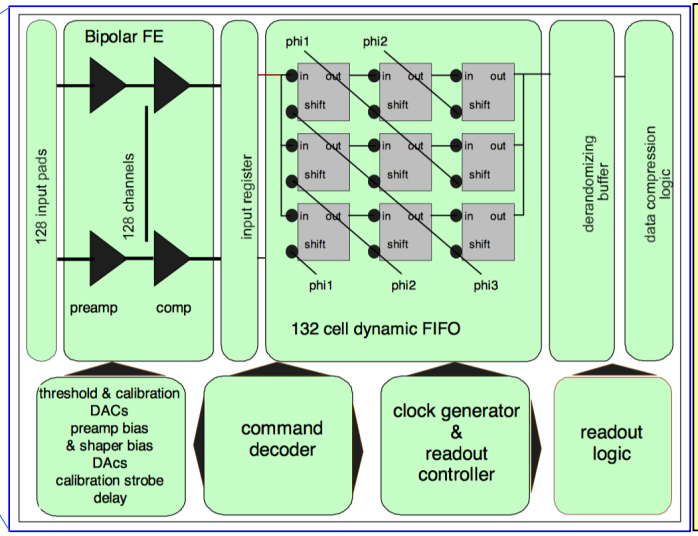
- 2112 barrel modules
- one shape



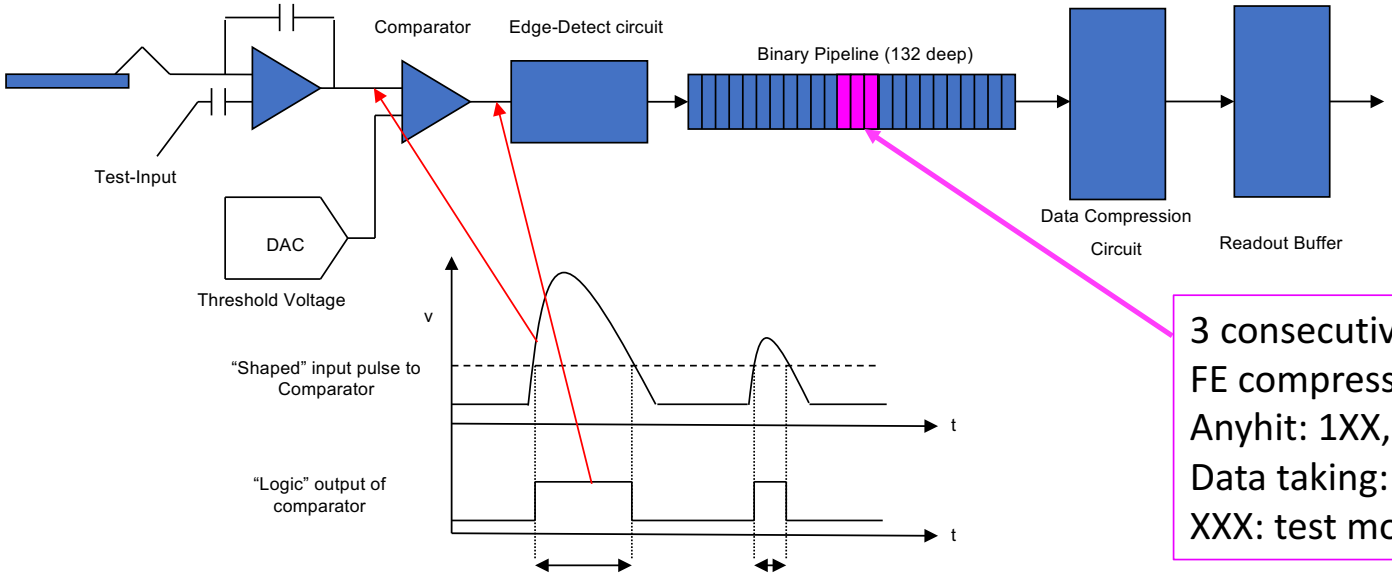
- 1976 end-cap modules
- 3 shapes

The ABCD3TA ASICs

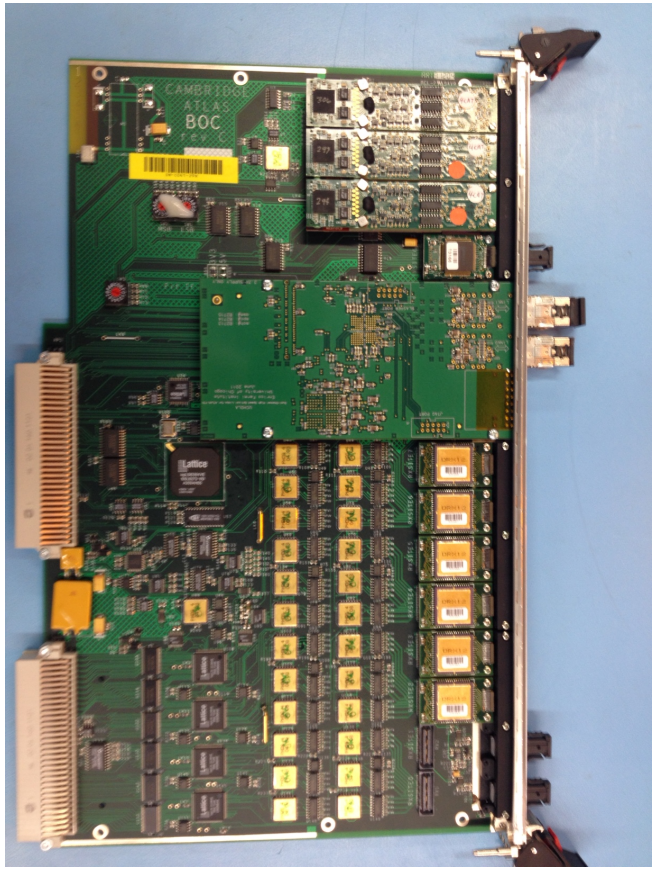


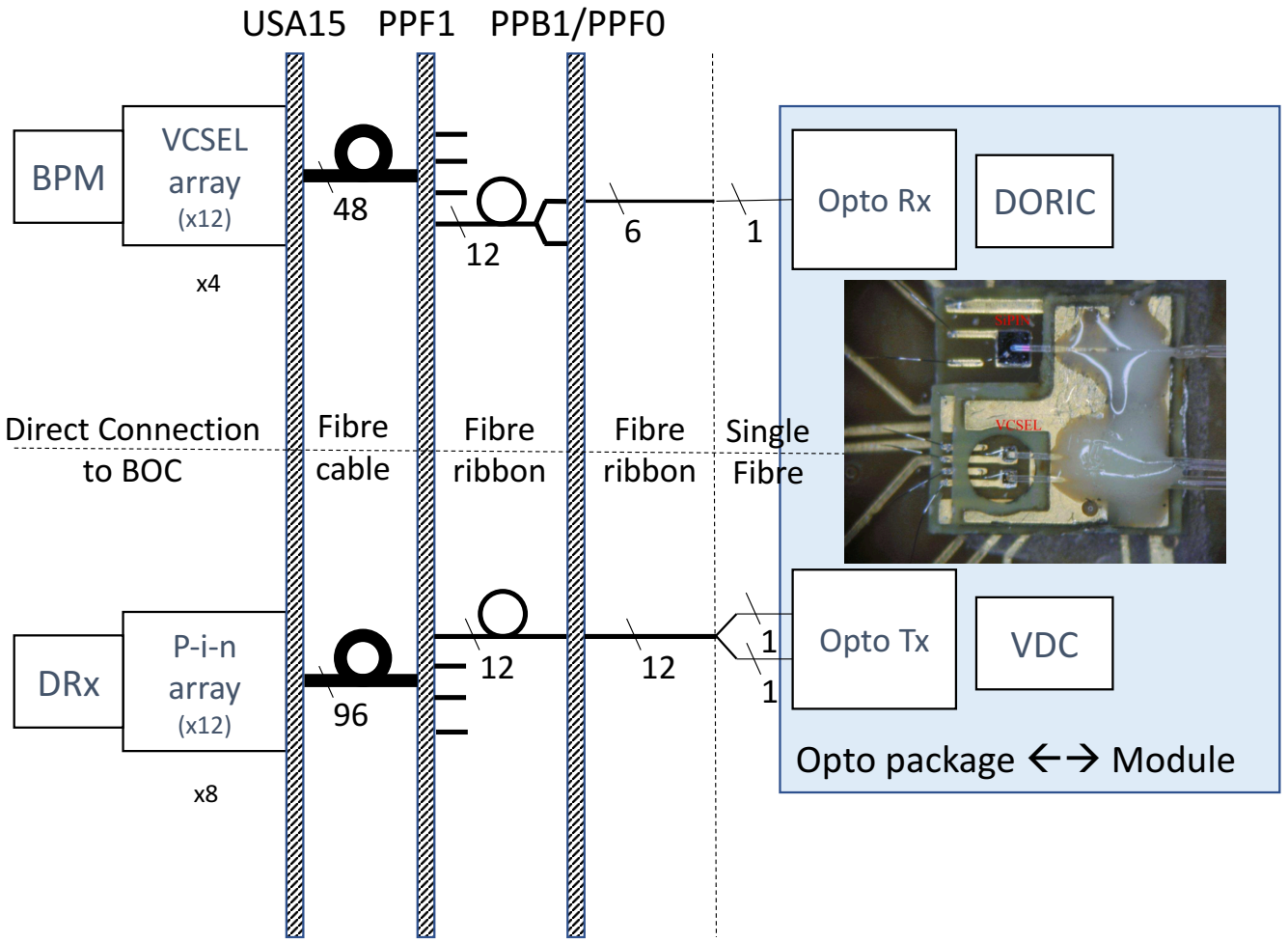


- 128 channel ASIC with binary architecture fabricated using DMILL technology
  - BiCMOS process with min 0.8µm gate width
- Glued to hybrid (Cu/polyimide flex circuit)
- 20ns front end shaping time
- 4-bit trim DAC/channel for threshold adjustment, with 2-bit range setting ensures minimal spread in discriminator threshold

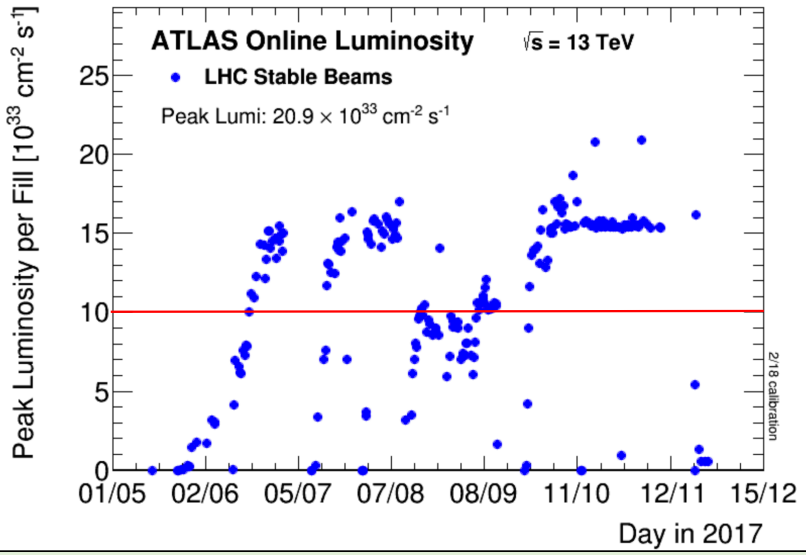


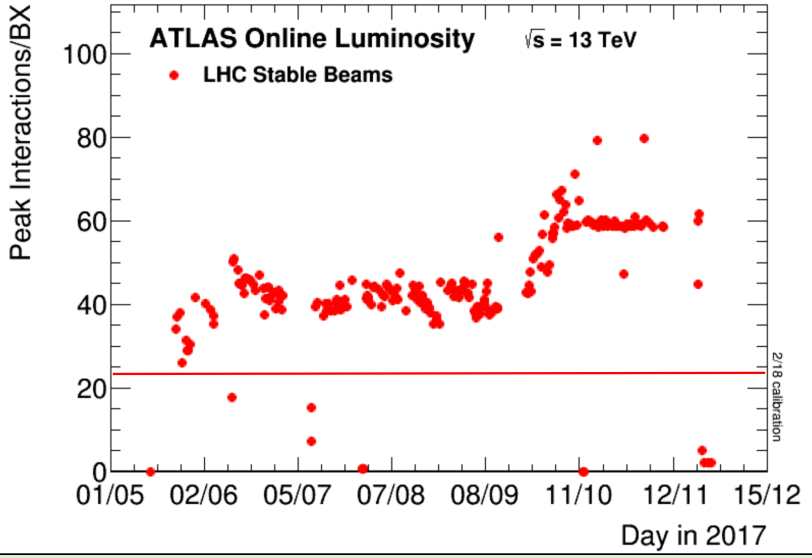
3 consecutive time-bins sampled
FE compression logic:
Anyhit: 1XX, X1X, XX1
Data taking: X1X, 01X for 50s, 25ns bunches
XXX: test mode




USA15
PPF1
PPB1/PPF0
BPM
VCSEL array (x12)
x4
48
12
6
1
Opto Rx
DORIC
Direct Connection to BOC
Fibre cable
Fibre ribbon
Fibre ribbon
Single Fibre
DRx
P-i-n array (x12)
x8
96
12
12
1
1
Opto Tx
VDC
Opto package ←→ Module

SCT Operating Conditions at the LHC





- The ATLAS tracker was designed for a nominal luminosity of $1x10^{34}cm^{-2}s^{-1}$ with a $<\mu>$ of ~23 at 70kHz L1 rate
- This has been routinely exceeded since 2016, with ATLAS striving for a L1 trigger rate of 100Hz to fully exploit physics potential
- Three distinct challenges:
  - Online data processing, bandwidth limitations, radiation damage mitigation

Radiation Damage – Impact on SCT Operations

Static Configuration updated as needed

- Leakage Currents
  - Increased by ~5 orders of magnitude since start of Run-1
  - Trip limits adjusted after several months
- Depletion Voltage
  - Type inversion already in innermost barrel
  - We still operate with nominal 150V HV
- Noise & gain
  - Largely stable, regular calibrations
- ABCD Shaper/preamp current
  - Signal amplification and shaping – still with default settings!
  - Optimise noise/gain while scan shaper and preamp DAC settings
- Chip thresholds
  - Channel trim adjustments every ~few weeks

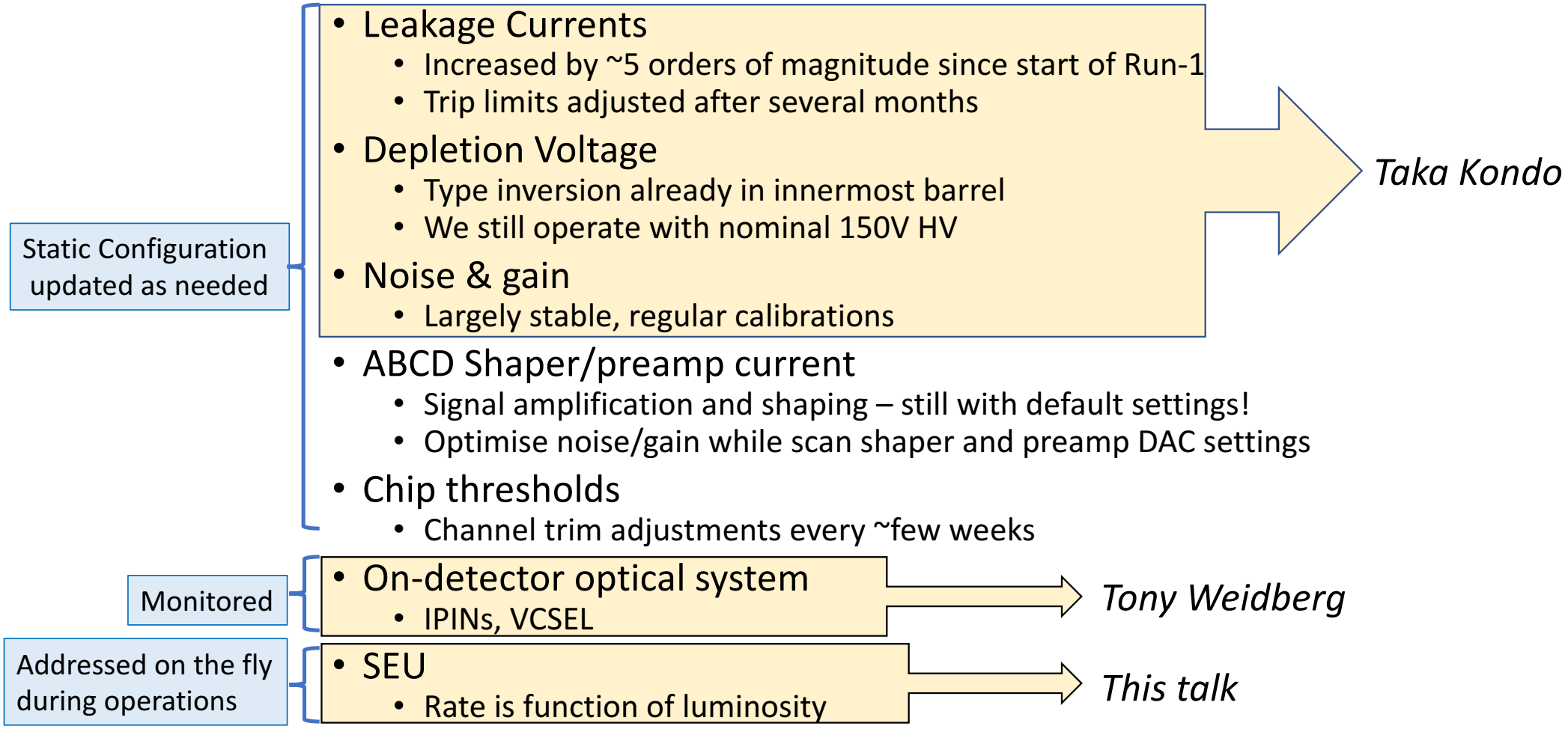
Monitored

- On-detector optical system
  - IPINs, VCSEL

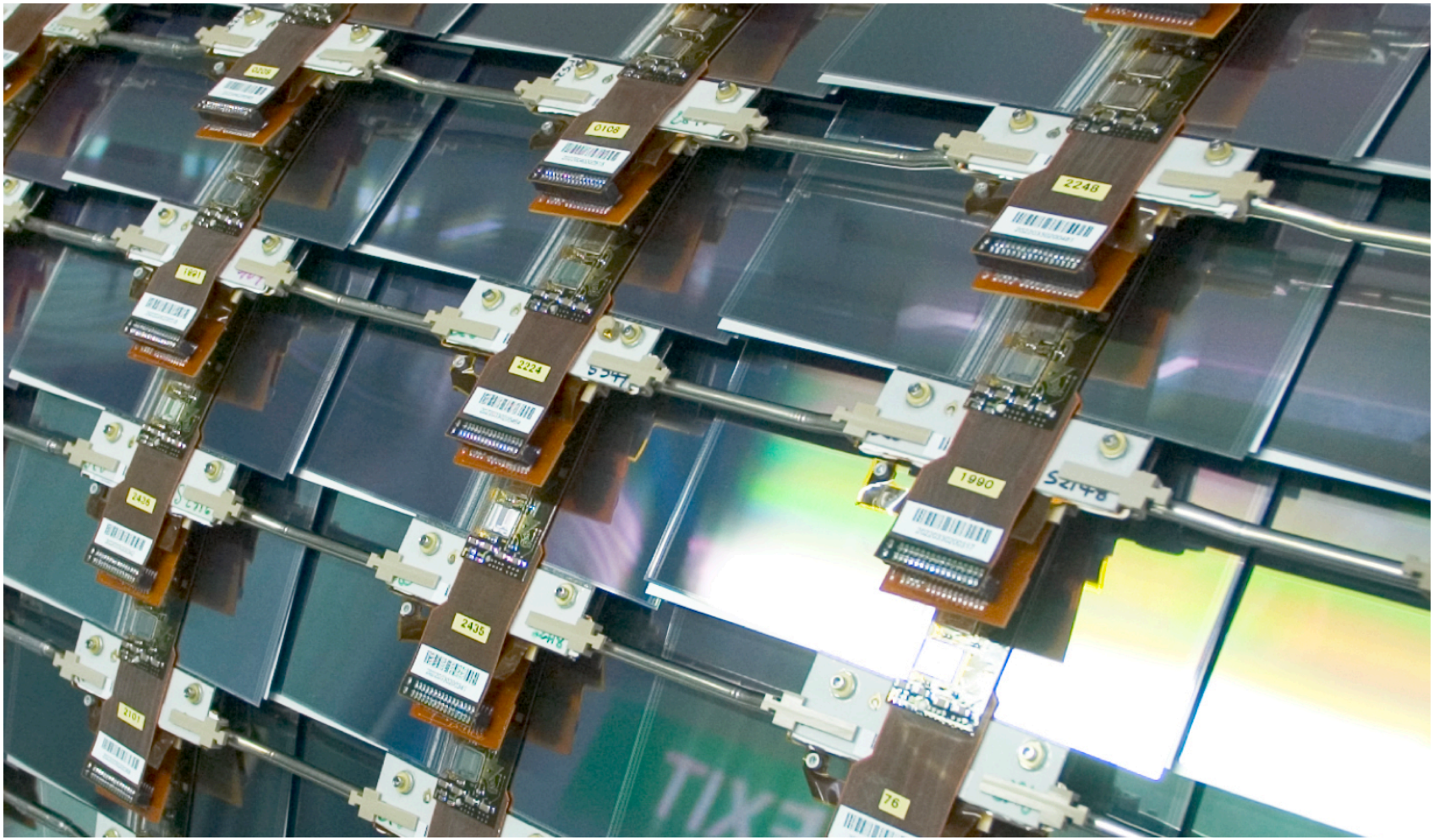
Addressed on the fly during operations

- SEU
  - Rate is function of luminosity

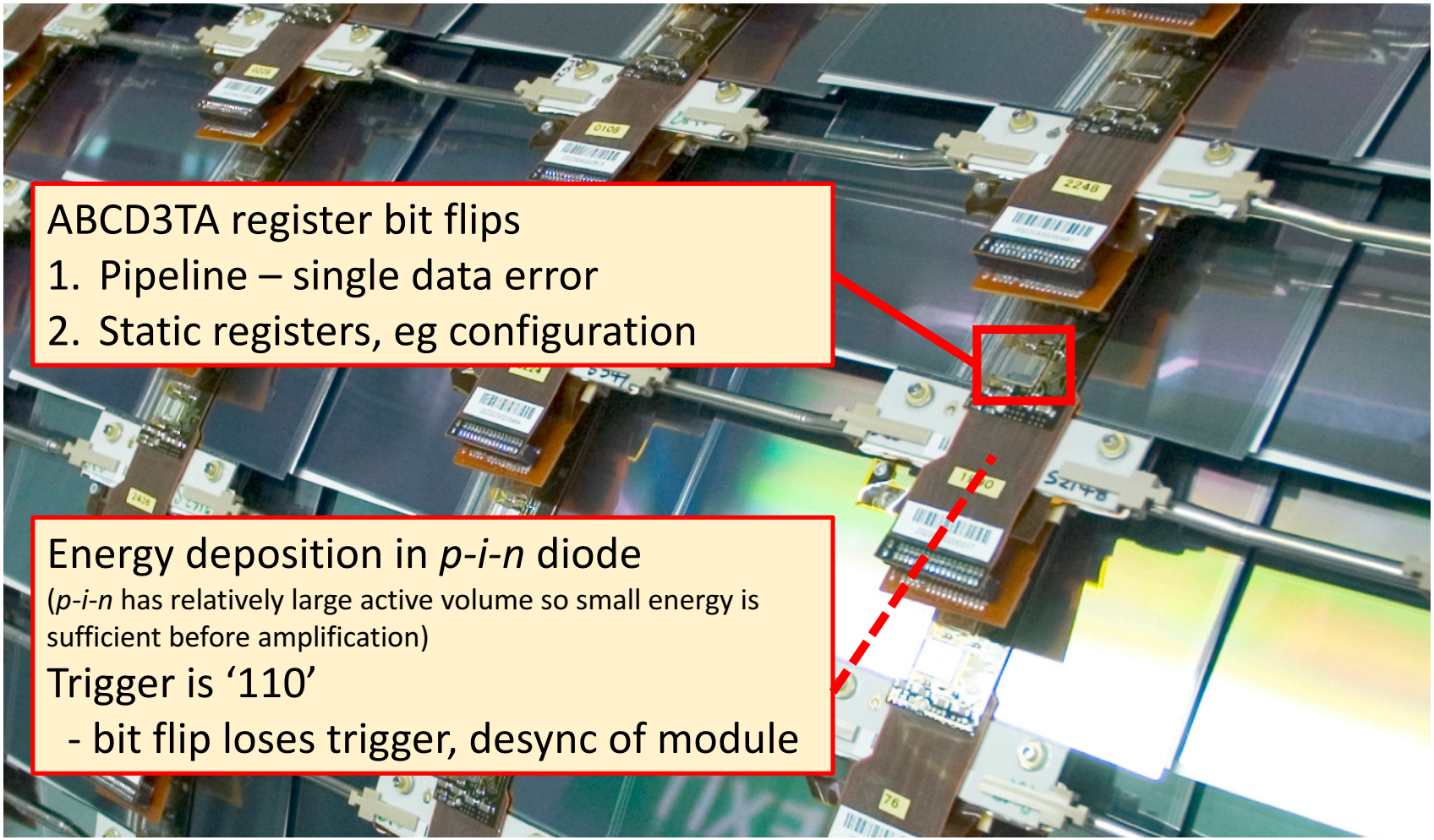
Radiation Damage – Impact on SCT Operations



SCT SEU vulnerabilities



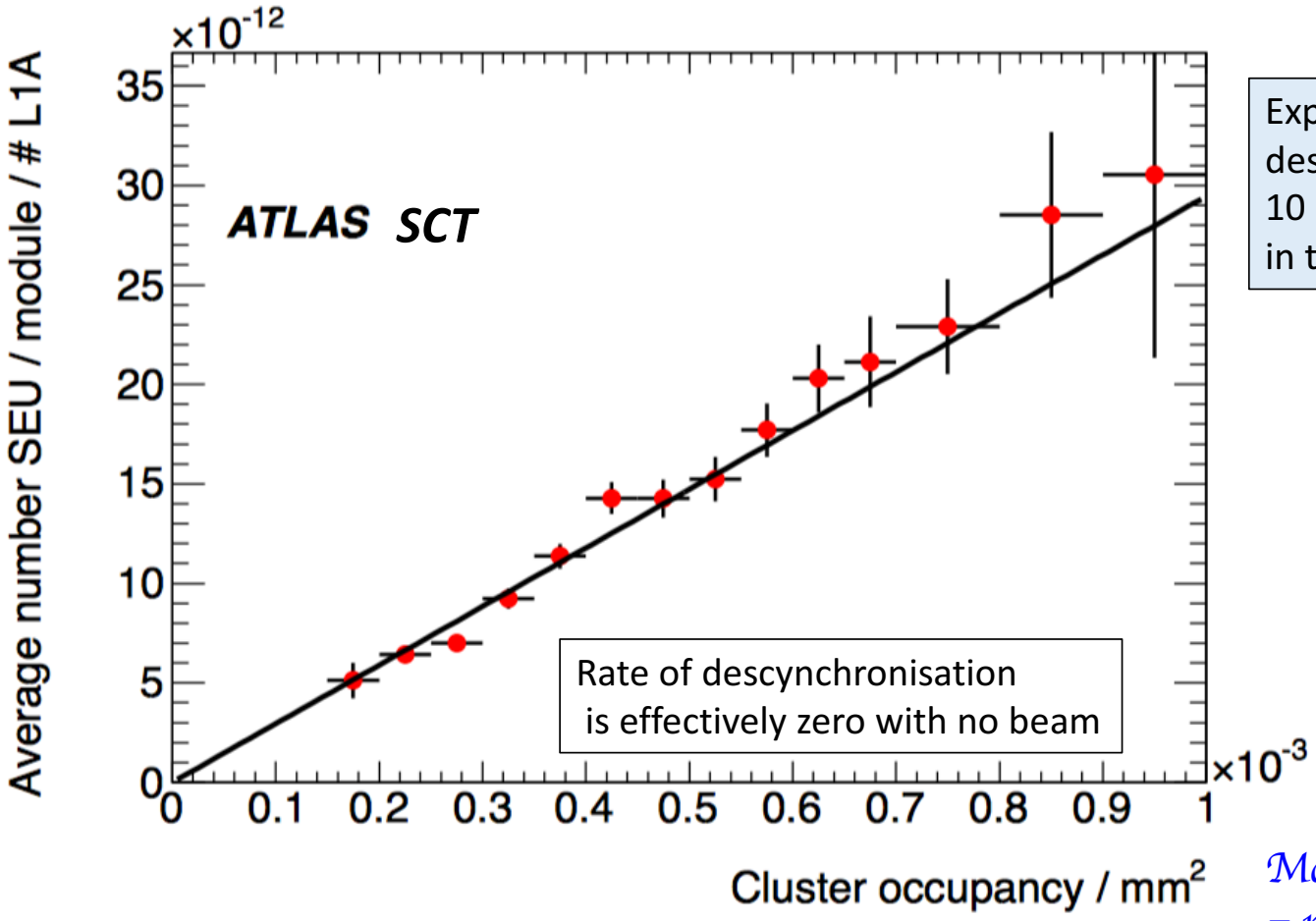
SCT SEU vulnerabilities



Evidence for module desynchronisation by SEU

"Smoking gun" is that desync error rate should scale with particle flux…

Desync count using spread in occupancy over many runs



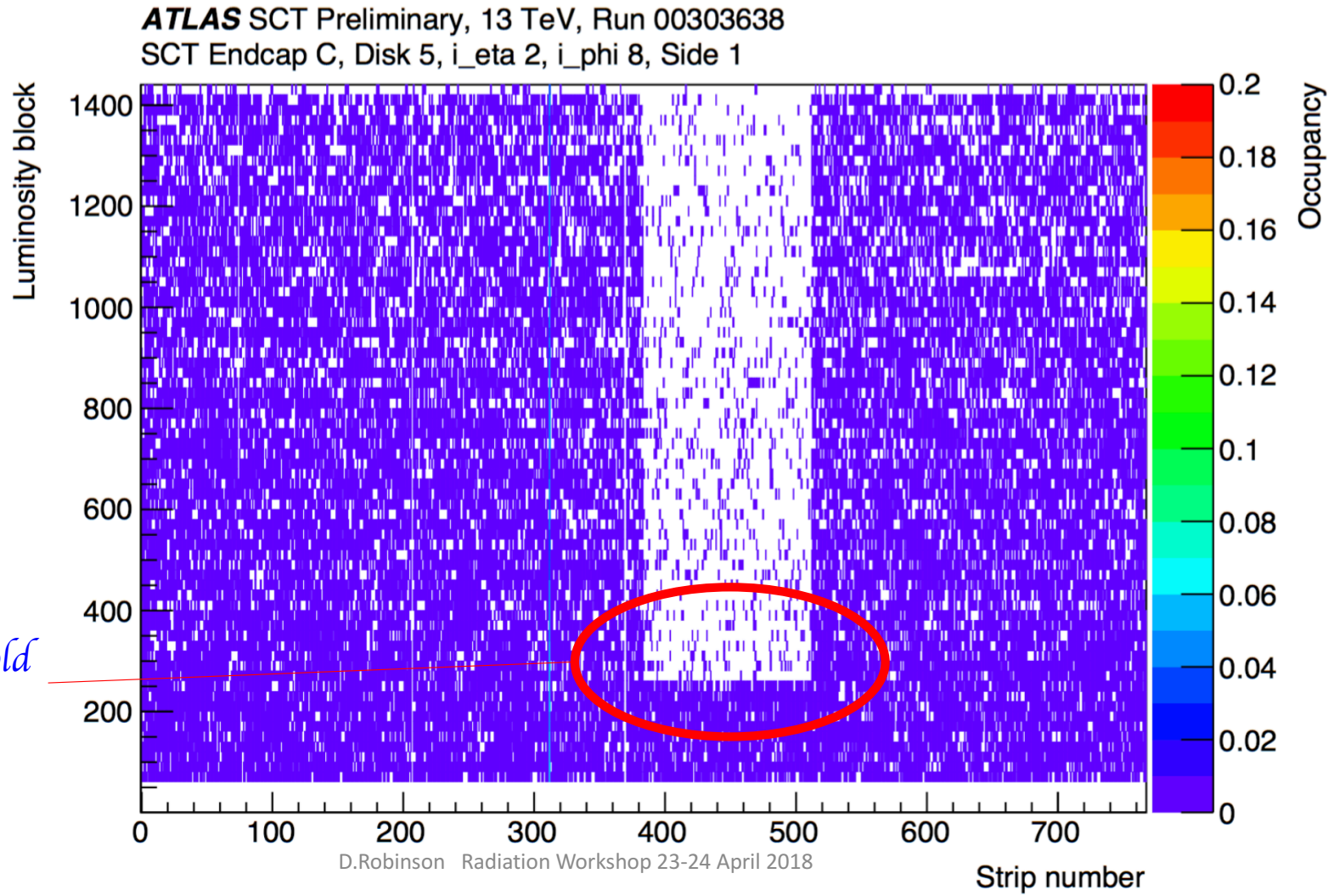
Expect ~100s of SEU-induced desynchronisations per 10 hour run @90kHz L1 rate in typical high lumi fill

Module occupancy/area = proxy for particle flux

Evidence for chip configuration bit flip by SEU

Luminosity block = 1 minute interval

Onset of high threshold for chip 4 (383-512)



Expected SEU Rates

derived from test beam studies

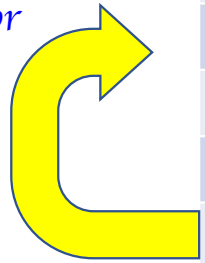
When SCT was first being designed, we were not aware of SEUs and their potential to disrupt data taking!

- P-i-n diodes in SCT opto packages
  - Test beam studies *Nucl. Instrum. Meth. A 481 (2002) 575.*
    - Threshold for energy deposition @ Ipin=100uA for SEU is 2.3MeV
    - SEU x-section measurable for 14.1 MeV neutrons, 450 MeV protons and 300-450 MeV pions
  - Prediction vs measurement for ~7fb^{-1} data sample : 1900 vs 2405
    - *2014 JINST 9 C01050*
- ABCD configuration registers
  - Test beam studies *Nucl. Instrum. Meth. A 552 (2005) 292*
    - Study rate of bit flips with 200MeV pions and 24 GeV protons
  - For 3x10^{14} hadrons.cm^{-2}
    - 3x10^{-6} SEUs/s/module, ie few hundred bit flips per typical 10 hour run
  - Factor ~3 discrepancy between predicted (test-beam) and measured rates
    - based on study of bit flips 1→0 in threshold registers, from count of noisy chip rate

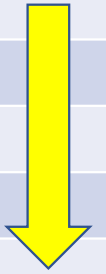
SEU Mitigation – module desynchronisation

- We sample online HLT-triggered ATLAS data
  - Using standard monitoring framework within ATLAS TDAQ
    - would be better to trap events in the ROD, but...
- Continuously monitor and publish SCT flagged errors
- Watchdog requests reconfiguration of indiviual module(s) with errors

Repeat if necessary with reset or power cycle



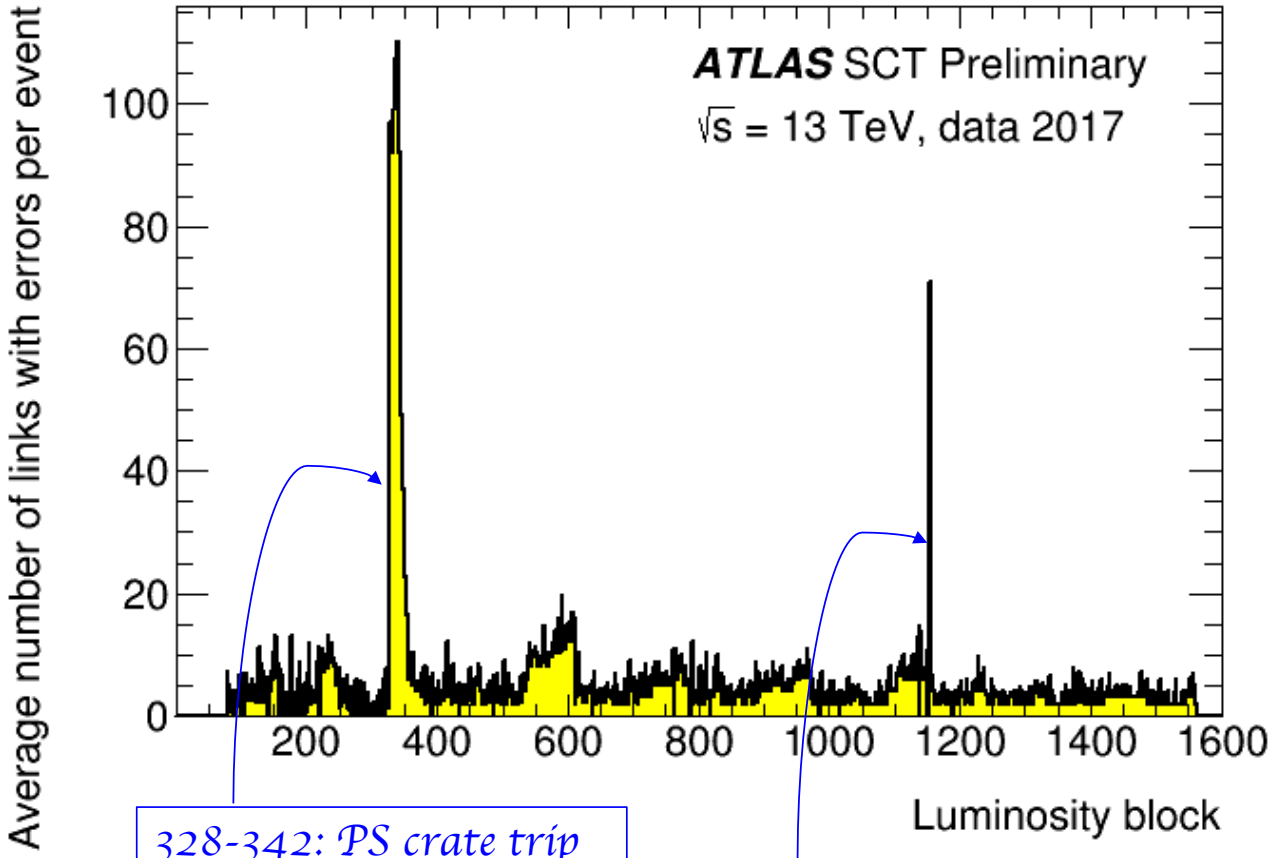
Action	Error(s) on module data link
Normal data taking	None
SEU provokes desync	L1 mismatch
Mask off link at ROD level	Timeout/mask (empty data)
Reconfigure module	Timeout/mask (empty data)
Re-enable mask	BCID mismatch, L1ID mismatch
Normal data taking	None (after next BCR and ECR respectively)



About 10-20s

Same mechanism for non-SEU configuration issues…

Suppression of link errors by module recovery



- 8176 data links in total
- Module recovery restricts count to <~5 typically at any one time
- Without module recovery, we observe increment of ~1 link errors per LB
  - ~50-60 per hour, depending on delivered luminosity
- SEU is cause of a fraction of these

Impact of bit flips on ABCD configuration

Threshold/Calibration DACs

8-bit threshold (15:8)	8-bit calibration (7:0)	High noise, or low efficiency

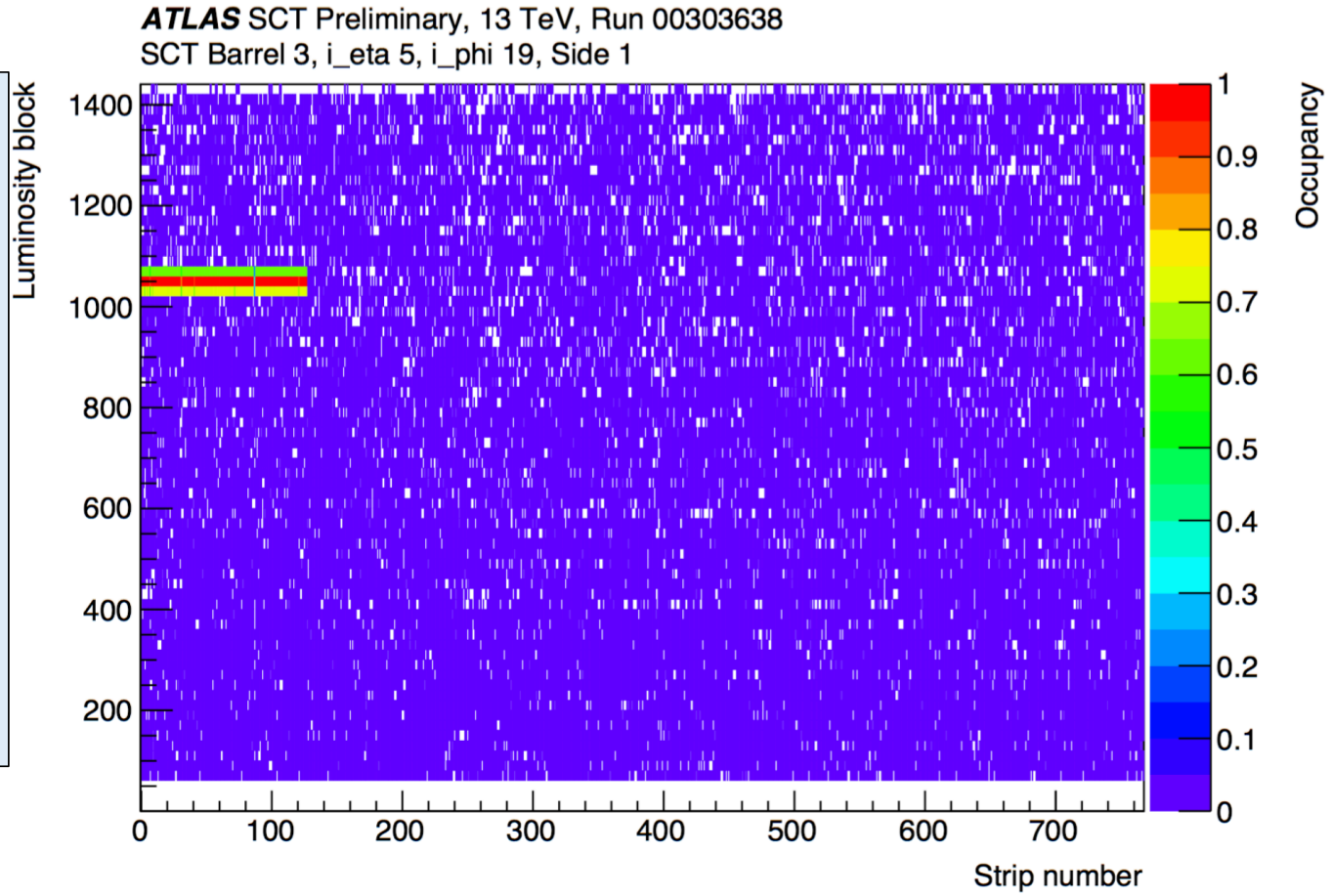
Configuration Register

Bit	Name	Function	
0-1	Readout Mode	Selects the data compression Criteria (see Table 3.6a)	FE data compression: Anyhit, X1X, 01X, XXX
2-3	Cal_Mode<1:0>	Selects the Calibration code (see Table 3.11). The state of these two bits also determines which channels are tested when Test Mode is enabled.	
4-5	Trim DAC range <1:0>	Selects the range of the trim DAC (see Table 3.1a)	Channel by channel threshold spread
6	Edge_Detect	Enables the edge detection circuitry in the input stage is enabled.	
7	Mask	When this bit is set the input register is disabled and the contents of the mask register are routed into the L1 pipeline.	Invalid data
8	Accumulate	When this bit is set the Accumulate function is enabled.	Pipeline bit latched → 100% occupancy
9	Input_Bypass	This bit determines which set of token/data inputs are active.	Chip sequencing → loss of chip data
10	Output Bypass	This bit determines which set of token/data outputs are active.	
11	Master	When clear the chip acts as a Master providing the masterB input pin has be asserted. This bit is "ored" with the value on the "masterB" input. If the result is "0", the chip is placed into master mode. Otherwise, it is placed into slave mode.	
12	End	When set this bit configures the chip as the end of a readout chain.	
13	Feed_Through	When clear the chip outputs a 20MHz clock signal but only is the chip has been configured as a Master (see above)	20MHz clock if on Master
14-15	not used		

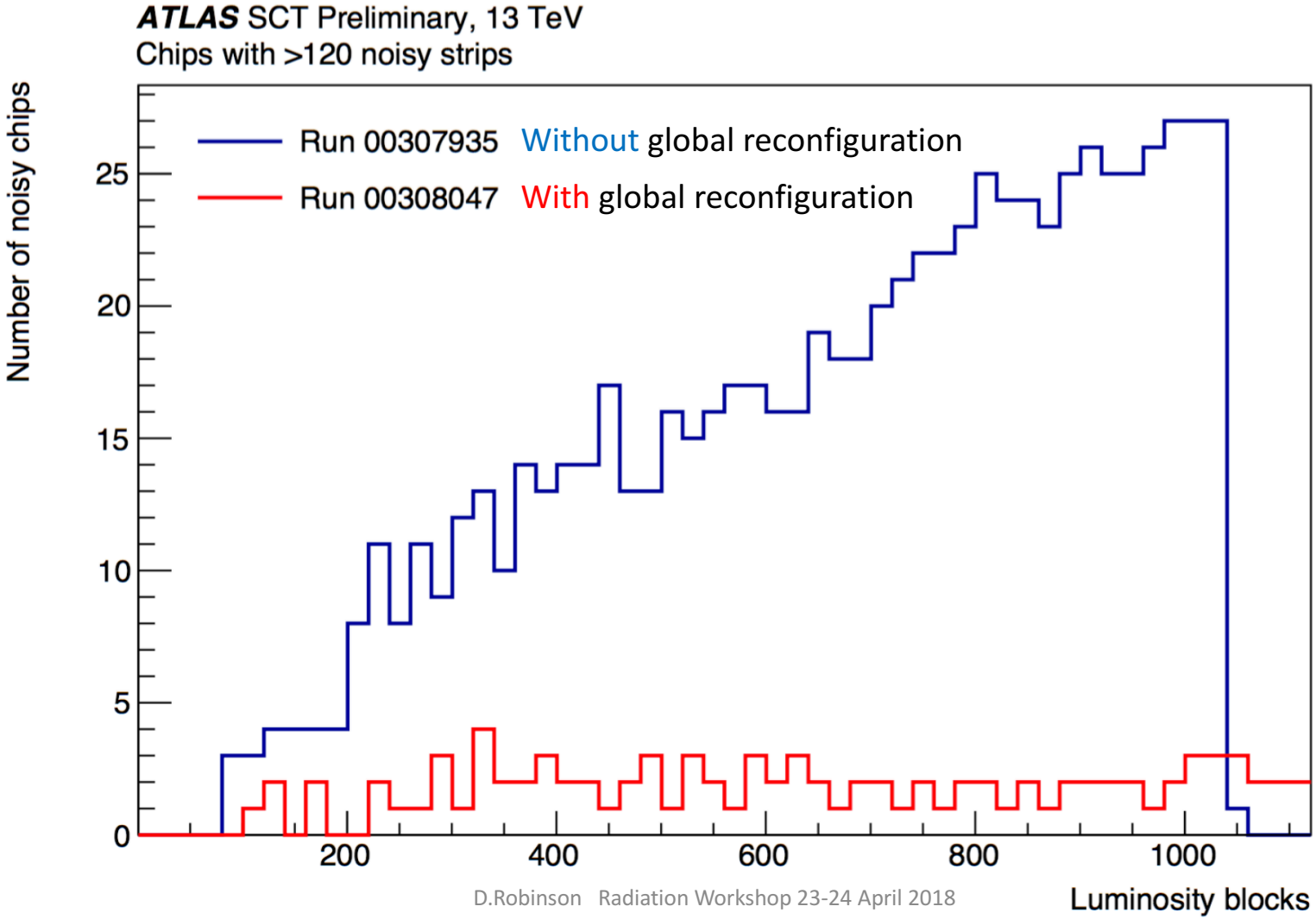
SEU Mitigation - ABCD

We issue a
Global Reconfiguration
of the SCT every N lumiblocks
(N currently set to 90)

Imposes dead time to ATLAS
for ~1.4 seconds
→ Overall impact on data
taking efficiency is negligible

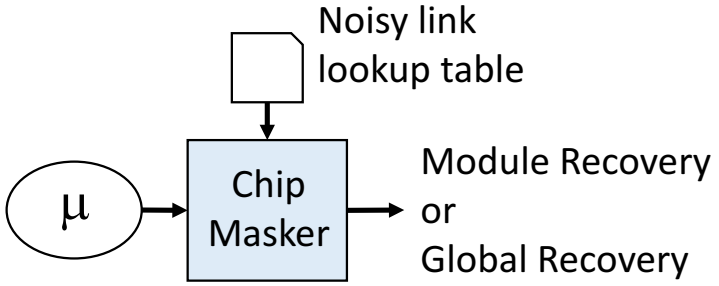


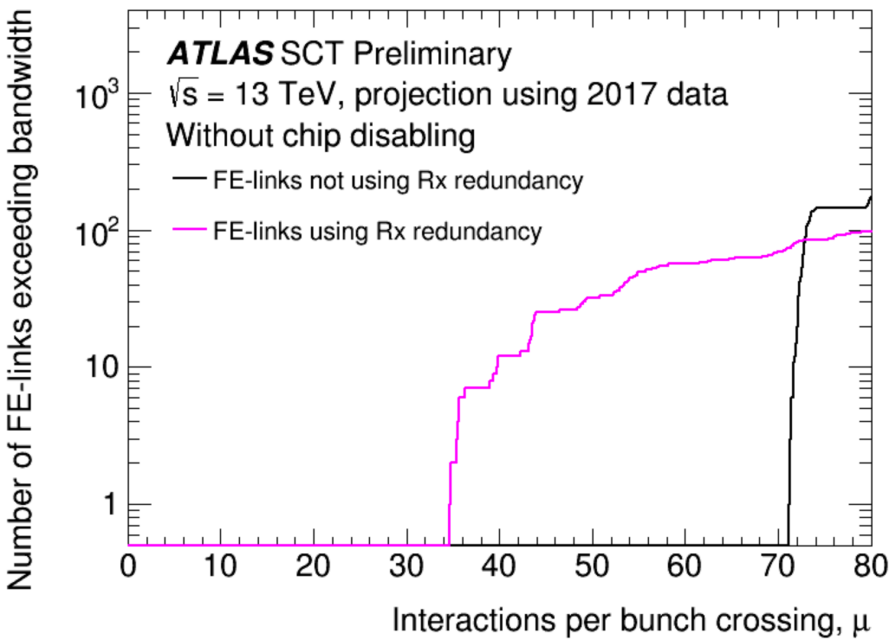
Suppression of SEU-induced ABCD misconfiguration by global recovery

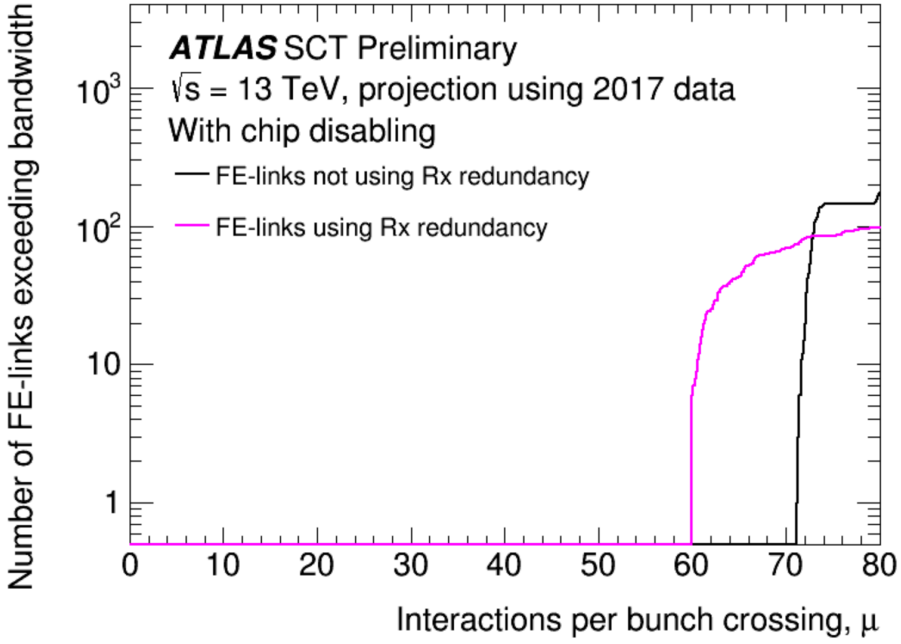


Dealing with bandwidth constraints

We use the same mechanism to dynamically mask ABCD chips on the fly (and flag masking in data), depending on published μ value
→ Mask up to ~0.6% of chips at <μ>=60
→ Maintains data flow within bandwidth limitations





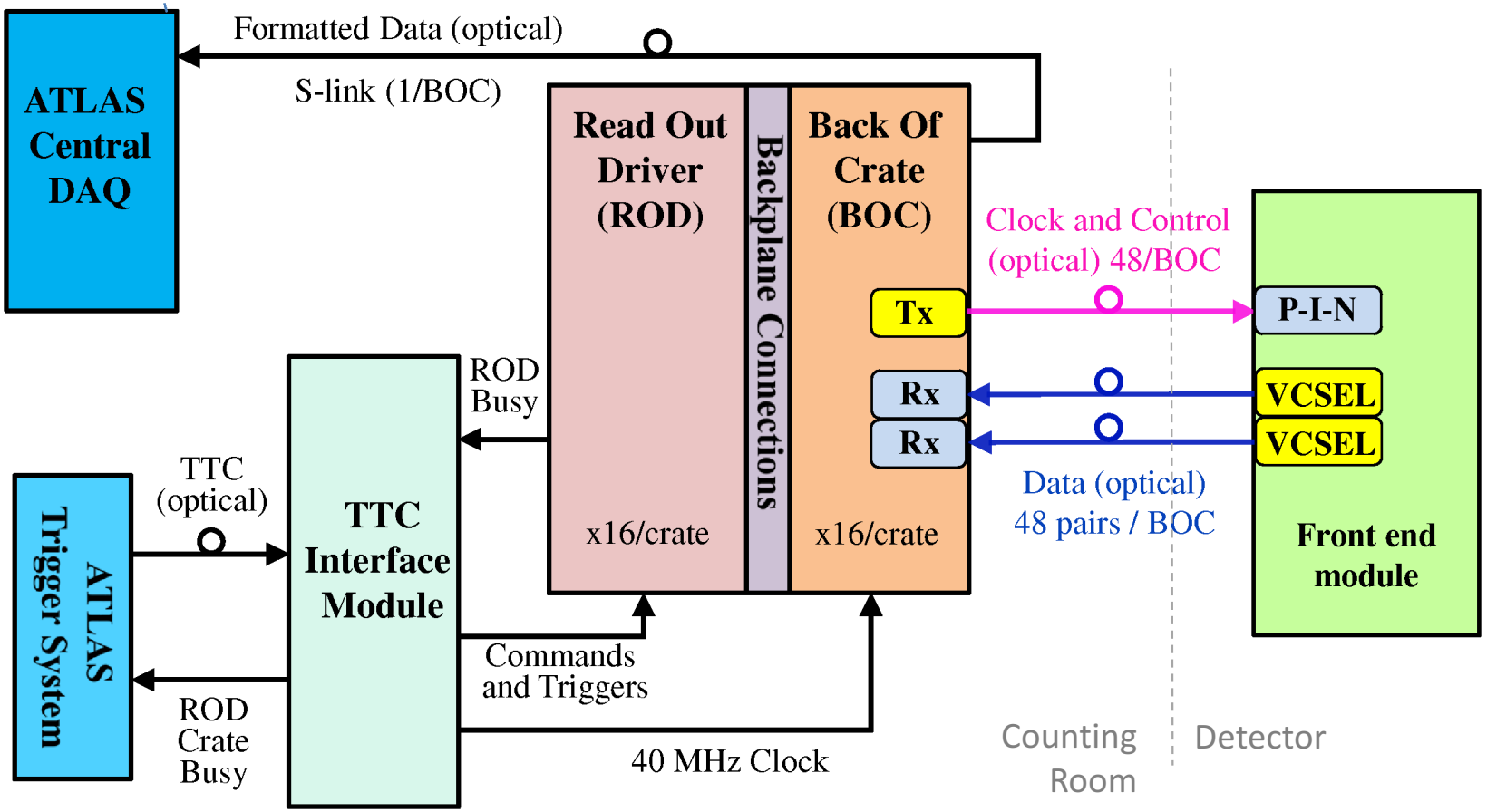


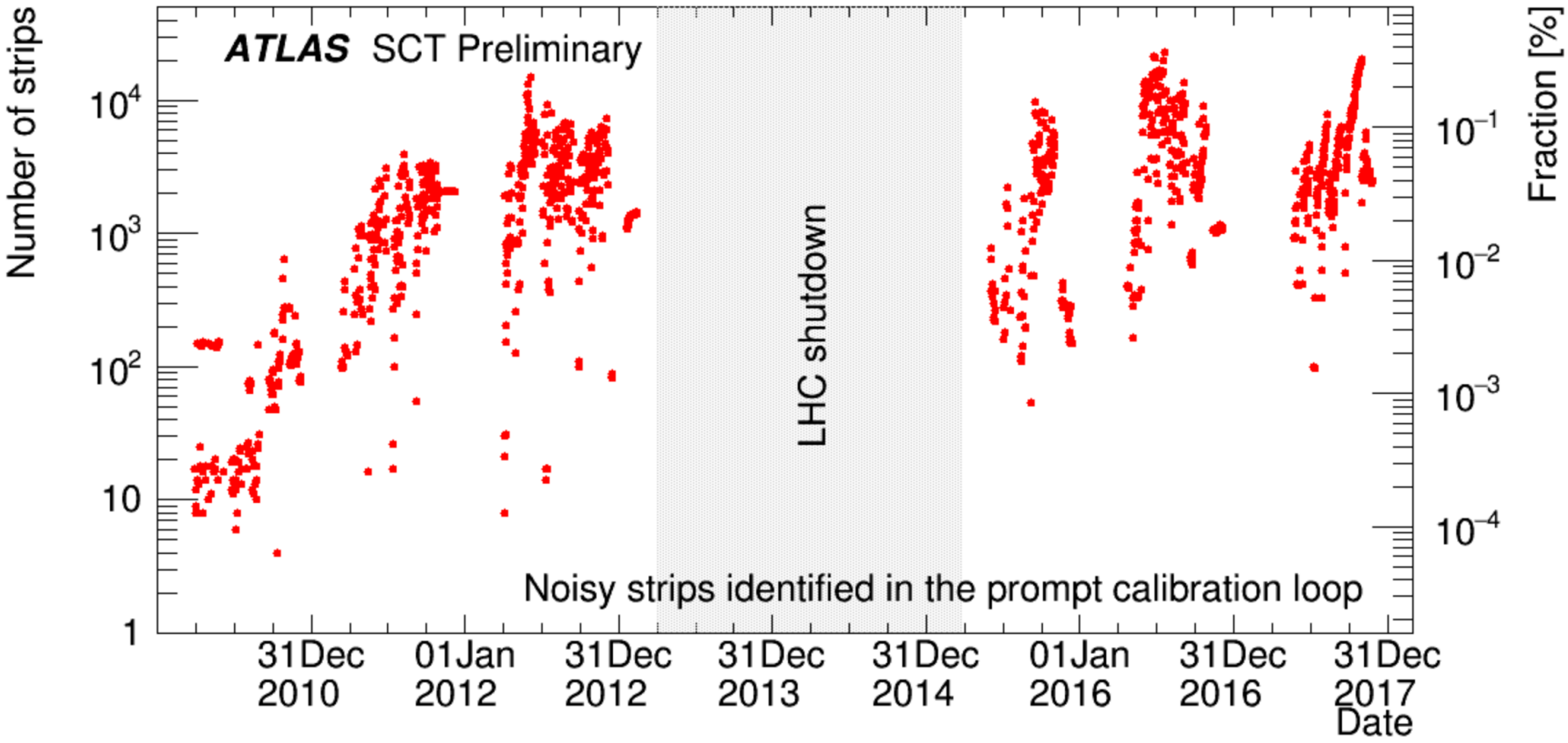
Summary

- The ATLAS SCT operates routinely at <μ>~60 with L1 rate 70-100kHz
  - Recall the design goals were originally <μ> up to ~23
- We observe clear evidence of SEU effects
- Measured rate of SEUs is comparable with predictions from early test-beam tests using pions and protons
- Very effective SEU suppression is in place, combining regular global reconfigurations with targeted module reconfigurations
- Impact of SEUs, and of the mechanisms in place to suppress them, have negligible impact on SCT data taking efficiency and on SCT data quality
  - Both >>99.9%

BACKUP

SCT DAQ and Optical Communication




ATLAS SCT Preliminary
Number of strips
Fraction [%]
LHC shutdown
Noisy strips identified in the prompt calibration loop
31Dec 2010
01Jan 2012
31Dec 2012
31Dec 2013
31Dec 2014
01Jan 2016
31Dec 2016
31Dec 2017
Date