SEU in CMS pixels

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for the CMS pixel group

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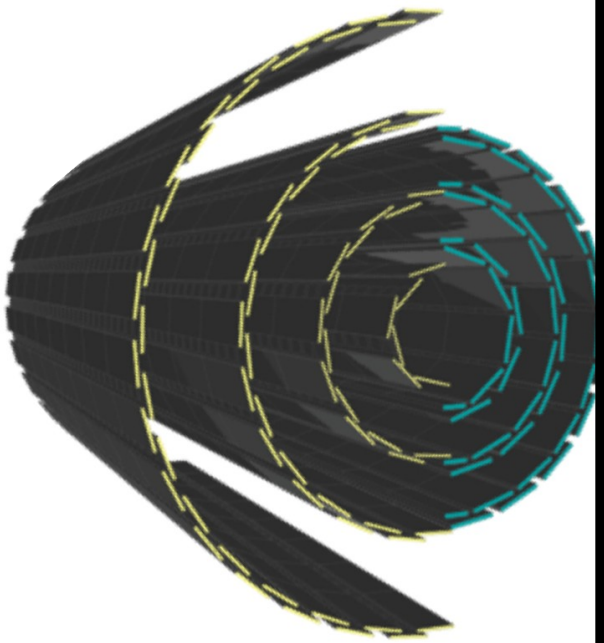
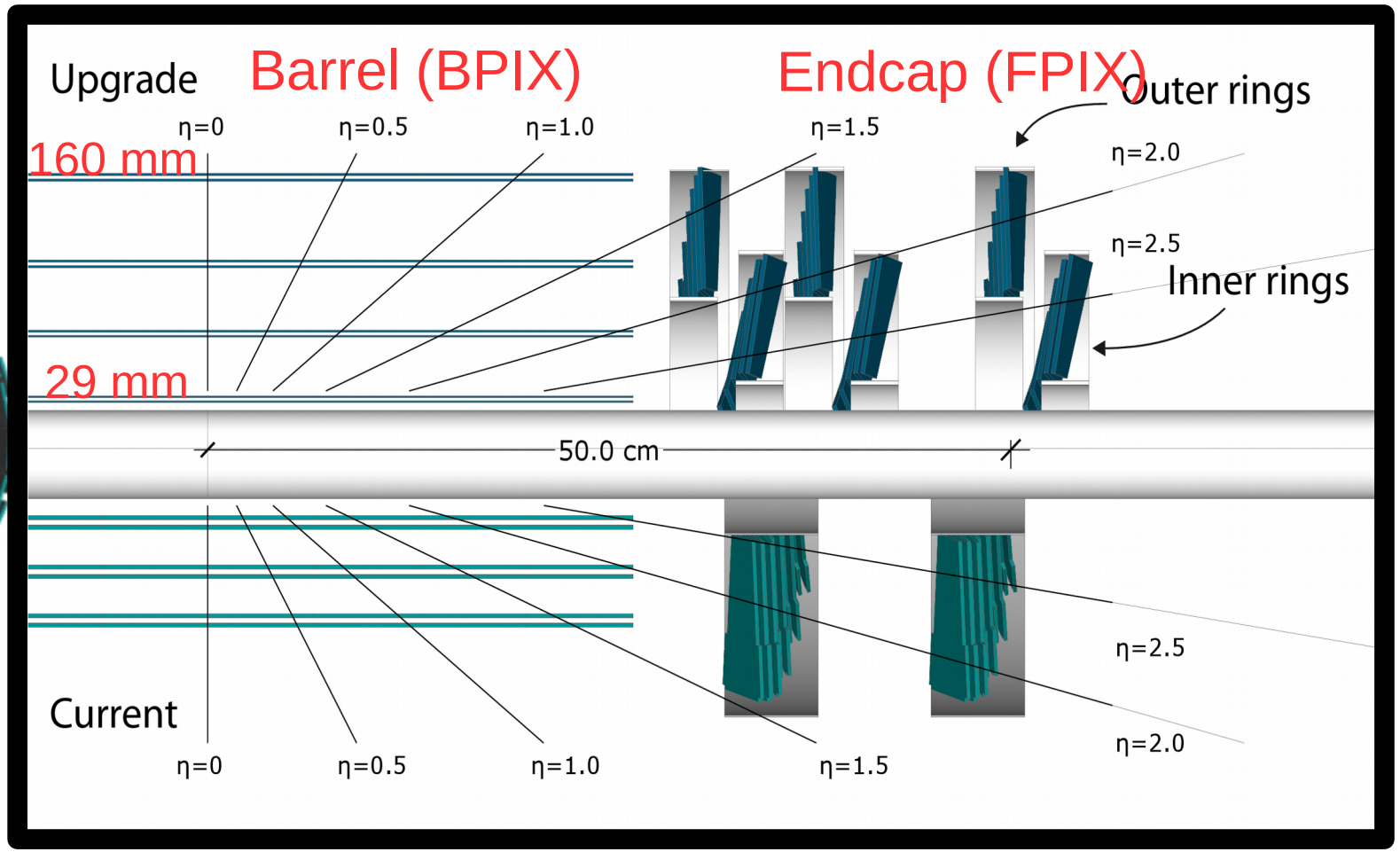
CMS pixel overview
SEU expectations and mitigation strategy
Operational experience

CMS Phase 1 pixel detector

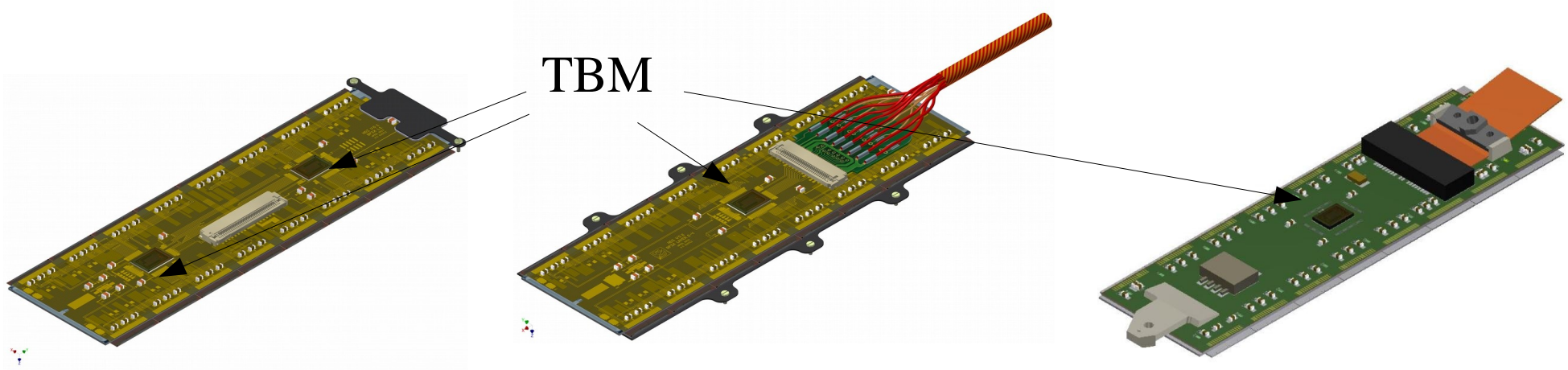




Similar design concept, with more layers/channels, higher rates

Improved front-end, same technology as “phase 0” (0.25 um CMOS)

CMS Phase 1 pixel modules (16 ROCs)



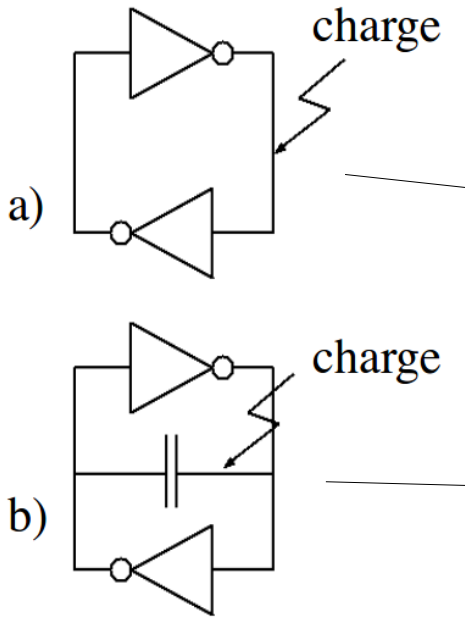
layer	Radius [cm]	modules		Particle rate [MHz/cm^2] @1e34	TBMs/ Cores
1	3.0	96		58	2 / 4
2	6.8	224		14	1 / 2
3	10.2	352		8.2	1 / 1
4	16.0	512		5.2	1 / 1
D1-3 inner	4.5-11.0	264		17	1 / 1
D1-3 outer	9.6-16.1	408		8.2	1 / 1

Possible SEU effects and mitigation

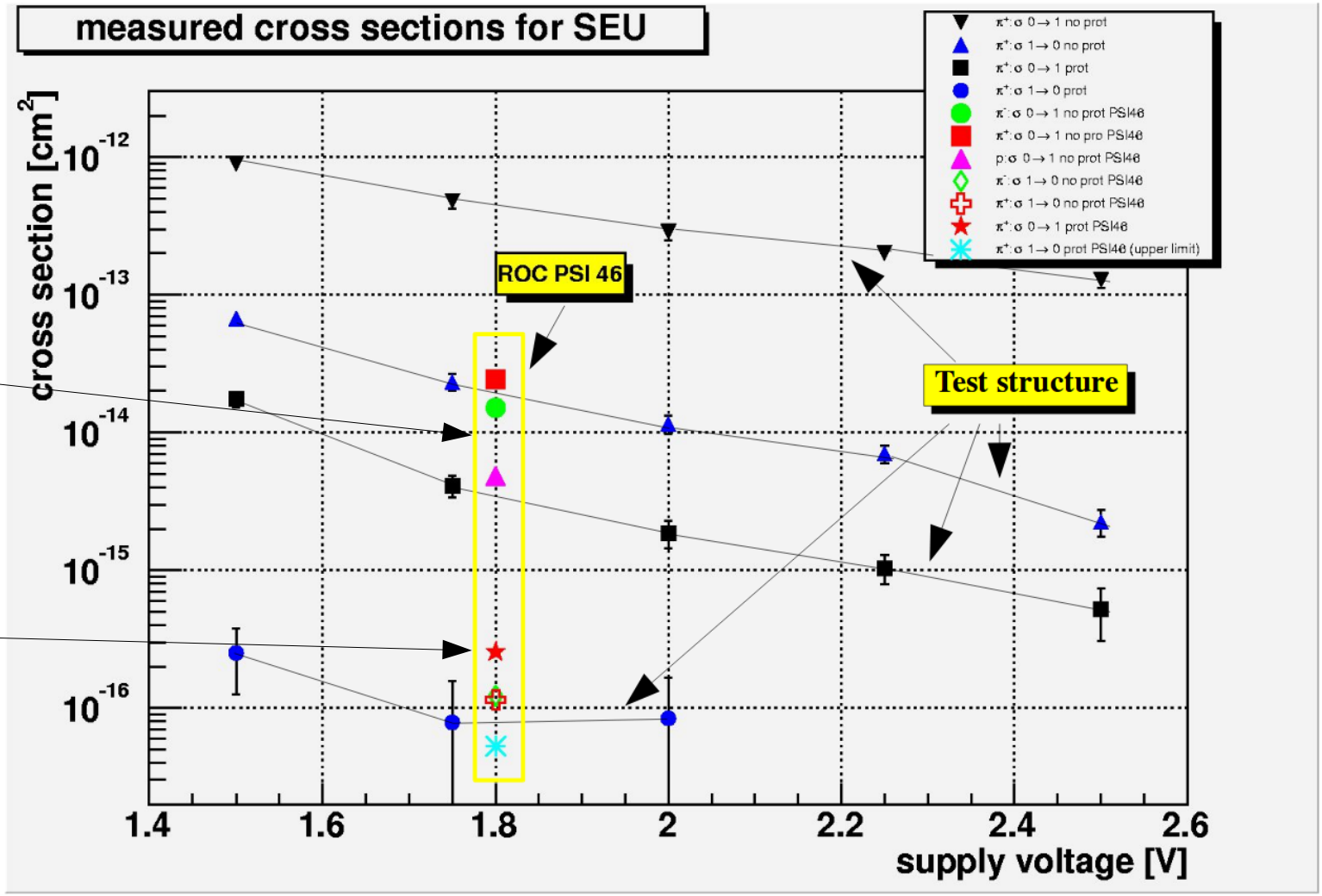
- Static (configuration registers)
  - Pixel
    - Trim / Mask : 5 bits / pixel — reprogram in between fills
  - ROC configuration registers
    - 19 / roc — reconfigure as needed (Soft Error Recovery, SER)
  - TBM configuration
    - 10 / 20 per module — reconfigure as needed (SER)
- Dynamic
  - Bit errors, loss of data / synchronization, frozen ROCs or columns, frozen TBM
    - frequent resets (O(100 Hz), not driven by SEU)
    - TBM get into a state only fixed by a power-on reset
  - Difficult to estimate or distinguish from other unknown effects

SEU Rate measurements (beam test)

Unit storage cell (a) without and (b) with SEU protection



PSI46V2.1 has all trim and mask bits protected

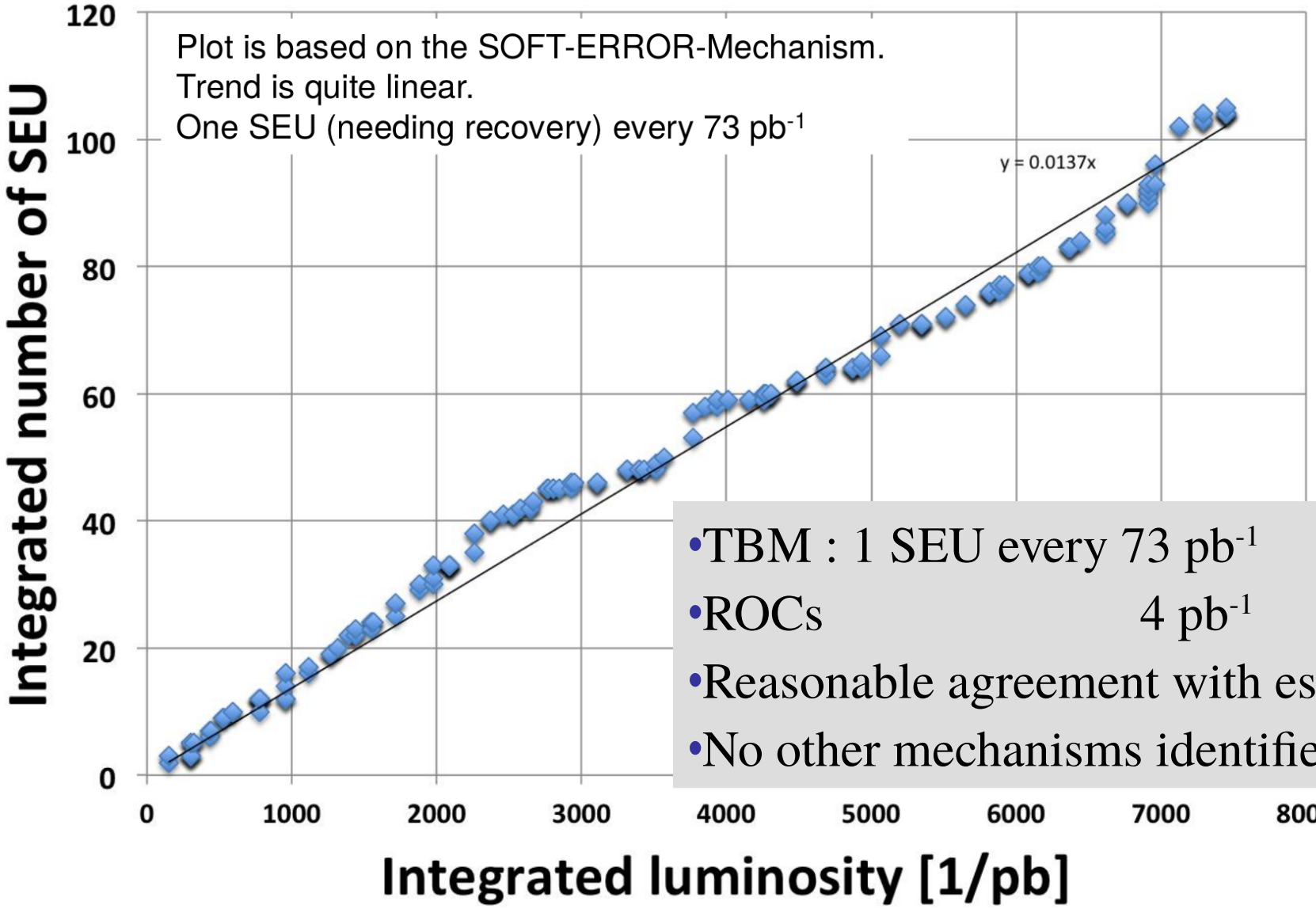


Wide range of values, depending on direction, layout, protection

BPIX L1 SEU rate expectations @ 1e34

- Projection of SEU test beam results for Phase 1,
- to be taken as pessimistic order of magnitude estimates
- Trim bits (4 bits/ pixel) → 0.5 px/ s ~ 0.04 % / h inefficiency buildup
  - single pixels may become inefficient or noisy → no mitigation needed during runs
- ROC DACs (19 DACs/ ROC) → 0.5 10^{-3} ROC/s ~ 0.1 % / h ~ 8 pb^{-1} / SEU
  - Single ROCs may become inefficient → reprogram (SER)
- TBM Ctrl (5 registers / TBM) → 2 10^{-5} TBM/s ~ 0.04 % / h ~ 330 pb^{-1} / SEU
  - Full / half module may become inefficient → reprogram (SER)
- SEU concept of the CMS pixel detector, unchanged for phase 1
  - Use simple capacitor protection only
  - Fast reconfiguration and frequent resets

Run 1 SEU



- TBM : 1 SEU every 73 pb^{-1}
- ROCs 4 pb^{-1}
- Reasonable agreement with estimates
- No other mechanisms identified

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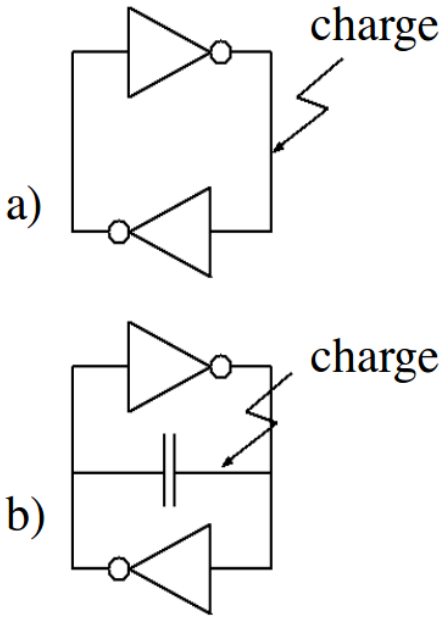
TBM SEU problem

- New error mode observed in Run2 (Phase 1) :
  - TBM cores (½ TBM) stop sending data, the other half continues without problems
  - Reset or reconfigure does not fix the problem
  - Only power cycling does
- Behaviour consistent with an SEU in one particular TBM FF (readout control)
  - Dynamic SEU, no connection with control registers, not cured by reconfiguration
  - Connected to power-on reset, but not soft-reset
    previous TBM versions had an additional “hard-reset” which was never used and therefore removed :(
  - Circuit modified with respect to the Run 1 / Phase 0 TBM
  - Not SEU protected (unlike DACs/Registers and many other flip-flops)

Compatible with SEU in unprotected FF

Unit storage cell (a) without and (b) with SEU protection



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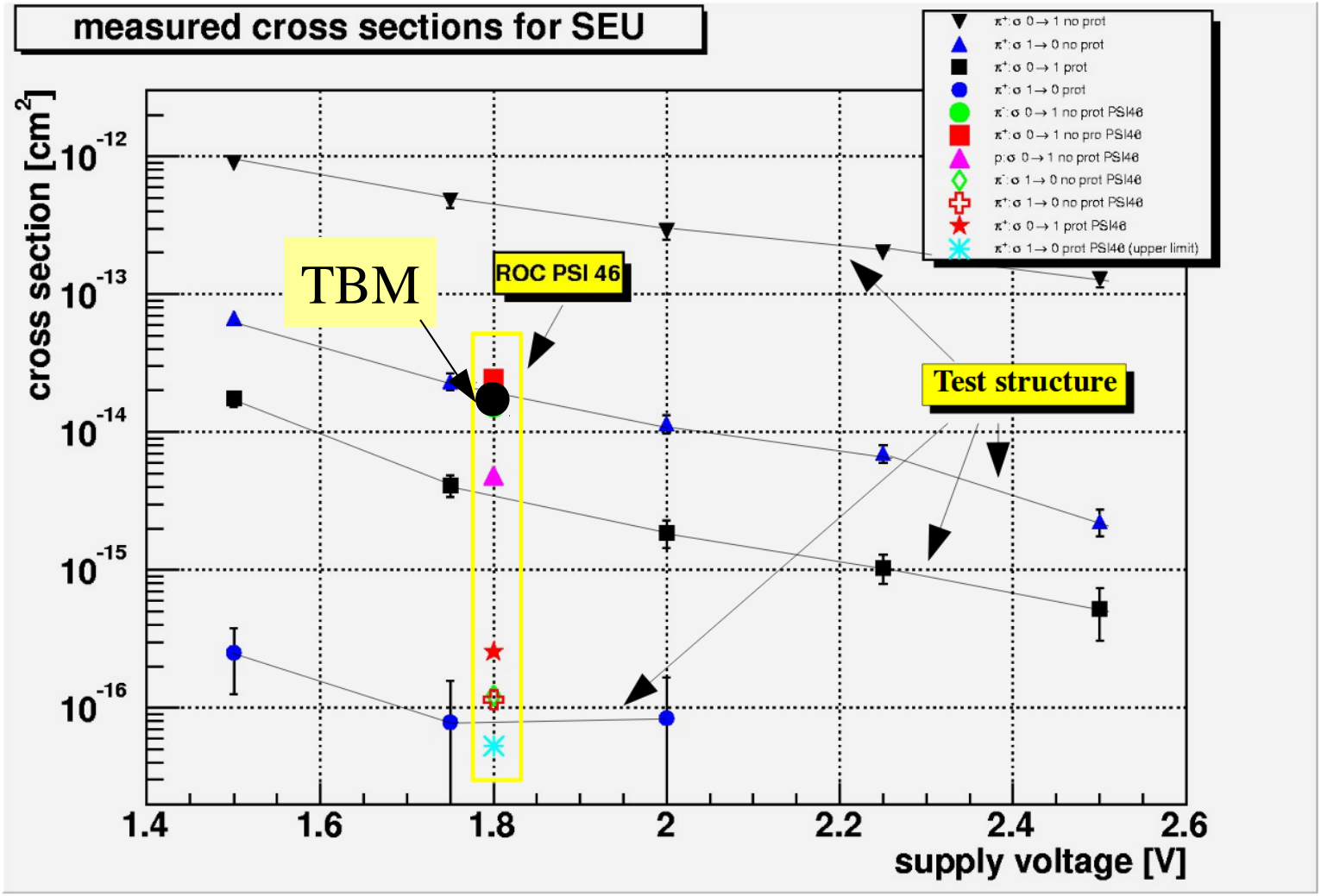
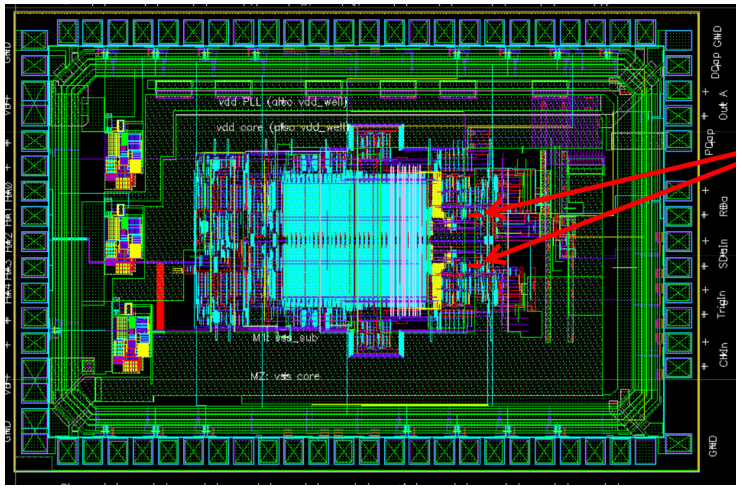


TBM SEU implications

- In 2017 modules were power cycled when the fraction of unresponsive module reached a threshold value (few %)
  - Time between power cycles at high luminosity : several hours
  - More frequent: Soft-error recovery (reconfigures ROCs/TBMs, does not fix TBM SEU)
- Contributed <1 % inefficiency,
  - not a show-stopper, but painful (in combination with other problems)
- During LS2 the first layer will be replaced, the TBM has been revised
  - Capacitor protection for the suspected FF
  - Connection to general soft reset
  - Additional reset signal (encoded on trigger line)
- Dedicated tests with micro beams are in preparation to confirm diagnosis and cure



Summary

- The CMS pixel has addressed SEU with a simple capacitor protection of (most) relevant cells
- The rate of soft errors is tolerable although slightly higher than expected from SEU
- A particularly nasty SEU effect stops the module controller chips until a power cycle
  - Will be cured in the inner layer TBMs after LS2
  - CMS will have to live with the problem in the outer layers / FPIX