



Silicon Sensor Simulation in the LHCb Monte Carlo Framework

Tomasz Szumlak on **behalf of the LHCb Collaboration Radiation effects at the LHC experiments and impact on operation and performance** 23 – 24 April 2018 CERN, Geneva

Outline

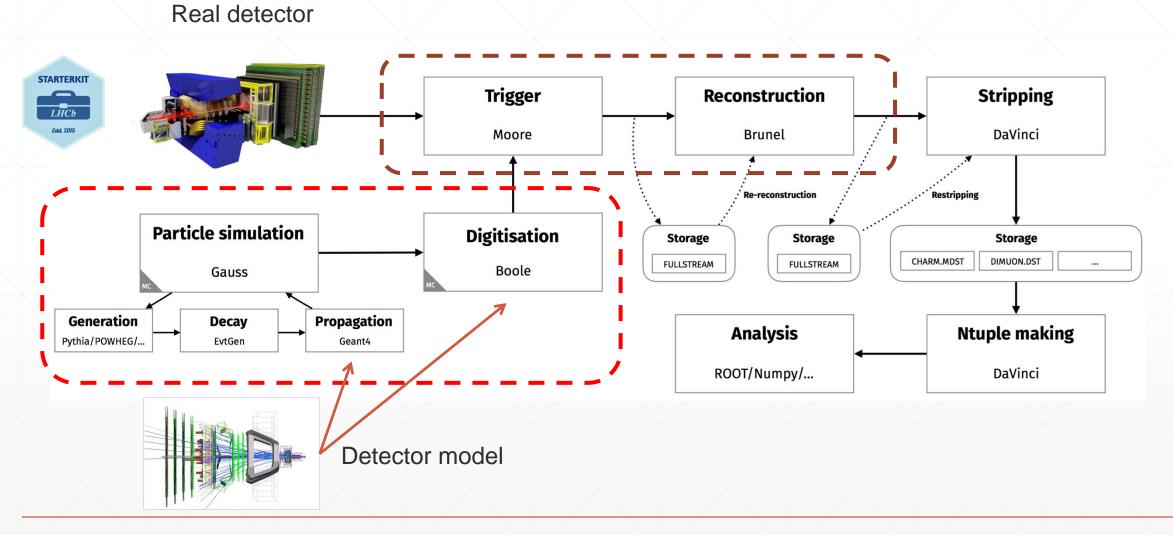
- Current silicon response simulation framework
- Tell1 (Trigger Electronics Level 1) electronics readout board emulation
- Silicon simulation for the upgraded detectors

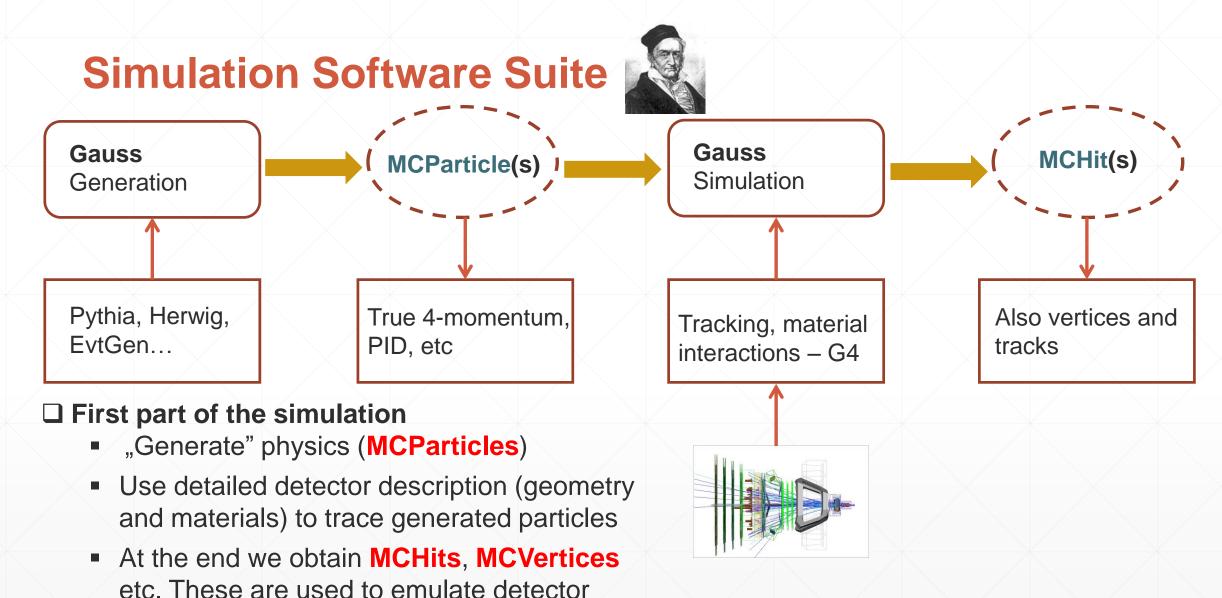
A general overview

Profiting from the fact that all of the tracking detectors are microstrip ones and readout by the same ASIC we provided a common framework for silicon simulation within LHCb

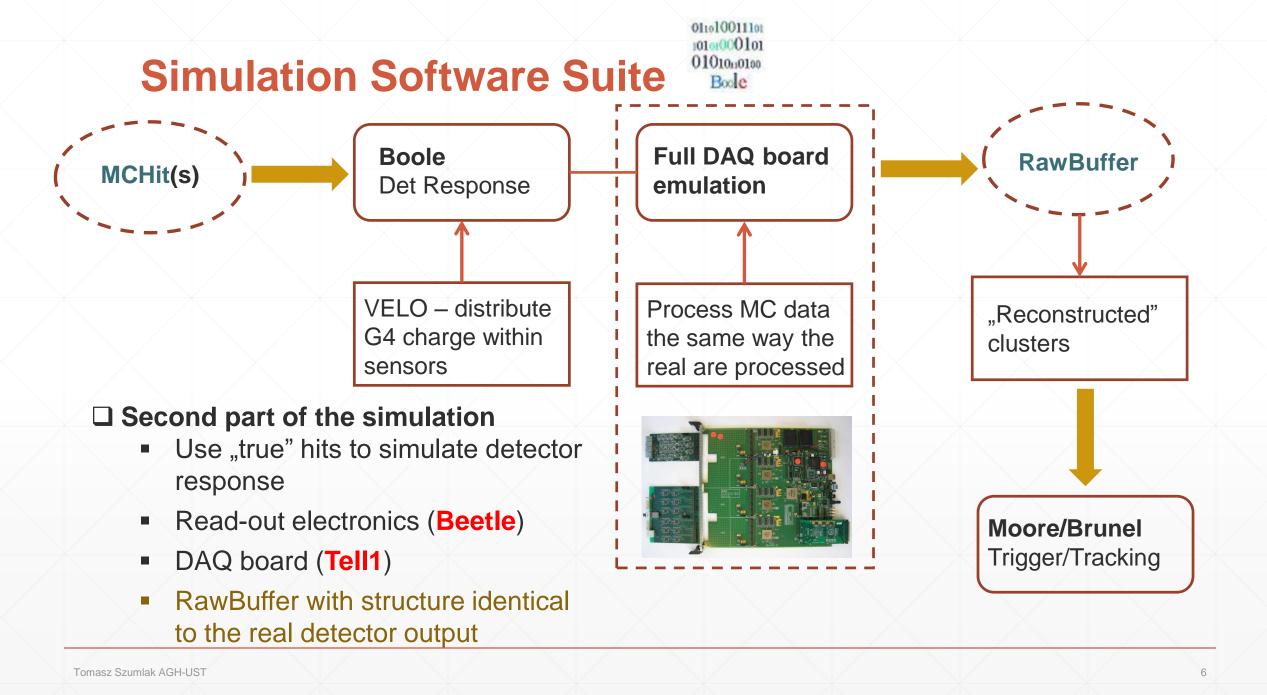
- □ The overall idea of the deposited charge (Geant4) distribution within the silicon bulk is the same
- Common code to model the Beetle readout chip response using dedicated configurations to evaluate detector specific front-end response pulse shapes
- □ Very similar digitisation code (analogue to digital)
- Due to different granularity and geometry the clusterisation is the most distinct part of the whole procedure
- □ Packing the clusters into RawBank follows again the same pattern

LHCb Software Suite

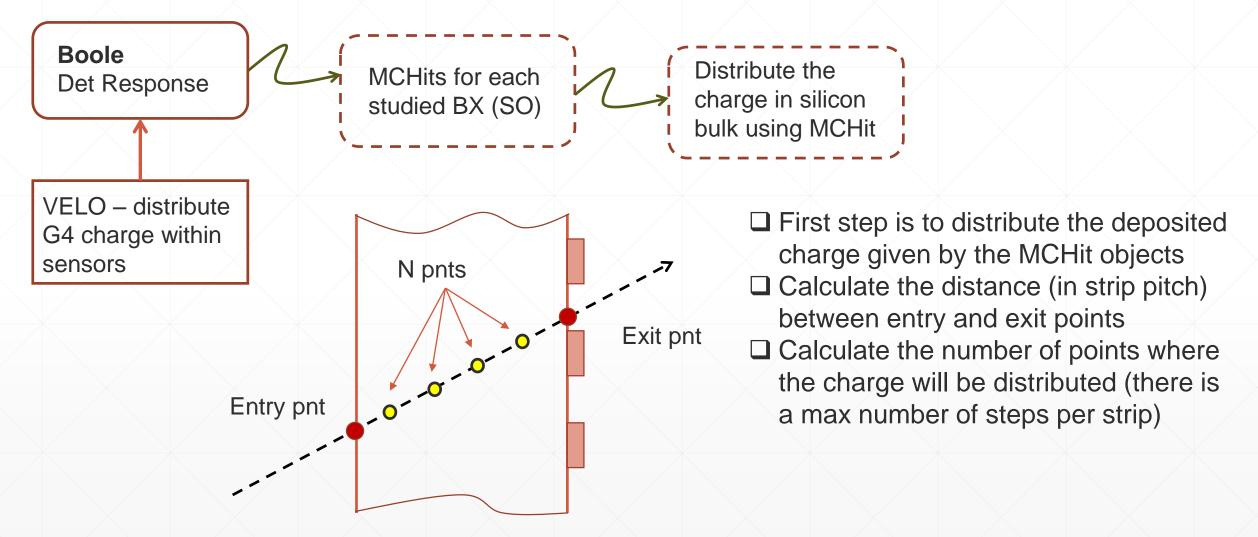




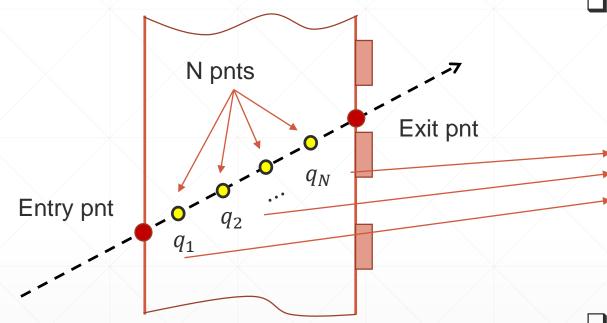
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Front end response (analogue signal)



Front end response (analogue signal)

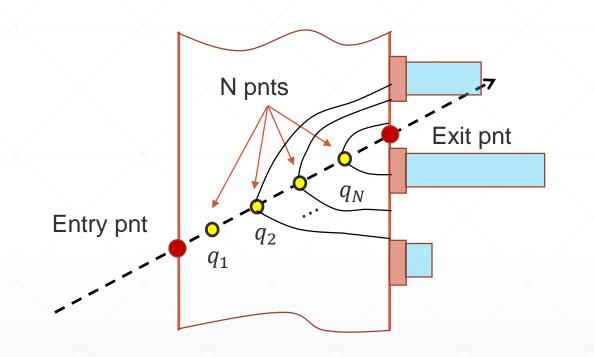


At this level, if requested we can use the radiation damage tool to simulate CCE loss and DML charge leakage

- Starting with generated total charge taken from G4 generated deposit, at each point we allocate partial charge that has three components:
 - Uniform component (the same value for each point)
 - Random component drawn from a normal distribution
 - \Box δ ray generation

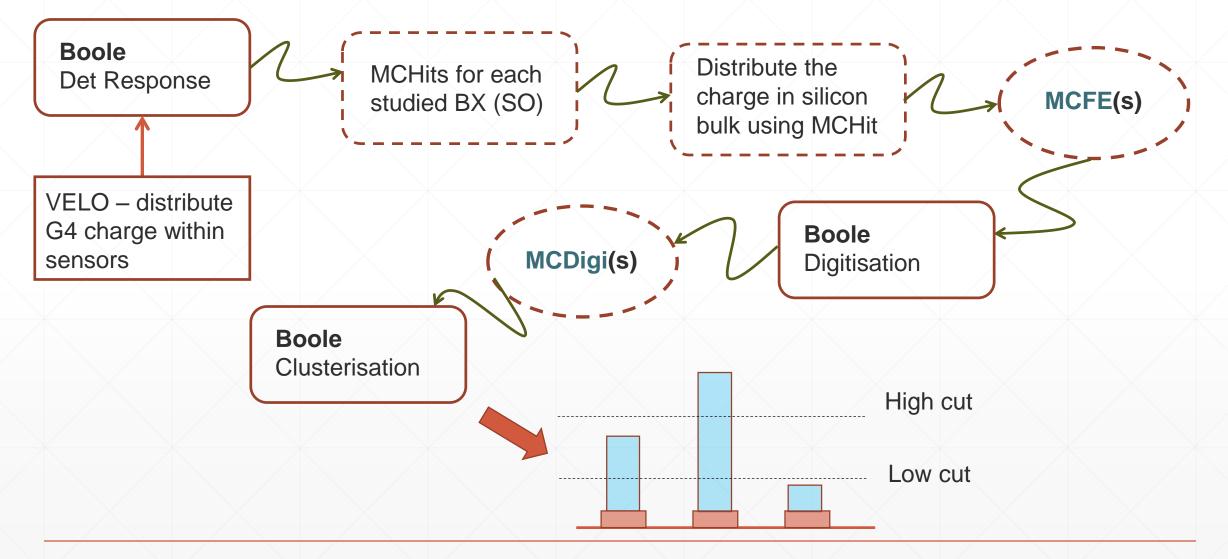
Generated charge normalisation to the total deposited energy at the end to avoid anomalus events

Front end response (analogue signal)



- Diffusion simulation
- Use gaussian smearing to calculate collected charge on strips
- If simulating radiation damage the "normal" diffusion can be scaled
- Introduce capacitive coupling (strip xtalk)
- Add **noise** taken from data
- □ If the **spill-over** is simulated repeat that whole procedure and use Beetle response tool to figure out the charge reminder
- Now we have front-end analogue signals (MCFE) that can be digitised

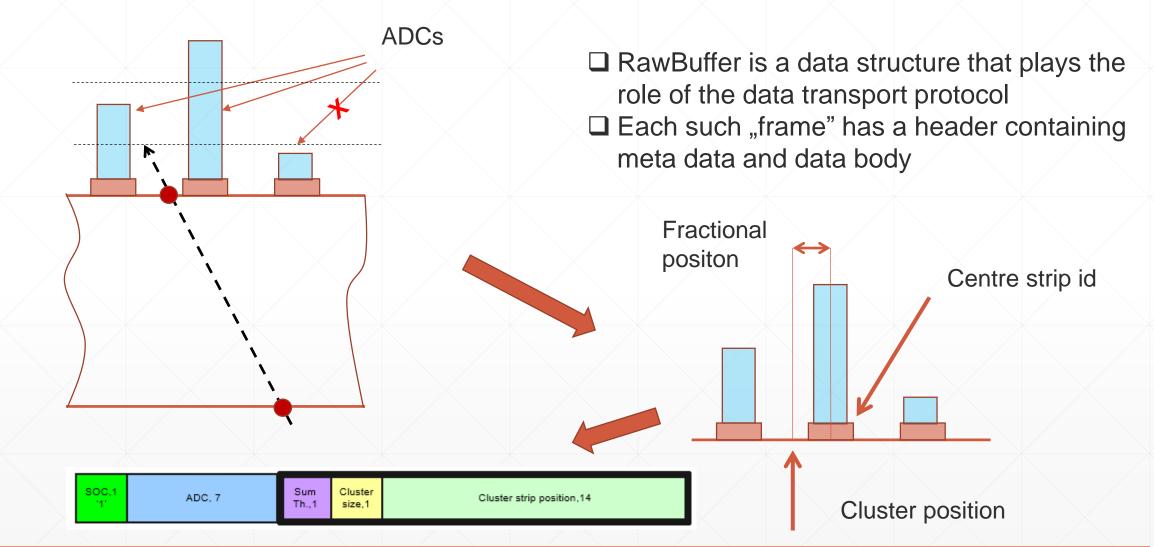
Detector Model



Clusterisation

- Complicated geometry and relatively high granularity make this process quite complicated for the Velo
- For these reasons the emulation code was partially ported to simulation s/w
- We use bit-perfect high level code that corresponds to the VDL machine code: reordering, zero-suppression and clusterisation
- Configuration is also taken from the calibration data stream: noise, threshold level, problematic channels

Raw buffer – beyond is only trigger...

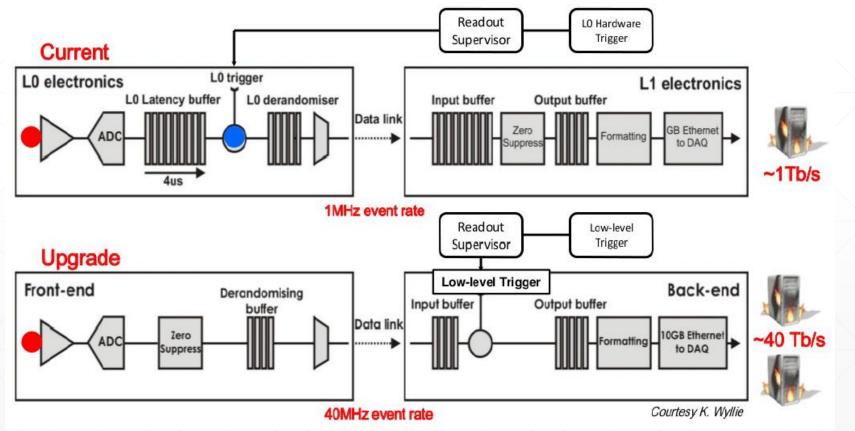


Upgrade

□Trigger-less

□ Sends out data with the machine frequency

□ On chip zero-suppression (SoC)



Silicon simulation and digitisation

- The overall idea very similar to the current s/w use MCHits to distribute charge, include noise, couplings, radiation damage
- Analogue to digital conversion using test beam results
- VELO pixel the output RawBuffer contains time ordered superpixels that are going to be further processed by HLT (High Level Trigge)
- Upstream Tracker the output RawBuffer contains zero-suppressed data that going to be spill-over corrected and clustered in HLT

Conclusions

- We use Pythia8/Geant4 to get hits and deposited energy (need also detector model)
- Simplified energy deposition in bulk and detailed information regarding total noise, readout electronics response, sensor x-talk, etc.
- Introduce radiation damage induced effects at this level (CCE, double metal layer, resolution)
- Similar approach for the upgrade (different detectors, different output format and further processing)

Current VELO

- Silicon (n⁺-on-n) micro-strip detectors
- 2x21 planes (R and ϕ)
- Floating pitch: ~40 –
 100 μm, thickness: 300 μm
- ~180 000 readout channels
- Total silicon area $\sim 0.32 m^2$
- Detectors operate at $-8^{\circ} C$

Current TT

- Silicon (p-on-n) micro-strip detectors
- Four planes $(0^{o}, +5^{o}, -5^{o}, 0^{o})$
- Pitch: 183 μm, thickness: 500 μm
- Long readout strips (up to 37 cm)
- ~143 000 readout channels
- Total silicon area $\sim 8 m^2$
- Detectors operate at 5^o C

Current IT

- Silicon (p-on-n) micro-strip detectors
- Four boxes and four planes $(0^o, +5^o, -5^o, 0^o)$
- Pitch: 198 μm, thickness:
 320 μm and 410 μm
- ~130 000 readout channels
- Total silicon area $\sim 4.2 m^2$
- Detectors operate at 5° C

