Summary of the Electronics/optoelectronic session, draft version 2.0, 4.05.2018

Monday 23 April 2018, 14:00-18:00, CERN

https://indico.cern.ch/event/695271/

1) Introduction, Alexandre Rozanov (CPPM-IN2P3-CNRS-Univ.Aix-Marseille)
2) TID effects at 130nm pixel electronics at low dose in ATLAS, Malte Backhaus (ETH, Zurich).
    - Observation of the strong increase of low voltage current from 1.7 A to 2.7A in FE-I4-B chips at IBL after low dose (0.2-1.5 MRad) in 2015.
    - Strong increase of the current during LHC fills (0.1-0.2 MRad).
    - Explanation by accumulation of oxide charges and detailed study of the effect in the X-ray irradiation facility.
    - Understanding of the temperature and irradiation rate dependence of the effect.
    - Mitigation of the effect in 2016 by increasing the cooling temperature from -10° C to +15° C and decreasing digital voltage from 1.2V to 1.0V.
    - Decrease to normal currents after TID of ~10 MRad and gradual return to default digital voltage and cooling temperature.

3) SEU in ATLAS FE-I4 electronics, Pierrefrancesco Butti (CERN).
    - ATLAS pixel FE-I4-B chips in IBL exposed up to the record peak luminosity of 2.1 10^{34} cm^{-2} s^{-1} at the small radius of 3.3 cm.
    - Design of the special SEU hard DICE latches for local pixel and global configuration memory.
    - Observation of the SEU 1->0 of the “enable” pixel latch, creating “quite” pixels.
    - Observation of SEU 0->1 of the MSB of TDAC lathes, creating “noisy” pixels due to sudden decrease of the threshold.
    - Observation of the dead chips and change in the current consumptions due to the SEU in the global configuration memory. Mitigated in 2017 by refreshing global memory during ECR every 5 seconds.
    - Studies of SEU by observation of the flip of “enable” bits and read-back procedures.
    - Development of software for gradual refreshing of the local pixel memories during ECRs in 2018.

4) In-Situ Radiation Damage Studies for SCT Optical Links, Tony Weidberg (Univ. of Oxford).
    - Observation of the decrease of the optical power of the VCSELs slightly larger than expected from test beam extrapolation.
    - Observation of the decrease of responsivity of p-i-n diodes smaller than expected from the test beam results. The difference is probably due to the

rate or annealing effects. Exact mechanism of the damage not yet understood.
- No effect on the depletion voltage of p-i-n diodes, as expected.
- Observed decrease of the VCSELs optical power and p-i-n diodes responsivity can be accommodated in the existing power budget until the end of run 3 in 2023.

5) SEU mitigation in the ATLAS SCT, Dave Robinson (Univ. of Cambridge).
   - Observed module synchronization error rate proportional to particle flux.
   - Expected bit flip in configuration memory and lost trigger in p-i-n diode.
   - Measured SEU rates for p-i-n diodes compatible with pion and proton test beam results. Measured SEU rates for ABCD registers factor of 3 higher than predictions from test beams.
   - Mitigation by reconfiguration of the modules with errors, typically 50/60 per hour.
   - Global reconfiguration of the modules after 90 luminosity blocks (~1.5 hour) with dead time of 1.4 seconds in combination of error module reconfiguration allows to achieve greater than 99.9% data taking efficiency.

6) Irradiation aging of the ATLAS Transition Radiation Tracker (TRT), Bijan Haney (Univ. of Pennsylvania).
   - Due to the irradiation of TRT preamplifiers a small decrease of Z->ee efficiency was observed at the end of Run 1.
   - Similar change of the effective thresholds was observed after irradiation of the electronics with Co^{60} source. Threshold shifts are saturated after the dose of 30 kRad and is stable up to 500 kRad
   - The drift of the gain was understood both on transistor level as well as at the higher threshold level.
   - After the irradiation effects were saturated, the thresholds were corrected.
7) CMS Tracker Optical Links Radiation Effects. Measurement and Prediction, Jan Troska (CERN).
   - Radiation testing of CMS laser diodes define qualification level at 500 fb^{-1}
   - Measured data and annealing used to predict laser threshold increase inside CMS for given luminosity.
   - Opto scan procedure periodically correct operating point for analog links, determine laser threshold and efficiency.
   - Model describe very well average observations.
   - Safety factors are used for future upgrades.
8) CMS pixel overview. SEU expectations and mitigation strategy. Operational experience, Wolfram Erdmann (Paul Scherrer Institut).
   - Observed during Run1 in TBM chip one SEU per 73 pb^{-1}, and in ROC chip one SEU per 4 pb^{-1}. This is in the reasonable agreement with test beam estimations.
   - New Run2 chips used the same SEU hard concept.

- In Run 2 observe new error mode consistent with SEU in one TBM FF, which was not SEU protected. TBM cores stop sending data, reset or reconfig does not help, need power cycle to restart. Unused "hard reset" was removed in new chip version.
- SEU cross-section of unprotected FF is 2 10^{-14} cm^2
- In 2017 modules were power cycled every few hours and more frequently soft error recovered. This procedure contributed to < 1% dead time. Not a show-stopper, but painful in operation.
- TBM chip was revised and first layer will be replaced in LS2.
- CMS has to live with this problem in outer pixel layers.

9) Radiation Hardness of Monolithic Sensors and readout Electronics for the ALICE Inner Tracker System Upgrade, Hartmut Hillemanns (CERN).
   - ALICE CMOS TJ 180nm pixel TID hardness is tested up to 2 MRad
   - Thresholds, currents, DAC settings affected by TID and dose rate. Current and DAC settings anneals after few days. Thresholds annealing slow, but readjusted with DAC settings.
   - Detector performance not affected up to 350 kRad
   - Typical SEU cross-section in region memory 7 10^{-14} cm^2
   - Single Event Latchup cross-section is less than 10^{-8} cm^2 for max. LET< 15 MeV cm^2/mg expected for LHC hadrons.

10) Discussion

- Need one more workshop at beginning 2019.
- No new thematic for 2019 workshop proposed yet.
- No explicit requests for the session on the irradiation of commercial electronics yet.
- Interest for the yellow book as the result of the workshop.

Lessons learned and messages to LHC upgrade community

1) Need to check for increase of the low voltage currents at low dose and design the system for maximum possible currents (multiple pads and wire bonds on low voltage supplies, choice of the cooling temperatures).
2) Need to use SEU hard designs for pixel configuration memories. Importance to develop from the beginning the software and hardware mechanisms for dead time free refreshing of the pixel configurations.
3) Importance to plan sufficient power budget in VCSELs and responsivity budget p-i-n diodes to accommodate for irradiation degradation effects.
4) Periodic reconfiguration of the modules (~1.5 hour) and reconfiguration of the modules with errors allows high data taking efficiency in ATLAS Si strips.
5) Importance to test SEU in the beam even with minor modification of the good working pixel chip.
6) Very interesting ongoing future developments of TJ 180 nm pixel CMOS for applications with radiation hardness