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Module Design and Development for LHCb VELO Upgrade Project

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TLHCb experiment is about to implement a major upgrade, scheduled to start data taking in LHC Run III. The Vertex Locator (VELO) is the silicon detector surrounding the interaction region. It will be completely replaced with a new light weight pixel detector capable of 40 MHz readout.

The upgraded VELO modules will each host 4 silicon hybrid pixel tiles, each read out by 3 VeloPix ASICs. The silicon sensors must withstand an integrated fluence of up to $8\times10^{15}1MeVn_eq/cm^2$, a roughly equivalent dose of 400 MRad. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, with a total rate of 1.6 Tbit/s anticipated for the whole detector. The detectors are located in vacuum, separated from the beam vacuum by a thin custom made foil. The foil will be manufactured through a novel milling process and possibly thinned further by chemical etching.

The VELO upgrade modules are composed of the detector assemblies and electronics hybrid circuits mounted onto a cooling substrate, which is composed of thin silicon plates with embedded micro-channels that allow the circulation of bi-phase CO_2. The front-end hybrid hosts the VeloPix ASICs and a GBTx ASIC for control and communication. The hybrid is linked to the opto-and-power board (OPB) by 60 cm electrical data tapes running at 5 Gb/s. The tapes must be vacuum compatible and radiation hard and are required to have enough flexibility to allow the VELO to retract during LHC beam injection.
The entire assembly must respect
strict deformation and bending constraints, have a high radiation tolerance and very low outgassing levels. The module design will be described

Presenter: DE AGUIAR FRANCISCO, Oscar Augusto (CERN)