Analytic thermoelectric modeling of silicon detectors – ATLAS ITk strips

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Particles, Strings,
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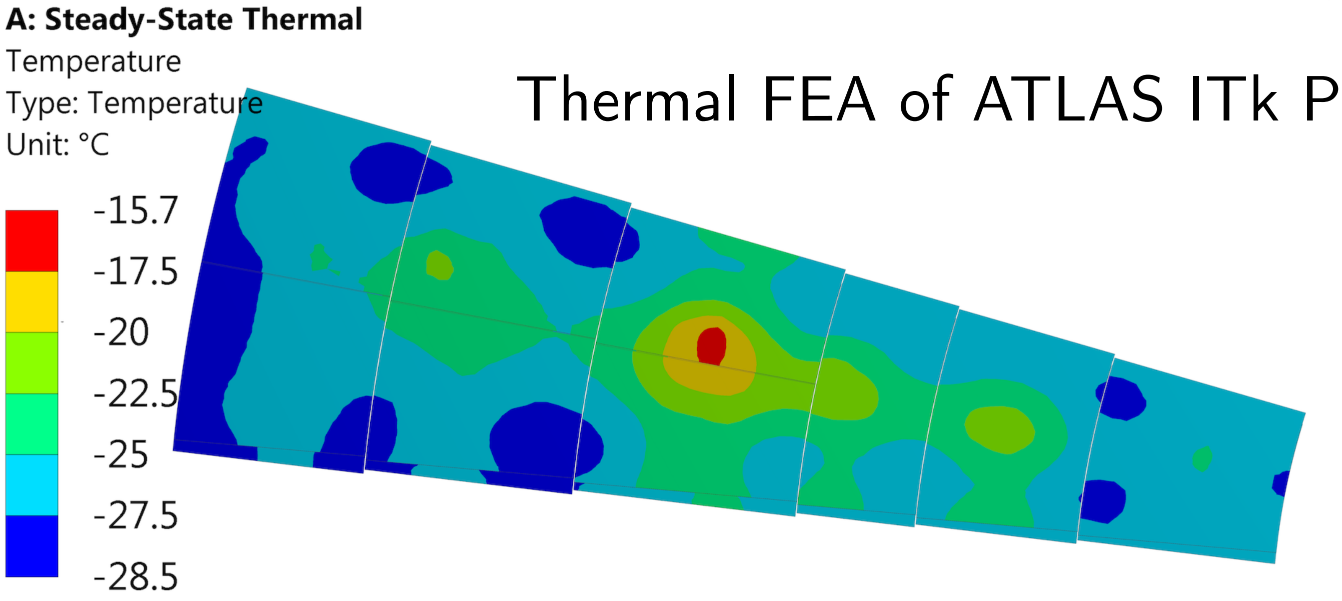
Collaborative Research Center SFB 676

Motivating an Analytic Model for Silicon detector



Thermal FEA of ATLAS ITk Petal

- Goal: model thermal and electric properties of silicon modules
- Thermal FEA results offer a snapshot of the thermal performance
  - Fixed power inputs
  - Fixed coolant temperature
- An analytic model of the thermal and electrical properties would:
  - Allow us to extrapolate to arbitrary inputs
  - Enable modeling of the entire lifetime of the detector (and predict thermal runaway)
  - Provide qualitative understanding of module behavior
  - ... and obtain results much faster compared to re-running FEA
- The model discussed here is detailed in a [paper in Nucl. Instrum. Methods]

Ingredients for the Thermoelectric Model

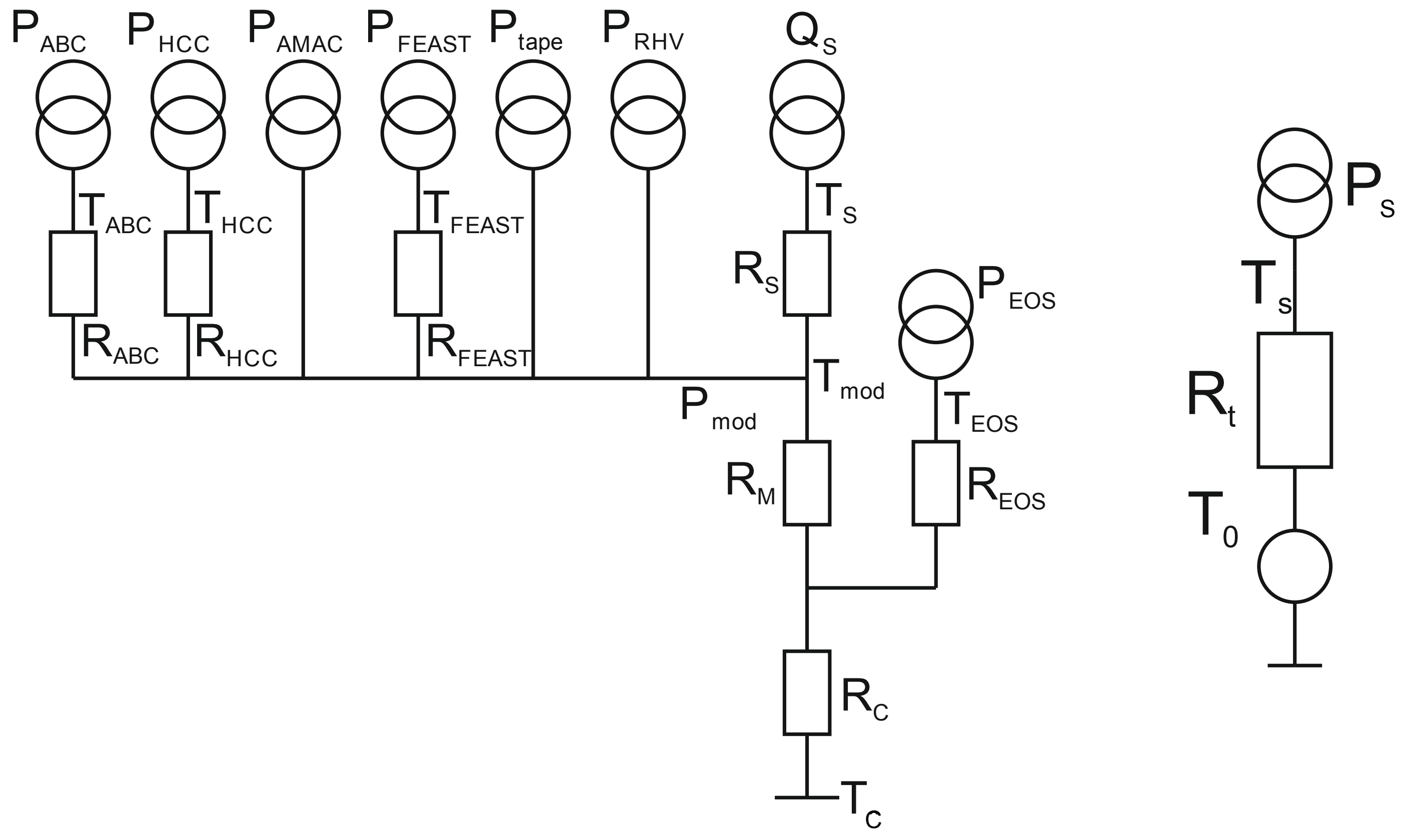
Five main components:

1. **Electrical:** Model of the module's electrical components
    - Including power estimates for each component, and interdependencies
2. **Thermal:** Linear model; estimate thermal impedances from FEA simulation
3. **Silicon:** Model of leakage current due to radiation damage
4. **Radiation levels** (particle fluence and total ionizing dose)
5. Encode any dependencies on temperature, radiation damage, etc. into the model

- In the following, we use the ATLAS ITk Strip detectors (barrel + endcap) to illustrate the construction of the model

The Thermal Model Component

Thermal schematic of the ATLAS ITk Strip module:



- Model the thermal pathways in 1 dimension, by analogy with the electrical model:

Electrical	**Thermal**
Electrical resistance	Thermal resistance (R)
Current source	Power
Voltage	Temperature
$\Delta V = I \times R$	$\Delta T = P \times R$

- Thermal impedances (resistance) must be determined using FEA (example later)

Calculating Sensor Leakage current

- "I_{ref}" current taken at a reference temperature (T_{ref}) –15° C
- Relationship between I_{ref} and Fluence is linear (see plot)
- We can calculate the sensor leakage power at a given time using:
  - I_{ref} vs fluence (Right)
  - Current-power relationship:

$$Q_{ref} = V_{\mathrm{bias}} I_{ref} A_{\mathrm{sensor}}$$

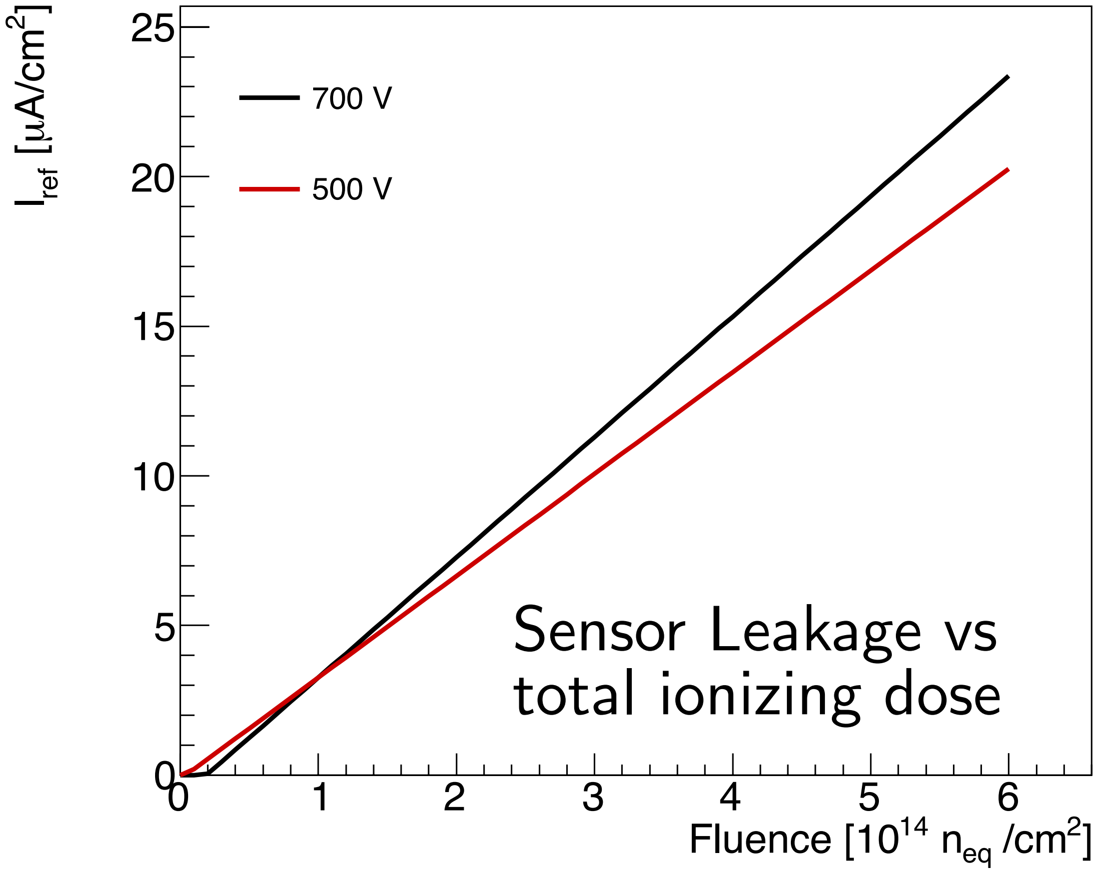
  - Relationship between leakage current & sensor T:

$$Q \sim T_S^2 \, e^{-T_A/T_S}$$

  - Thermal balance equation:

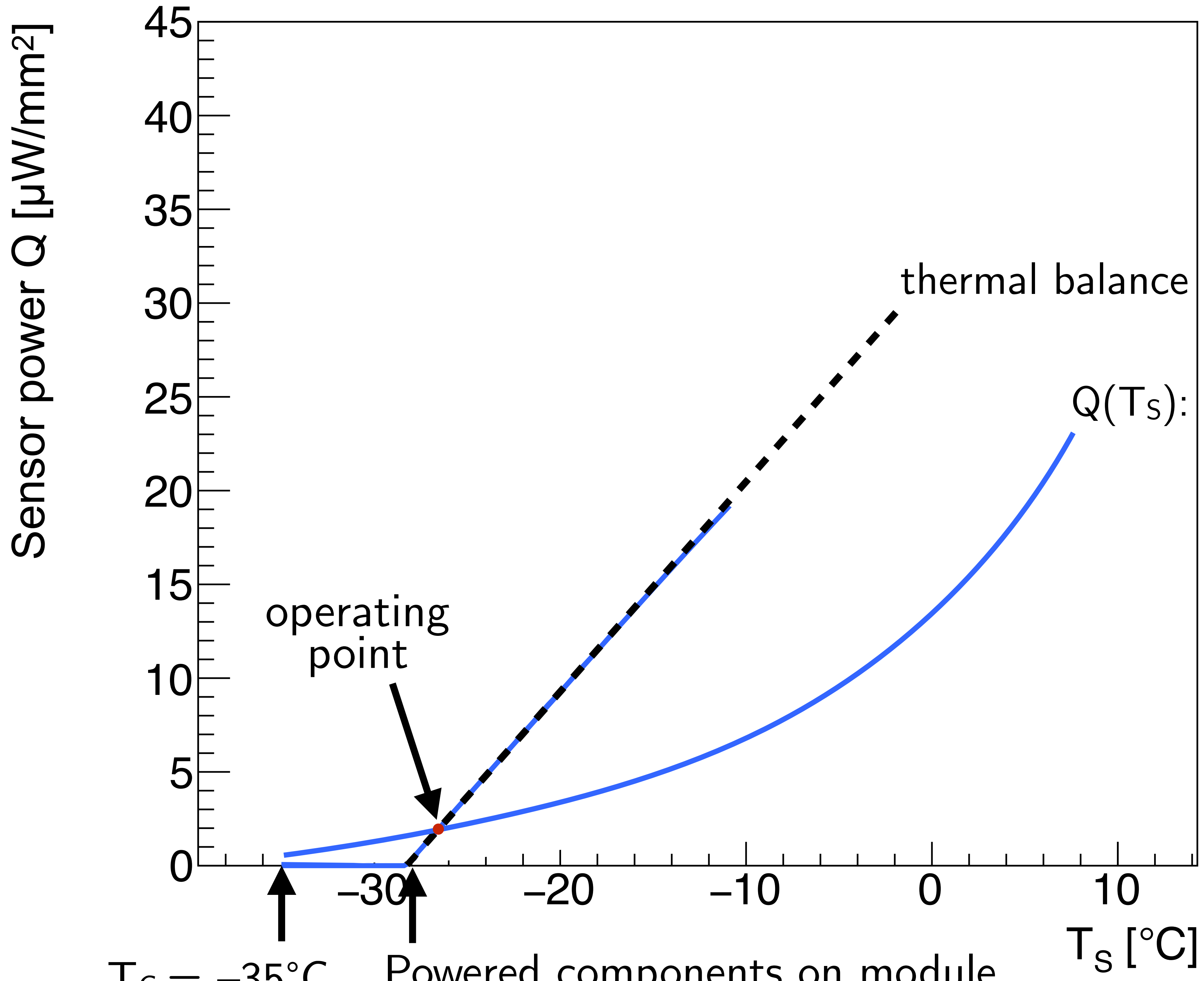
$$Q(T_S) = \frac{T_S - T_0}{R_t}$$

  - Solve (numerically) for T_S, $Q(T_S)$ by setting last two equations equal



Sensor Leakage vs total ionizing dose

Solving for Sensor T_S, $Q(T_S)$



thermal balance equation: $Q(T_S) = \frac{T_S - T_0}{R_t}$.

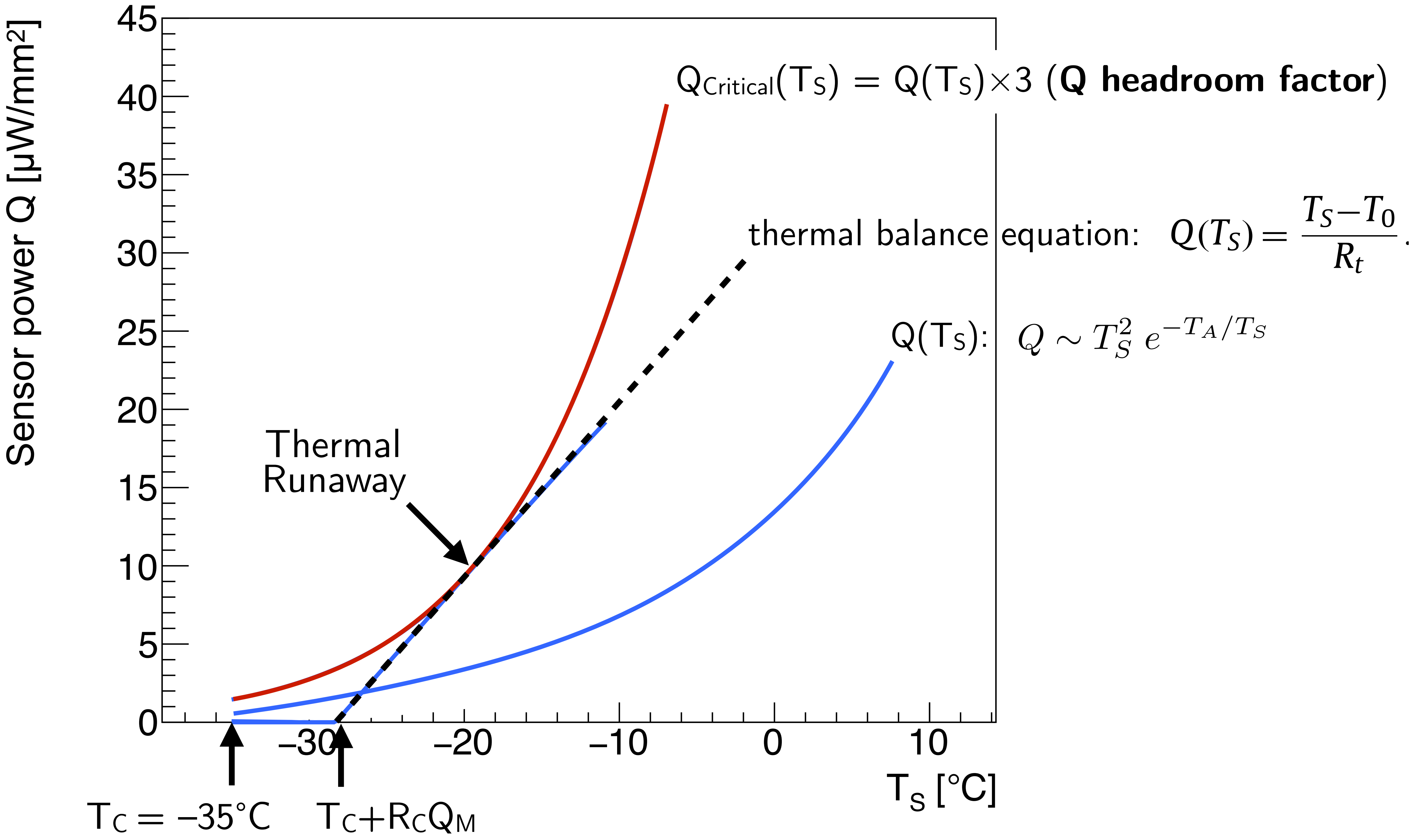
$Q(T_S)$: $Q \sim T_S^2\, e^{-T_A/T_S}$

operating point

$T_C = -35$°C

Powered components on module raise sensor T ($T_C + R_C Q_M$)

Sensor Q Headroom

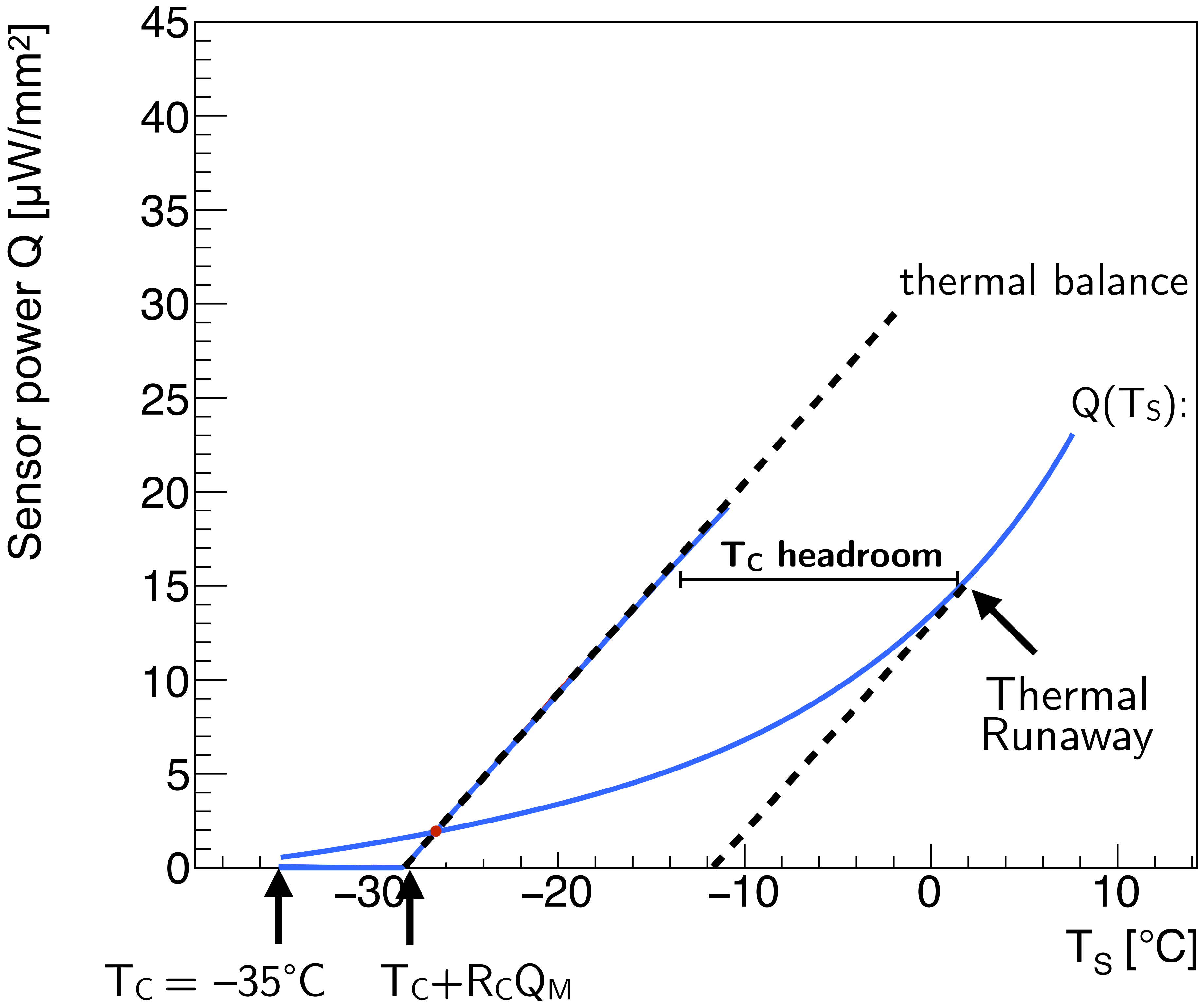


$Q_{Critical}(T_S) = Q(T_S) \times 3$ (**Q headroom factor**)

thermal balance equation: $Q(T_S) = \dfrac{T_S - T_0}{R_t}$.

$Q(T_S)$: $Q \sim T_S^2\, e^{-T_A/T_S}$

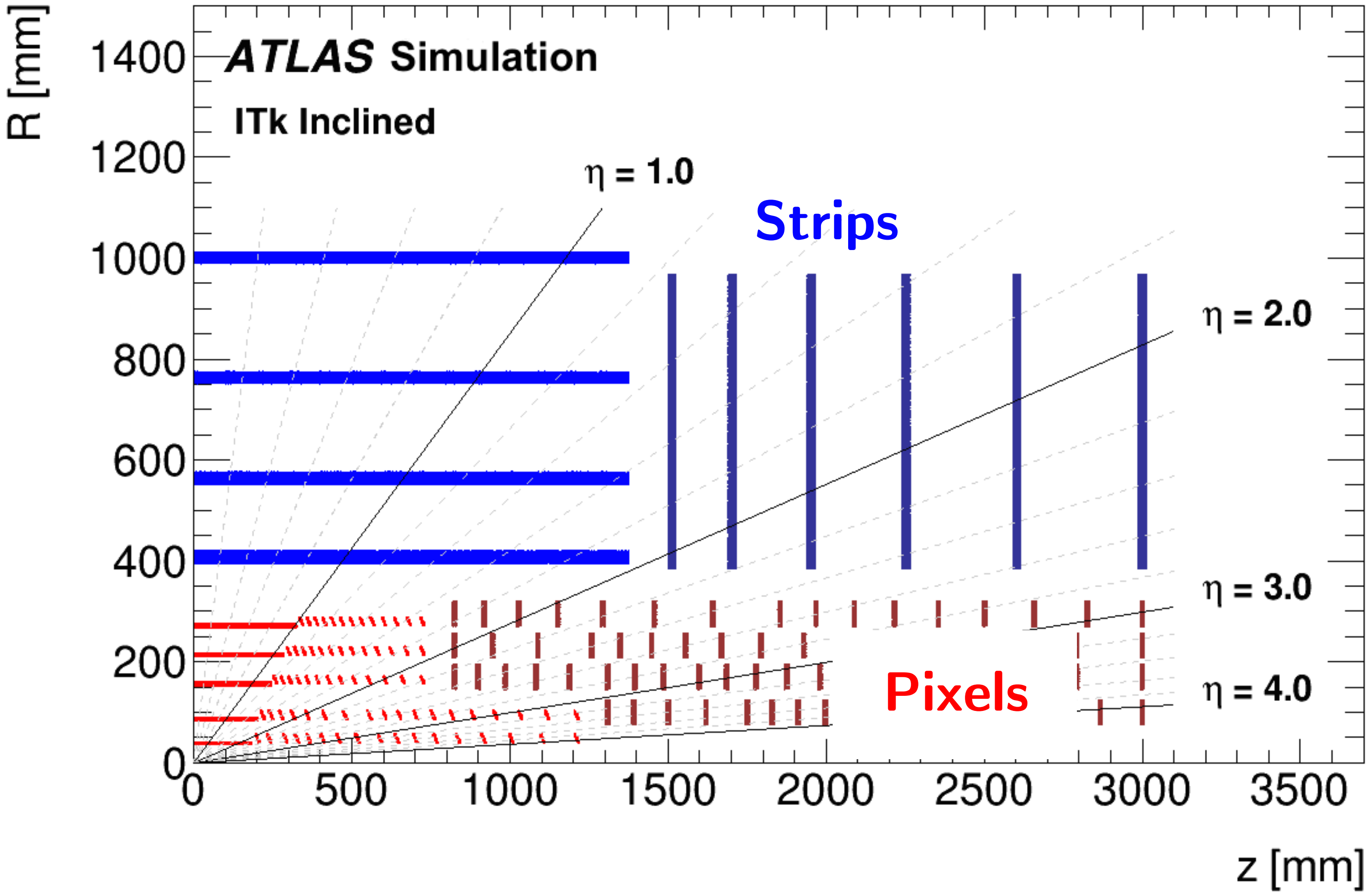
Coolant Temperature Headroom



thermal balance equation: $Q(T_S) = \frac{T_S - T_0}{R_t}$.

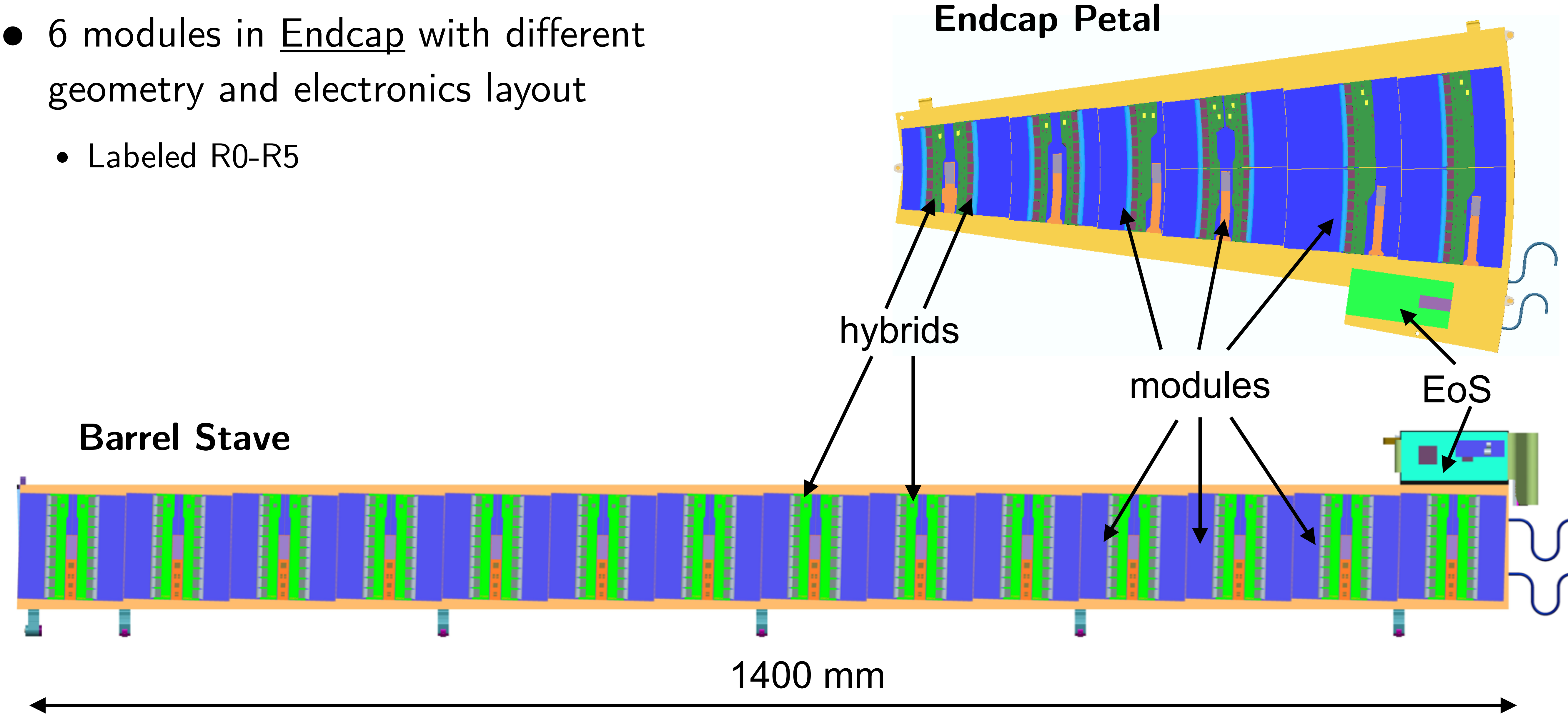
$Q(T_S)$: $Q \sim T_S^2 \, e^{-T_A/T_S}$

Case Study: ATLAS ITk Strip Detector (Barrel and Endcap)



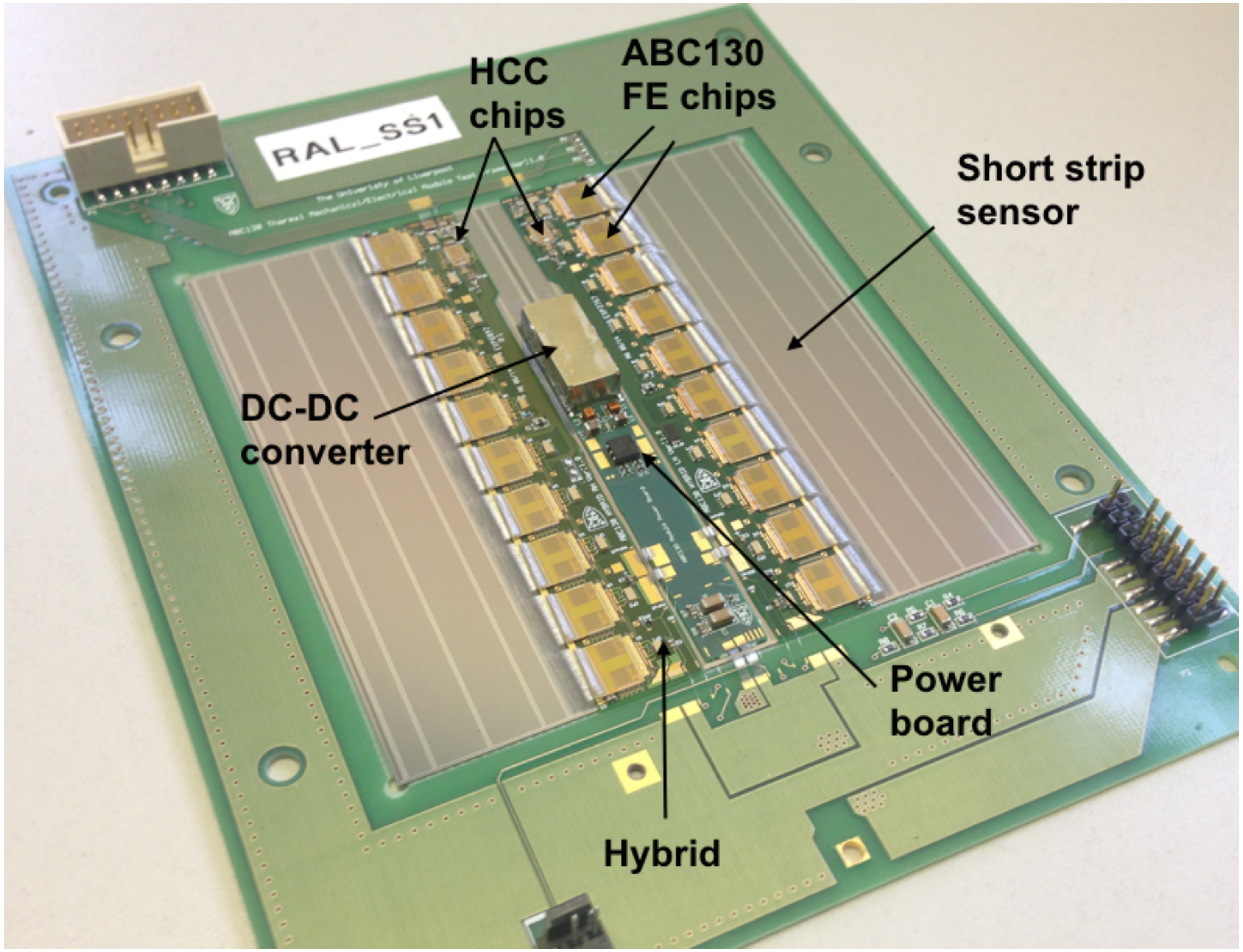
Basics of ATLAS ITk Strip System

- 13 modules in Strip Barrel with ~same geometry
  - Short strip (inner) and Long Strip (outer) layers
- 6 modules in Endcap with different geometry and electronics layout
  - Labeled R0-R5



Anatomy of an ITk Strip Module

- Silicon sensor
- Power Board:
  - DCDC converter “FEAST”
- Hybrid board:
  - ABC: Front-End chip
  - HCC: Control / readout chip
- Bus Tape
  - LV and HV distribution
- End-of-substructure (EOS) card
  - One per stave or petal side, additional powered readout components



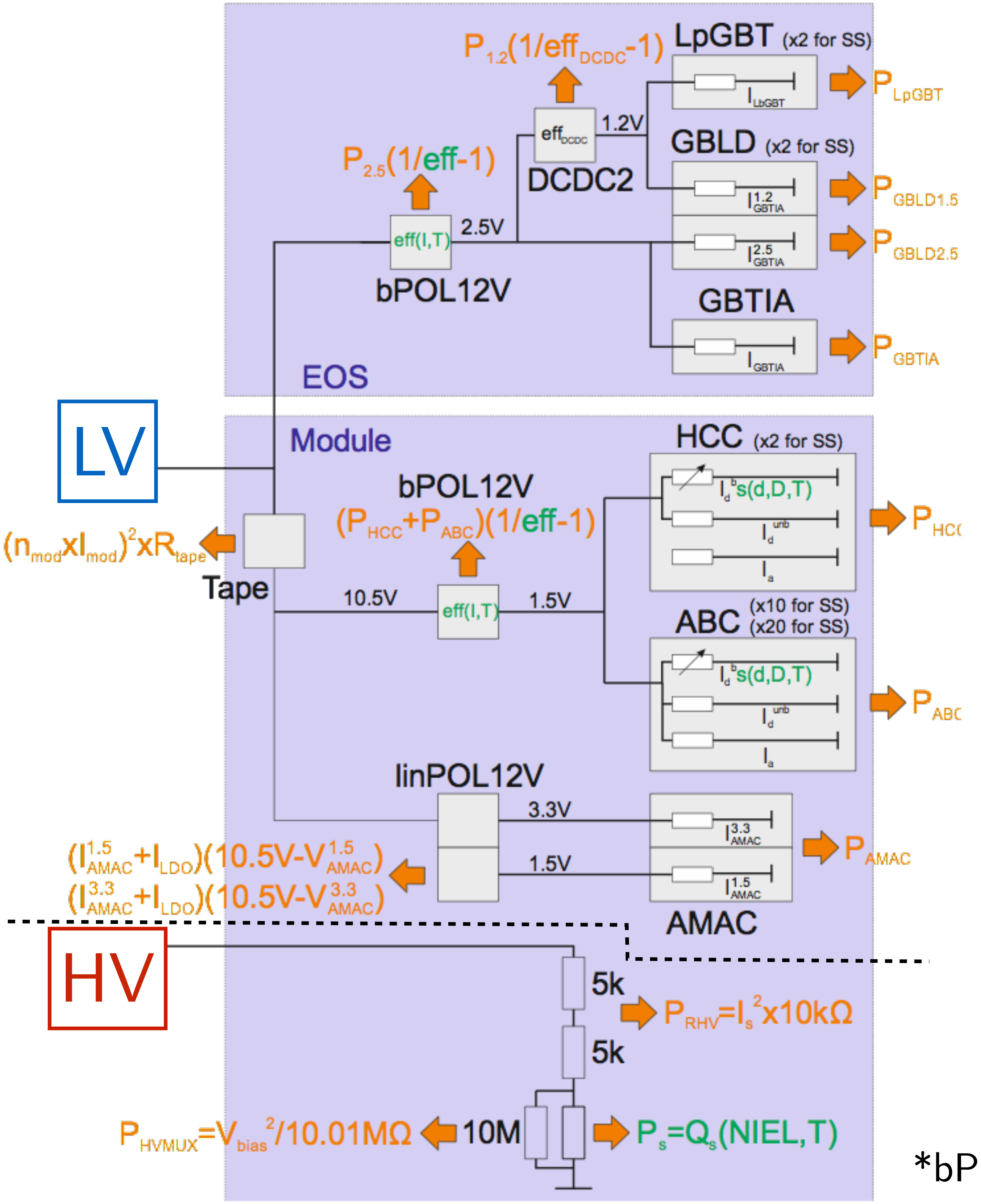
CO_2 Cooling with a nominal operating temperature of –35°C

Basic Inputs to the Model

Basic Inputs to the Model

- Electrical Model
- Thermal model (and deriving thermal impedances using FEA)
- Others

Basic Electrical Model of the Module



- LV and HV electrical models
- **Orange** arrows are sources of power (heat)
- **Green** parameters depend on component temperature

- In general, these are linear networks, with a few important exceptions
  - All non-linear components must be adequately described (shown later)

*bPOL12V = DCDC converter

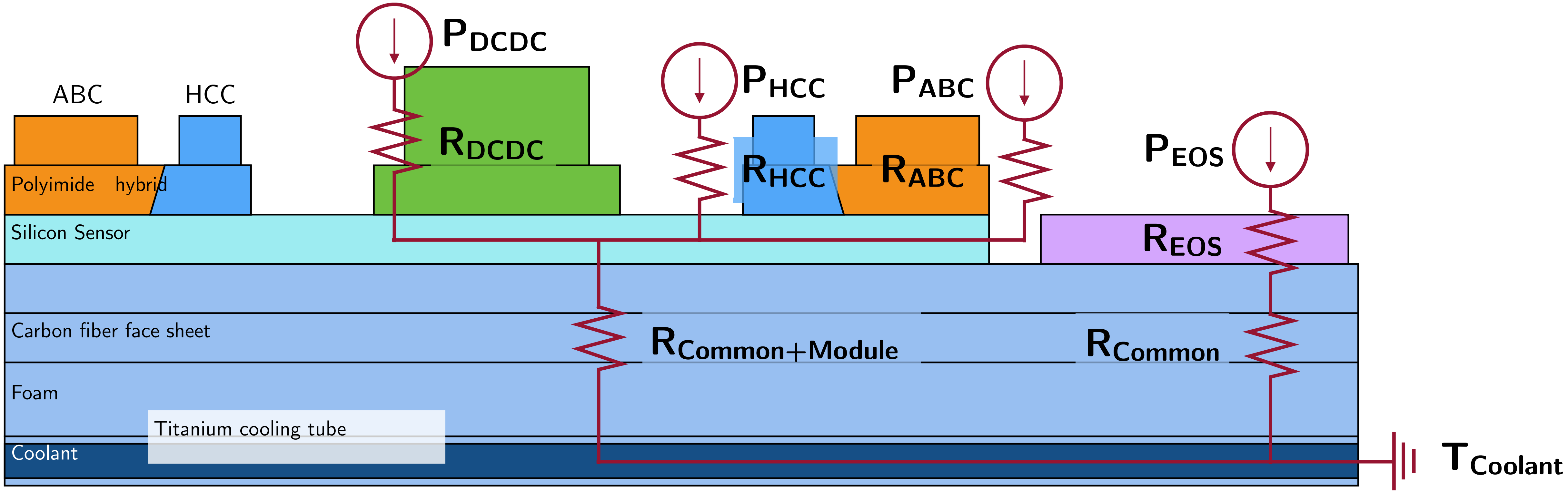
Electrical Component specifications

Description	input voltage [V]	Specifications for 1 component			n components per module (1 side)	Total power (1 side) [W]
		current [A]	power [W]	eff		
AMAC 1.5V	1.5	0.045	0.0675		–	
AMAC 3.0V	3.0	0.002	0.006		–	
Total AMAC	–	–	0.0735		1	0.0735
ABC (digital)	1.5	0.035	0.0525		–	
ABC (analog)	1.5	0.066	0.099		–	
Total ABC	–	0.101	0.1515		21*	3.1815$^{*\text{TID}}$
HCC (digital)	1.5	0.125	0.1875		–	
HCC (analog)	1.5	0.075	0.1125		–	
Total HCC	–	0.200	0.3		2*	0.6$^{*\text{TID}}$
FEAST (ABC,HCC)	–		$\frac{(1-\varepsilon)}{\varepsilon}(P_{\text{ABC}}+P_{\text{HCC}})$	$f(T,i)$	–	1.2605$^{*\text{TID}}$
“FEAST” AMAC regulators	–				–	0.415
Total FEAST	–				1	1.6755$^{*\text{TID}}$
Total Module (R1)	–					5.53*
			EOS			
VTRx: lpGBTx	1.2	0.625	0.750		–	
VTRx: GBLD 1.2V	1.2	0.0095	0.0114		–	
VTRx: GBLD 2.5V	2.5	0.018	0.045		–	
Total VTRx			0.8064		1	0.8064
GBTIA	2.5	0.053	0.1325		1	0.1325
FEAST					0.5†	0.35†
DCDC2				88%	0.5†	0.104†
Total EOS						1.4
EOS both sides						2.8

* Endcap R1 values. $^{\text{TID}}$ Affected by TID bump † One side of endcap EOS only

Thermal Model of the Module

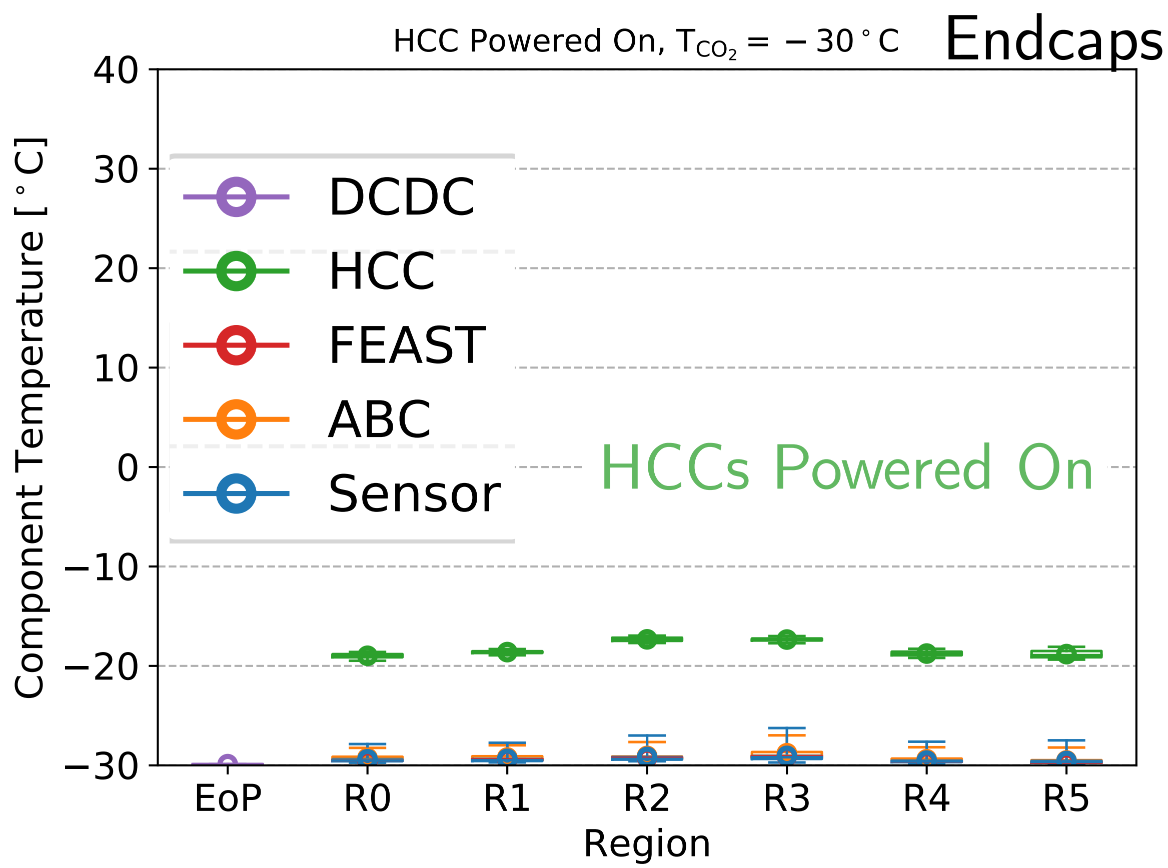
Cross-section of the
ATLAS ITk Strip module:

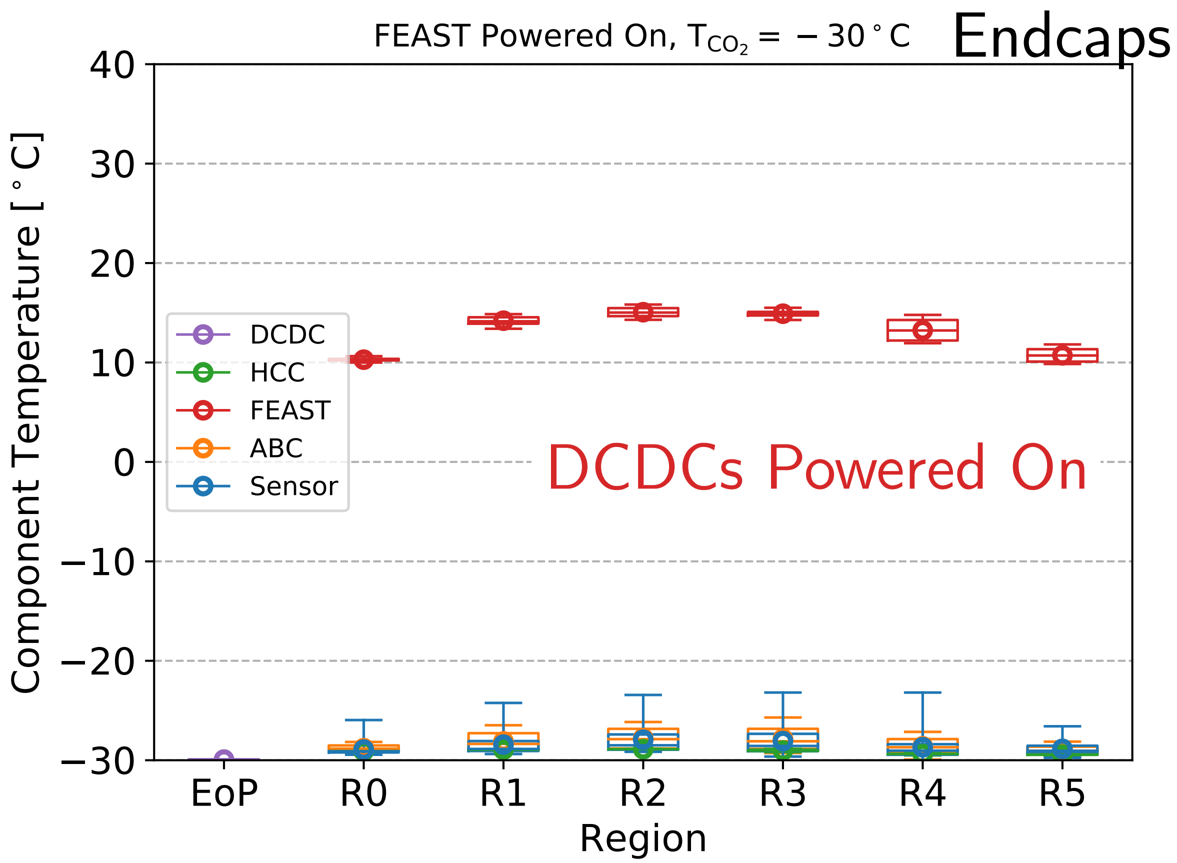


- Linear, 1-dimensional model
- Each component has its own effective thermal impedance
- Common thermal path between cooling pipe and silicon sensor
- Thermal impedances determined using FEA (see next slide)

Electrical	**Thermal**
Electrical resistance	Thermal resistance (R)
Current source	Power
Voltage	Temperature
$\Delta V = I \times R$	$\Delta T = P \times R$

Thermal Impedances: FEA Special Runs





etc…

- "Special FEA runs" powering each component type separately
- Three "special" runs total: HCCs, DCDCs, ABCs
- Four unknowns: R_{cm} and R_{HCC}, R_{ABC}, R_{FEAST} (system over-constrained)
- Solve for common thermal path resistance R_{CM} first – remaining R are trivial
  - If a component *x* is powered, its temperature is $\mathbf{\Delta T_x = P_x \times (R_x + R_{cm})}$ **(eq. 1)**
  - If a different component *y* is powered and x is off, $\mathbf{\Delta T_x = P_y \times (R_{cm})}$ **(eq. 2)**
  - Fit for Rcm using collection of (eq. 2) from each component;
  - Plug in Rcm to collection of (eq. 1) to solve for Rx for each component
- (Ignoring effects like cross-talk between modules)

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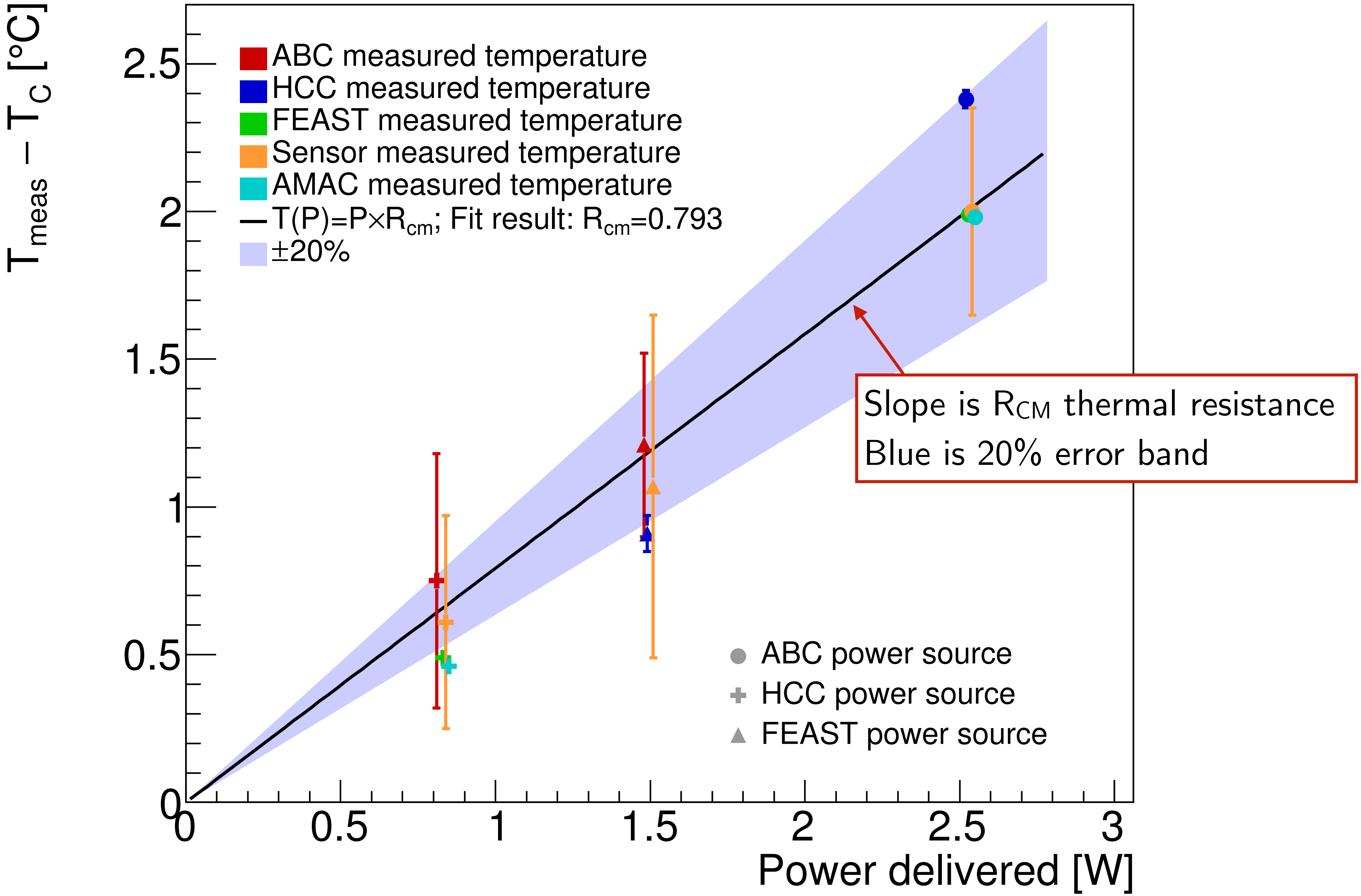
Fitting for common R_{CM}: An explanation

(Endcap Module R0)



Slope is R_{CM} thermal resistance

Blue is 20% error band

- To measure R_{cm}:

Notes on Thermal Impedances

- Summary of endcap thermal impedances:

Module	R_{cm} [K/W]	R_{FEAST}	R_{ABC}	R_{HCC}
R0	0.802	26.045	0.917	12.632
R1	0.991	28.256	0.671	12.744
R2	1.410	28.883	1.550	13.794
R3	0.873	29.333	0.566	6.812
R4	0.744	26.816	1.432	13.027
R5	0.596	27.450	1.034	13.177

- Barrel thermal impedances:

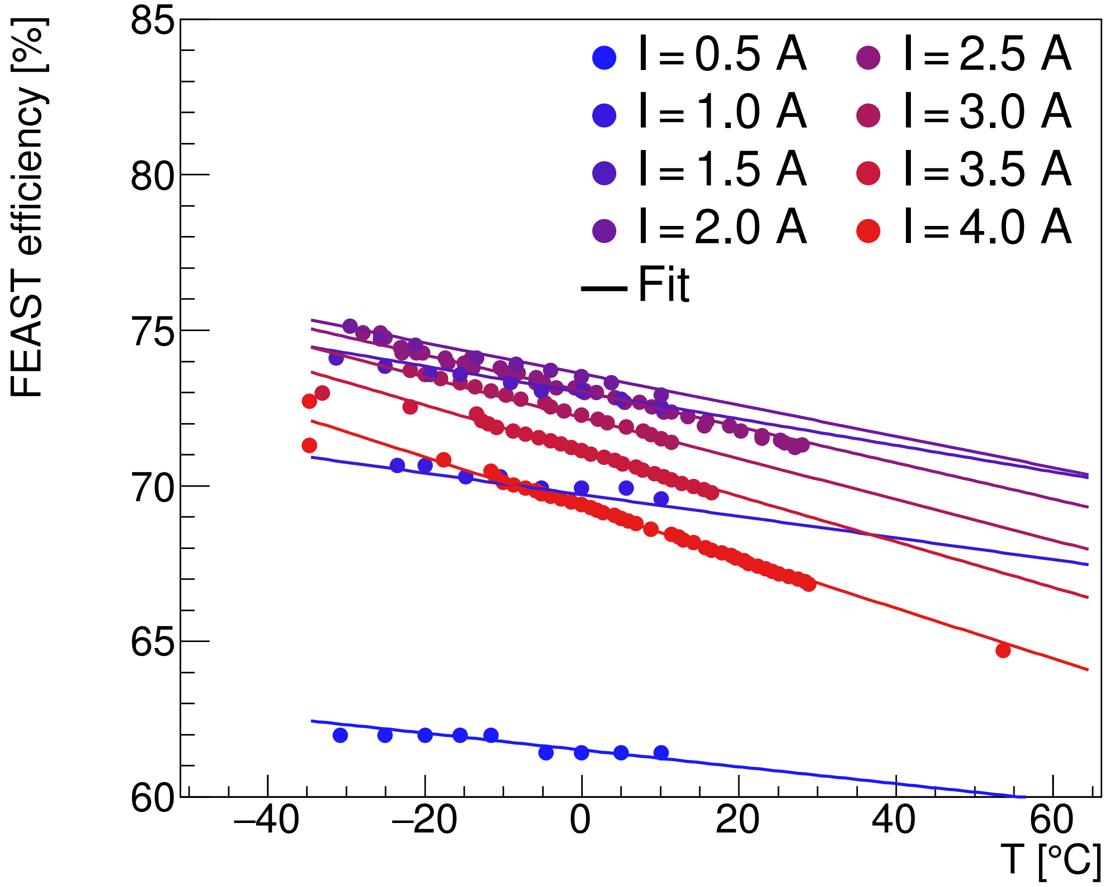
in [°C/W]	R_C	R_M	R_S	R_{EOS}	R_{ABC}	R_{HCC}	R_{FEAST}
Short strip module at EOS	0.890	0.222	0.02	15.0	1.003	12.305	19.650
Short strip module at middle	1.160		0.02	-	0.928	13.157	19.751
Long strip module at EOS	0.960	0.279	0.02	15.0	2.194	24.195	19.062
Long strip module at middle	1.360		0.02	-	2.141	25.174	19.663

- Notes
  - Could be some features caused by physical proximity of objects in some modules
  - Cross-talk could also cause other features

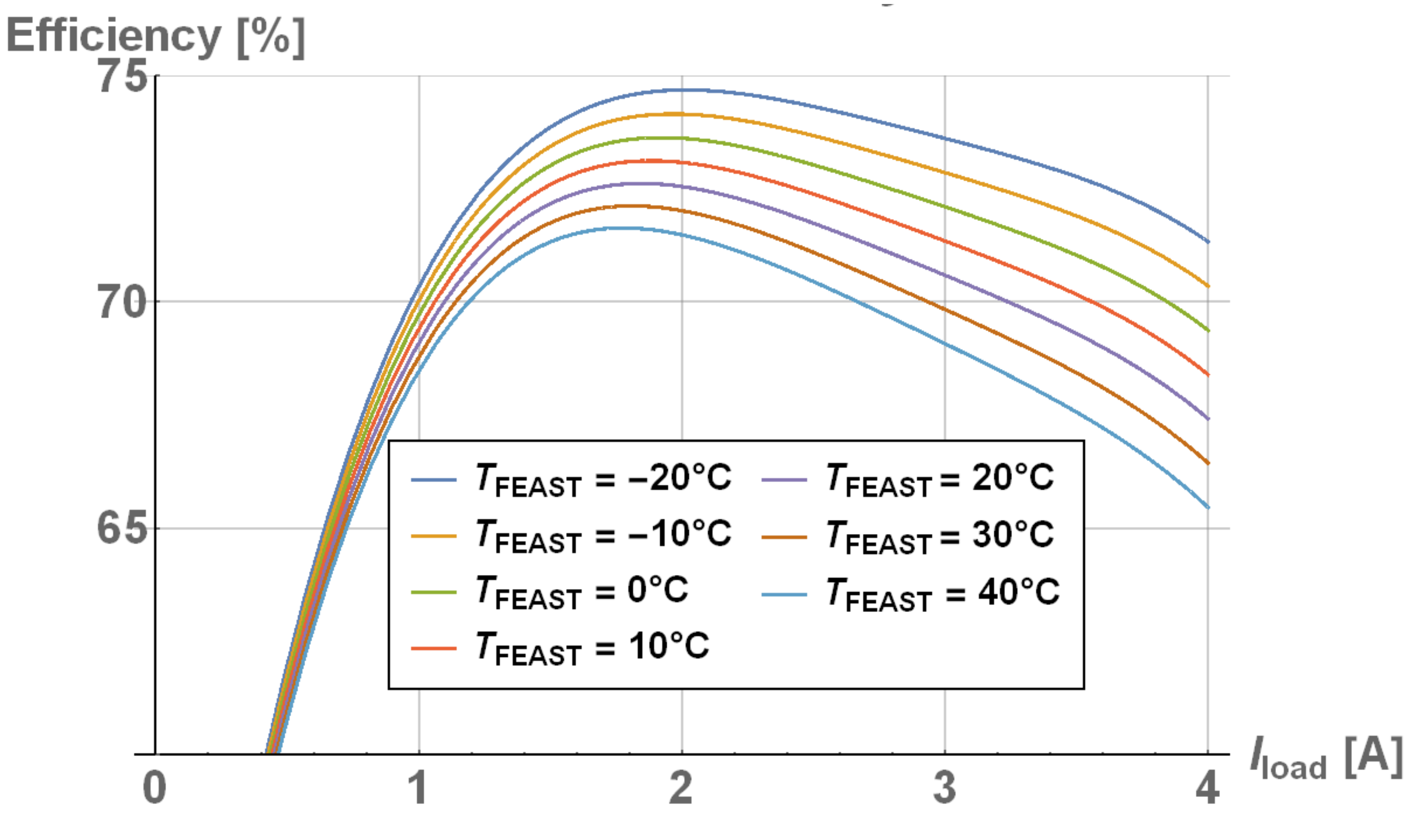
Other Inputs to the Model

- DCDC Converter efficiency dependence on temperature, current
- Readout chips affected by Total Ionizing Dose (“TID bump”)
- Flux and Total ionizing dose
- Operational profiles

Parameterizing DCDC Converter Efficiency



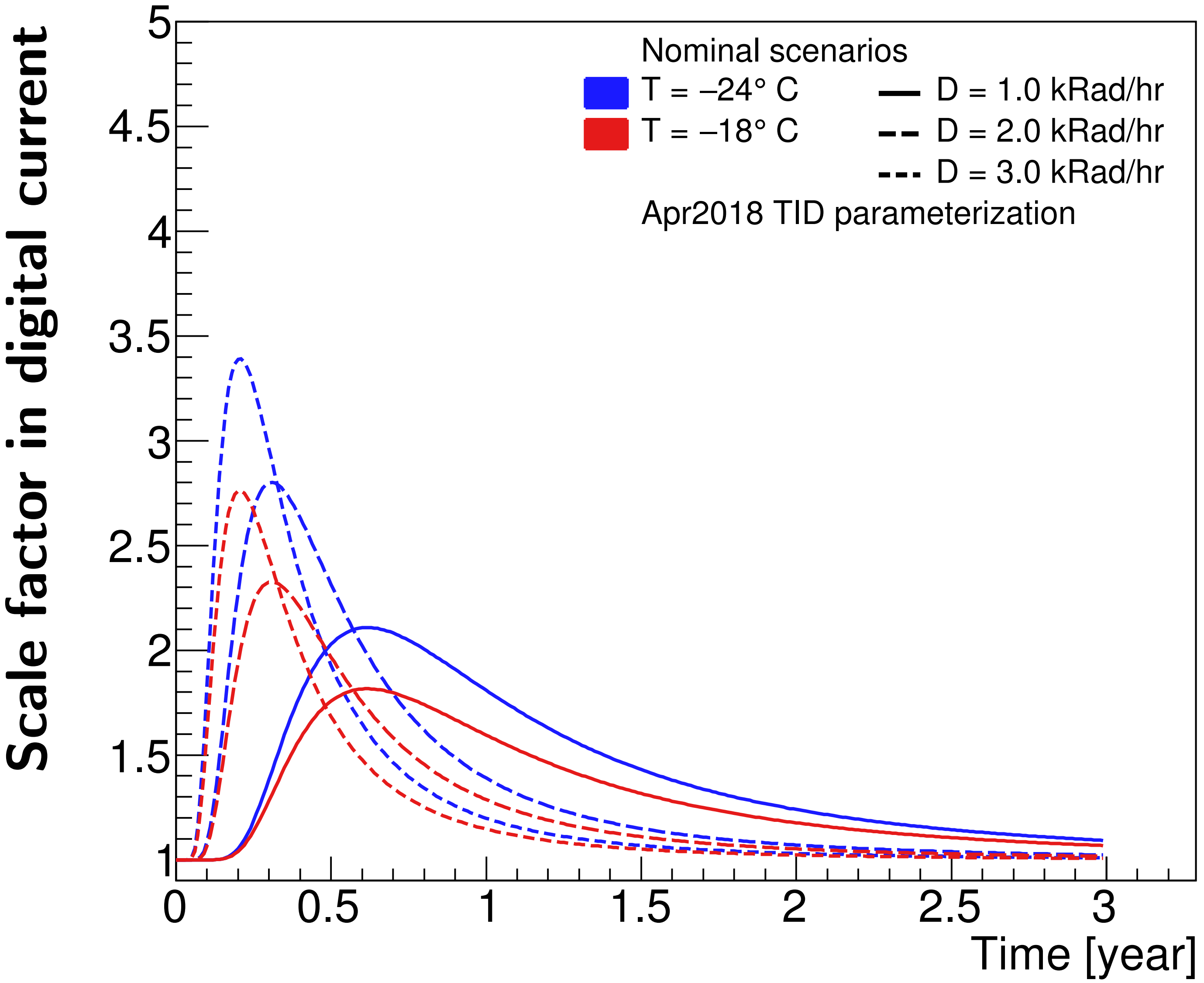
$$eff(I,T) = a + bI_{load} + cI_{load}^2 + dI_{load}^3 + eI_{load}^4 + fTI_{load} + gT$$



- DCDC converter efficiency is dependent on current and temperature
- Data measurements of efficiency vs load are fit to an “arbitrary function” for parameterized model
- When running the model we check that maximum current is (4A) is not exceeded

Input: TID Bump Characterization

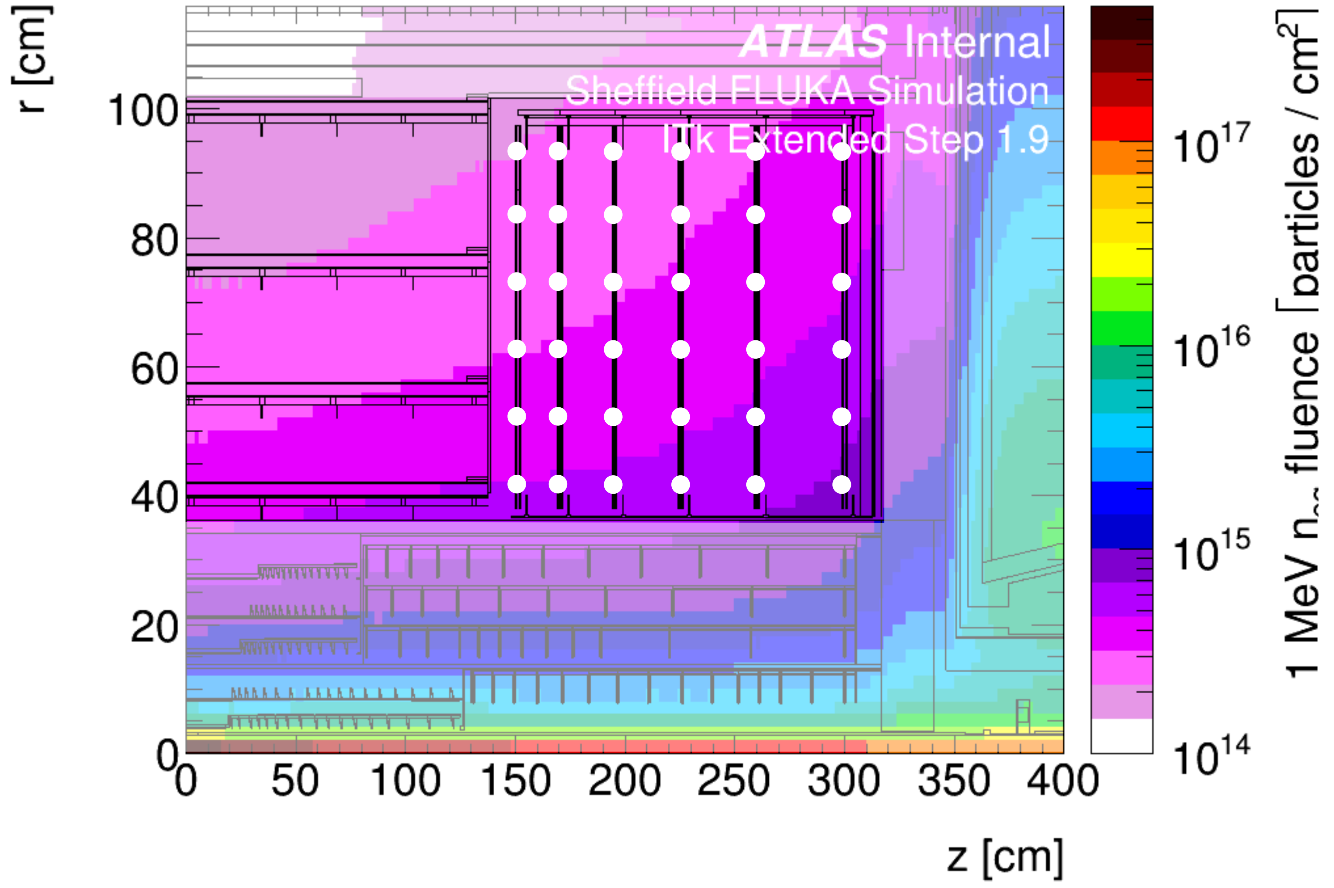
- Chips (ABCs, HCCs) digital current is affected by Total Ionizing Dose - "TID Bump"
- Parameterization shape picked to match data
- The scale of the bump depends on the <u>temperature</u> and <u>dose rate</u>
  - TID bump is bigger at <u>lower temperatures</u>
  - TID bump is bigger at <u>larger dose rates</u>
- Increase in current affects performance of DCDC converter, total EC power requirements, etc.
- Note that dose-rate dependence causes shifts in the timing of the peak



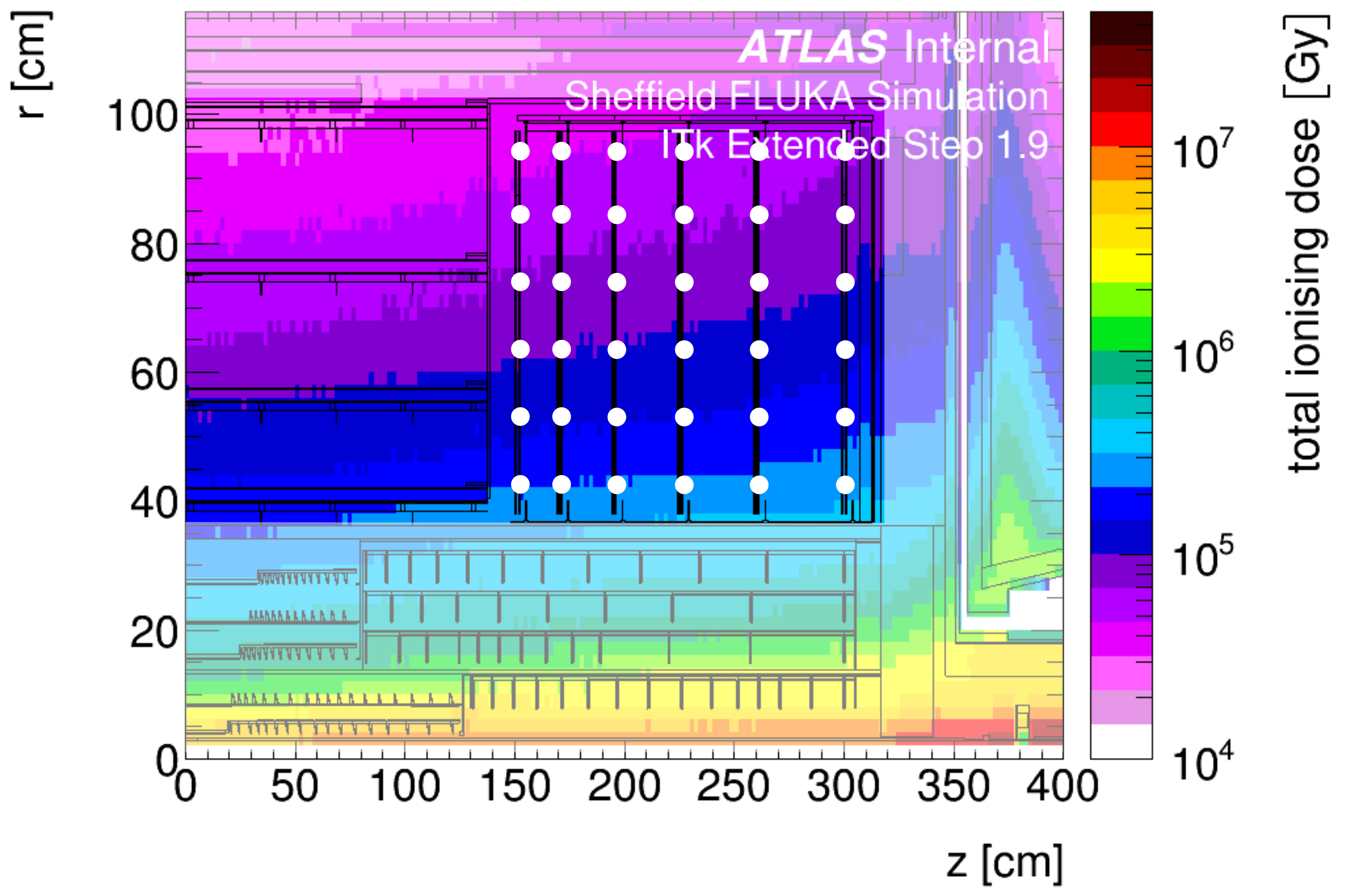
Modeling of Flux / Total Ionizing Dose

- Barrel: Flux and TID is relatively stable across horizontal staves
- Endcap: Large variations in flux and TID, so we model each module (36 total) with its own flux and TID

Particle Fluence (1 MeV n_{eq})

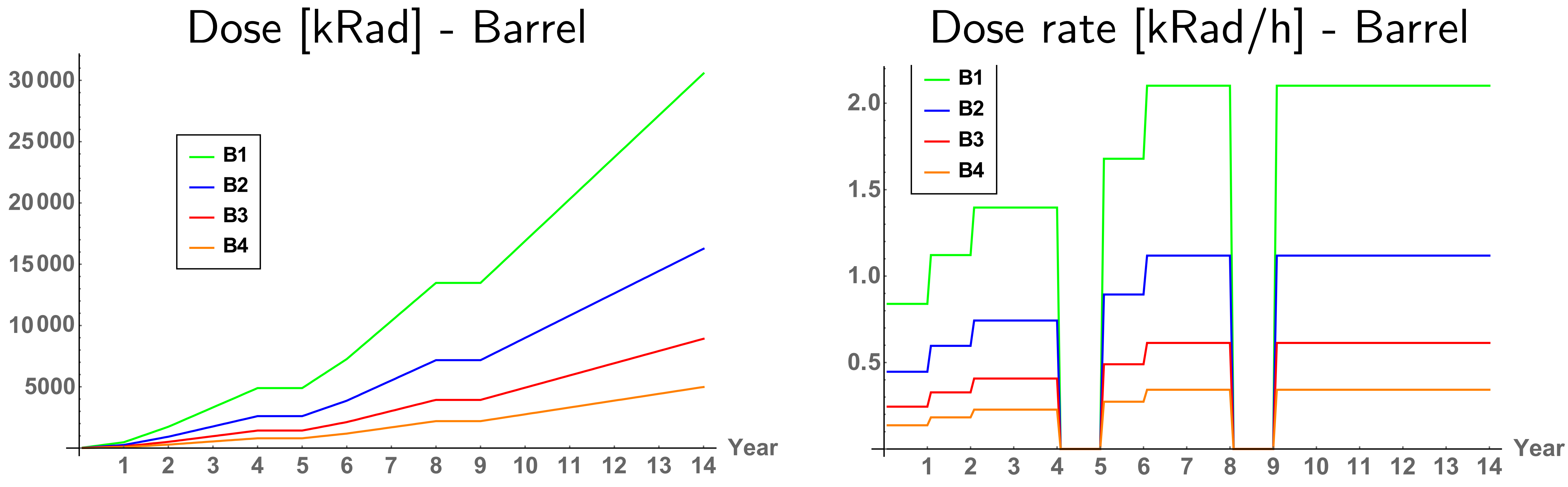


Total ionizing dose (TID)



- Flux in the range 2–5×10^{14} n_{eq}/cm^2
- TID in range 4.7–22.7 kRad

Operational Profiles



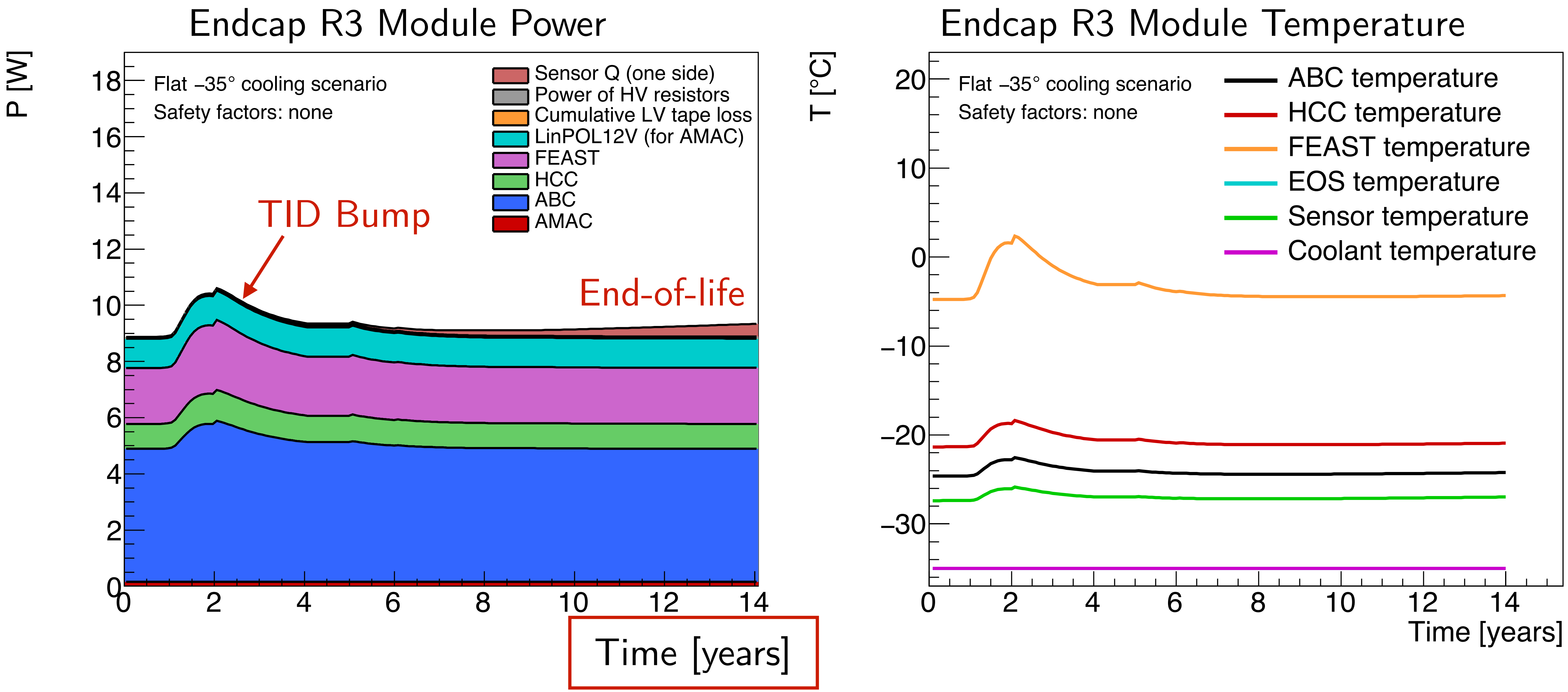
- HL-LHC plans to collect 3-4000 fb^{-1} over 14 years
- Thermoelectric Model is run in 1-month steps...
- ... using output temperatures from previous month as inputs to the next month
  - ABC, HCC currents are temperature-dependent (TID bump)
  - DCDC efficiency temperature-dependent
  - Sensor leakage current temperature-dependent

Model's skill is handling interdependencies

Model Outputs

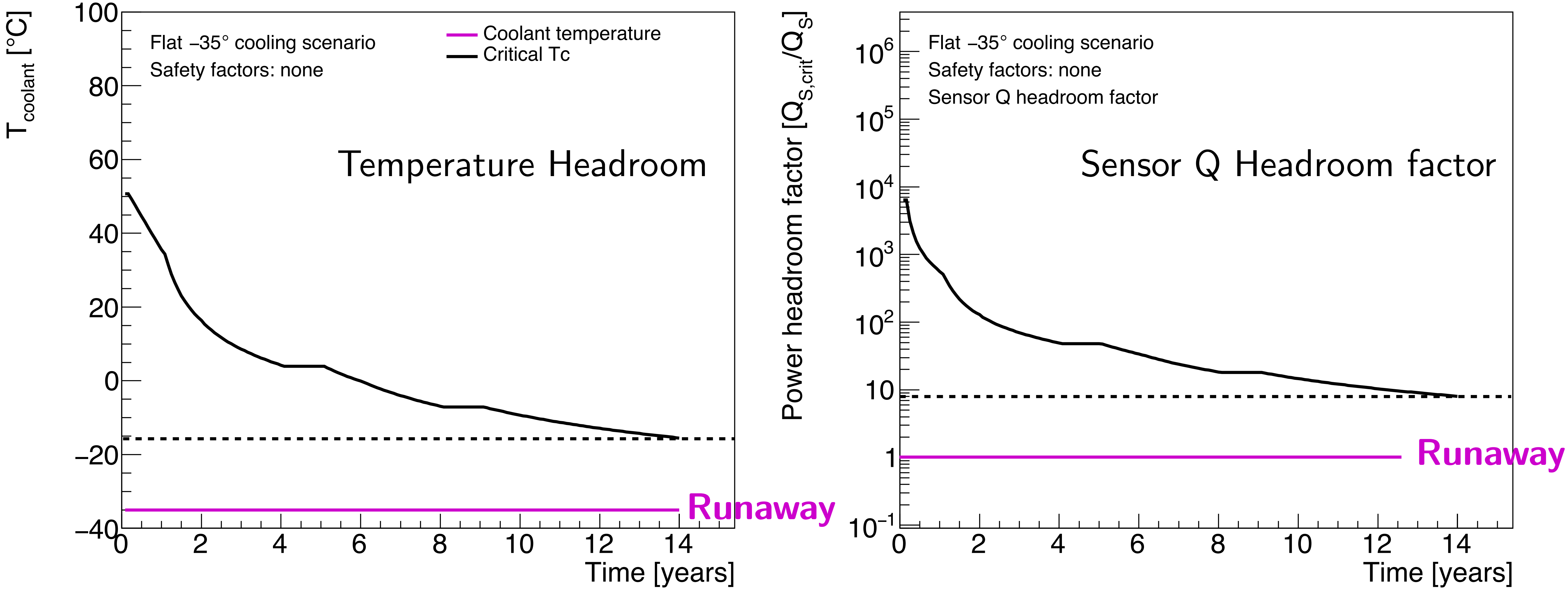
Model Outputs

Power and Temperature outputs, one Module



- TID bump increases chip currents
- → lower DCDC efficiencies, more power in DCDC
- → higher temperatures in all components, sensor
- → temperature-dependent TID bump decreases (damping effect)

Temperature and Sensor Q Headroom

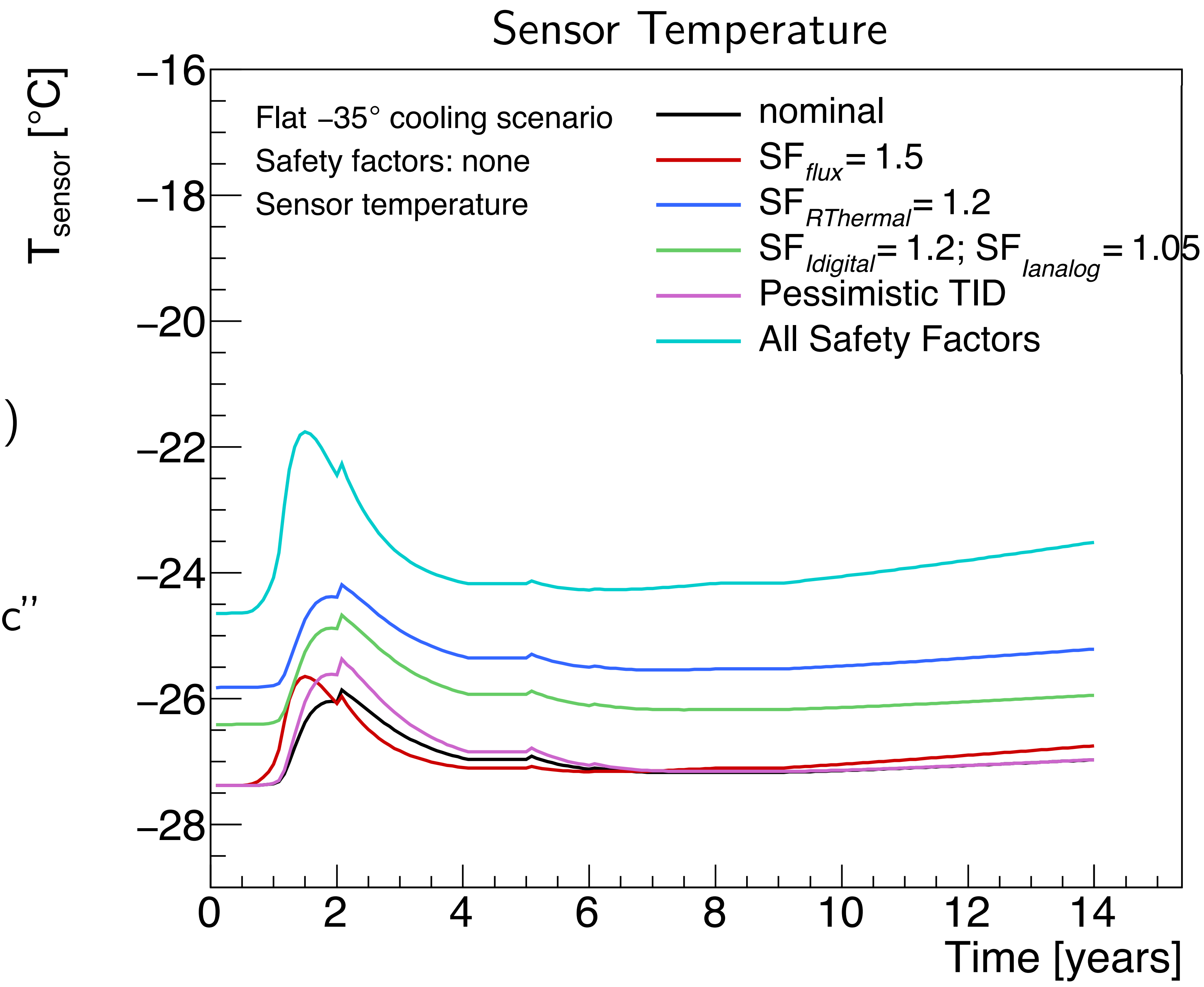


- Sensor Q Headroom factor:
  - Sensor leakage power factor Q_{Max}/Q_S before thermal runaway is reached
- Coolant temperature headroom factor:
  - Maximum coolant temperature before thermal runaway is reached

Scenario Comparisons – Safety Factors

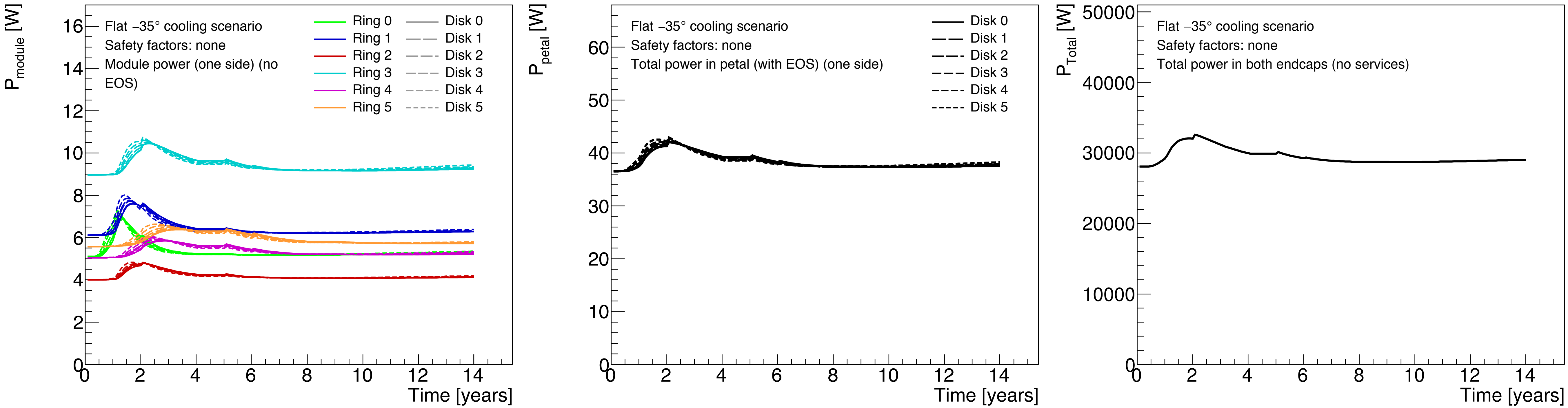
- With the thermoelectric model, opportunity to compare different scenarios
  - E.g. update power/currents of components
  - Test different scenarios
  - Apply different safety factors (below)

Flux / Total Ionizing Dose: +50%
Thermal Resistance: +10% (+20% EC)
Digital current: +20%
Analog current: +5%
TID bump parameterization: "pessimistic"



Model can predict Global System Requirements

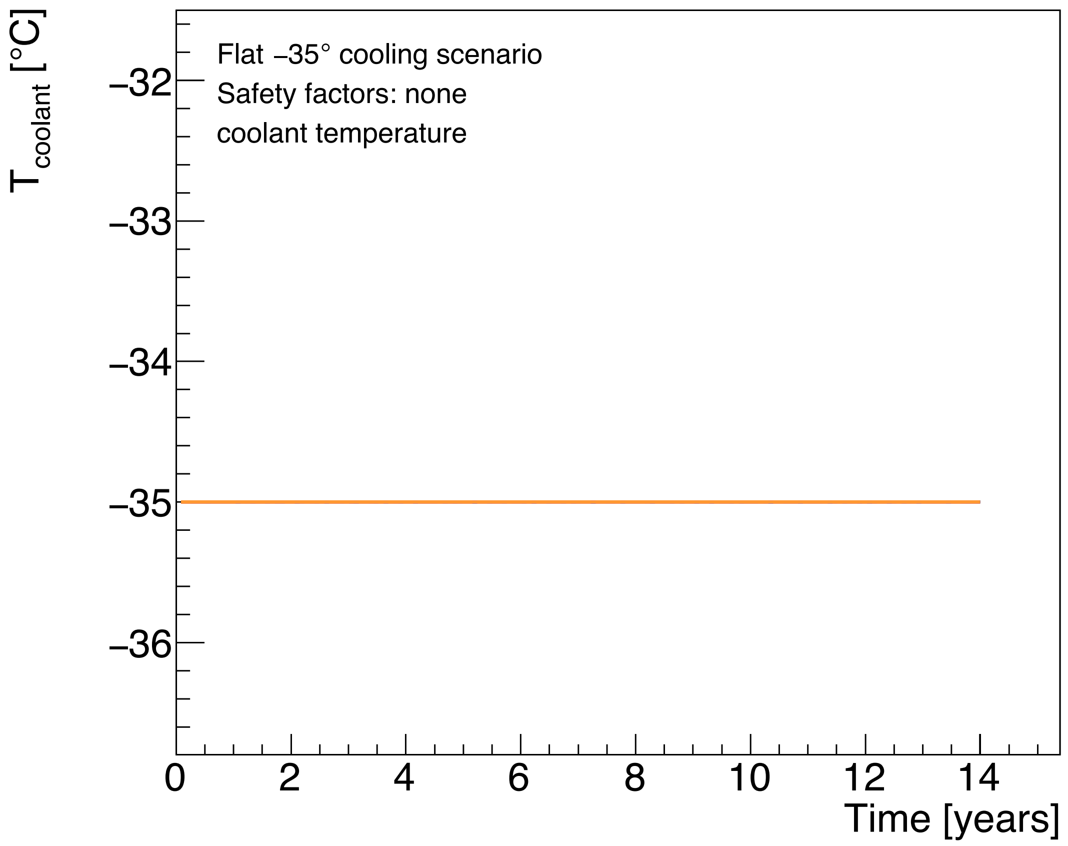
Individual ECModules → Petals → Full Endcap System

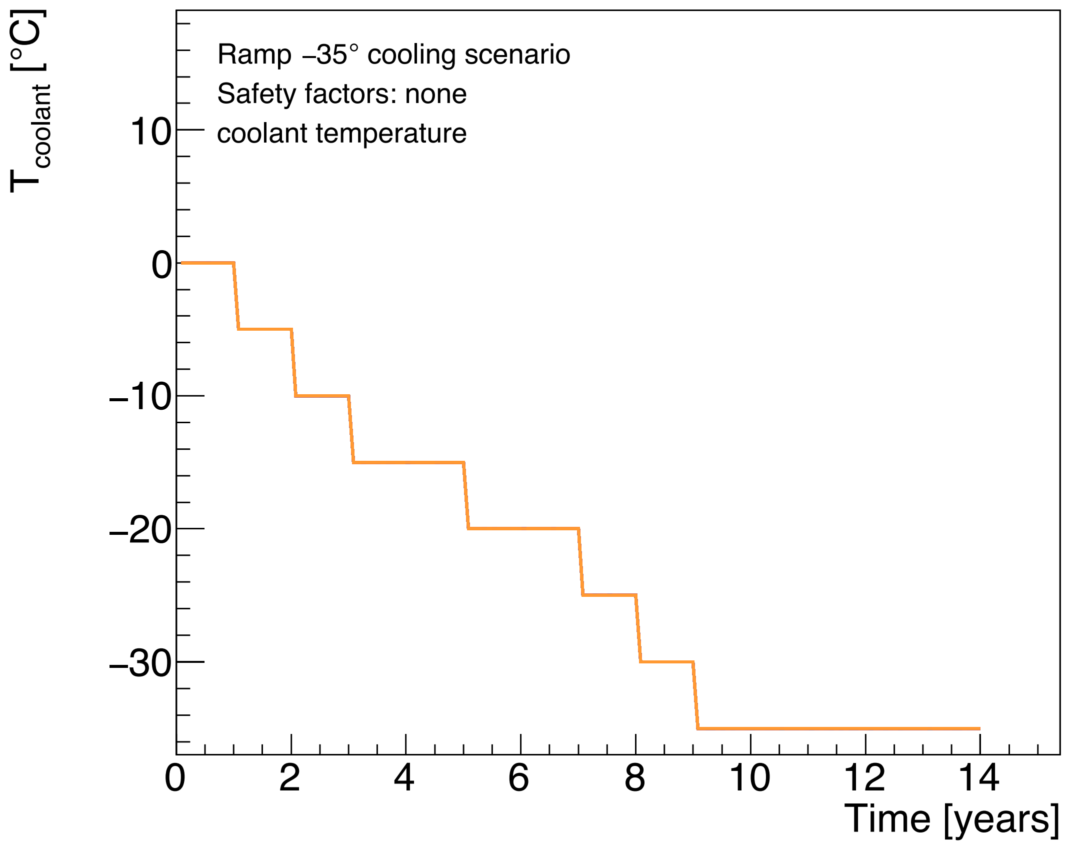


- Module-level effects can be propagated, to model the full system
- Note that maximum power is not the sum of the individual module maxima (offset TID peaks)
- Can be used to understand requirements for e.g. cables, cooling system

Testing Different Coolant Temperature Scenarios

Testing Different Cooling Temperature Scenarios

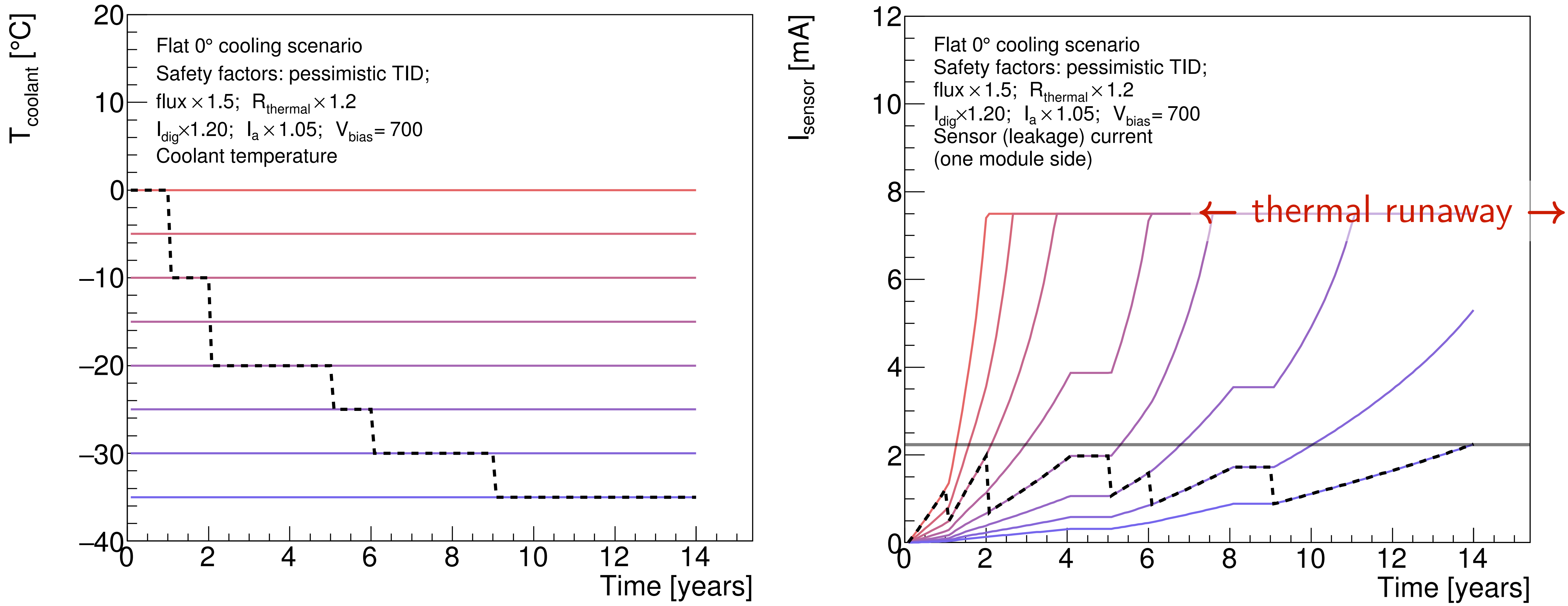




- Nominal coolant temperature scenario is –35°C
- Can try different cooling scenarios to optimize for certain effects:
- e.g. TID bump (~year 2) is mitigated with higher temperatures
- e.g. Thermal runaway (end-of-life) is avoided using lower temperatures

Test the effect on the endcap modules

Trying Different Temperature Scenarios (II)



- Example: use model to find a "ramp" scenario to keep sensor current < 2 mA at all times
- Note: Cannot expect perfect accuracy from this type of tuning

Benefits of a Thermoelectric Model

Input for Design Issues:

- Petal design with DCDC converter exceeding 4A maximum specification
- Input for chip designers to guide maximum allowable chip currents
- Avoiding scenarios with thermal runaway
- Choosing among materials with different thermal conductivity

Specifications:

- System-wide: Maximum power load on the cooling system
- Load on bus tapes (LV, HV)
- Load on LV and HV cables
- Etc.

Conclusions

Benefits of an analytic Thermo-electric model:

- Indispensable tool for understanding full detector system
- Qualitative understanding of module, detector operation
- Allows fast comparison of multiple scenarios, safety factors

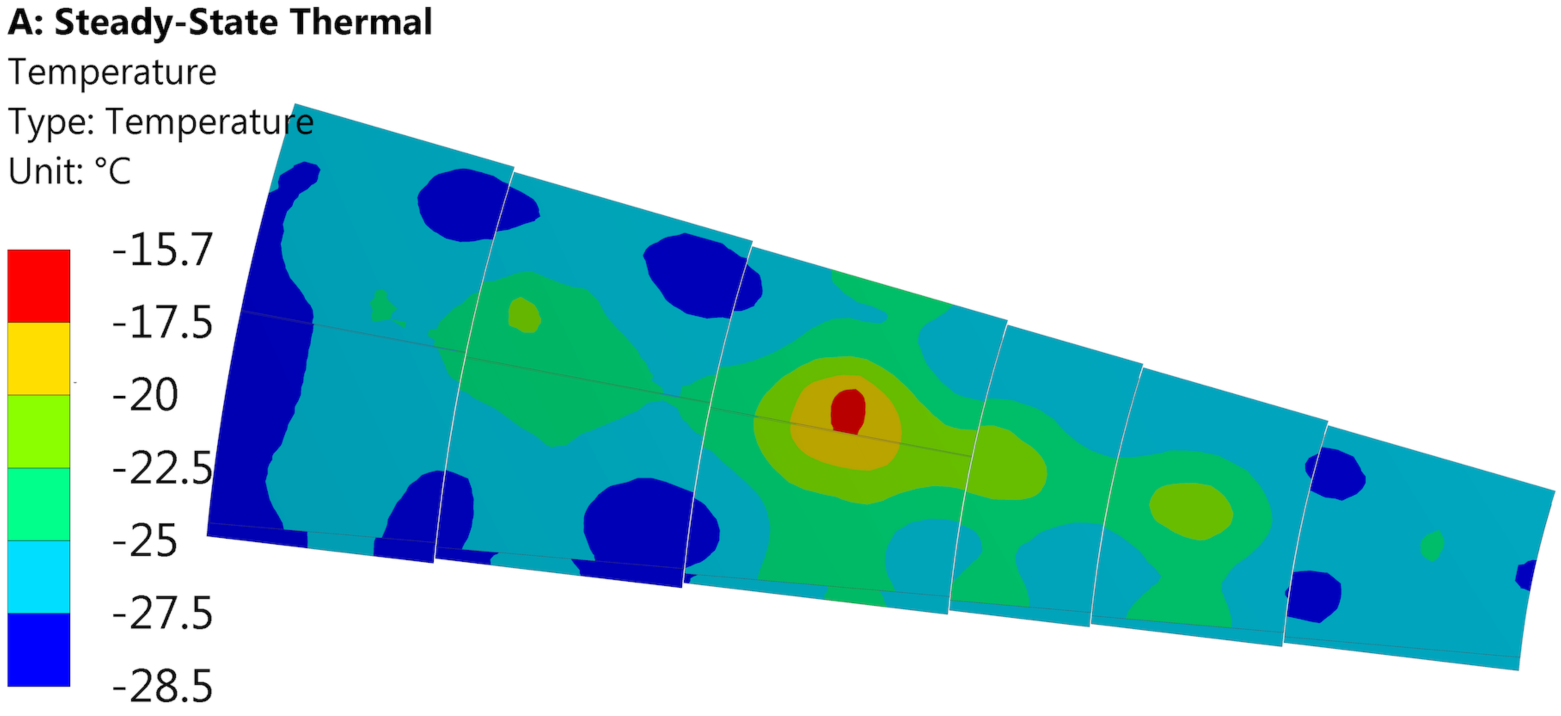
Caveat / Reminder:

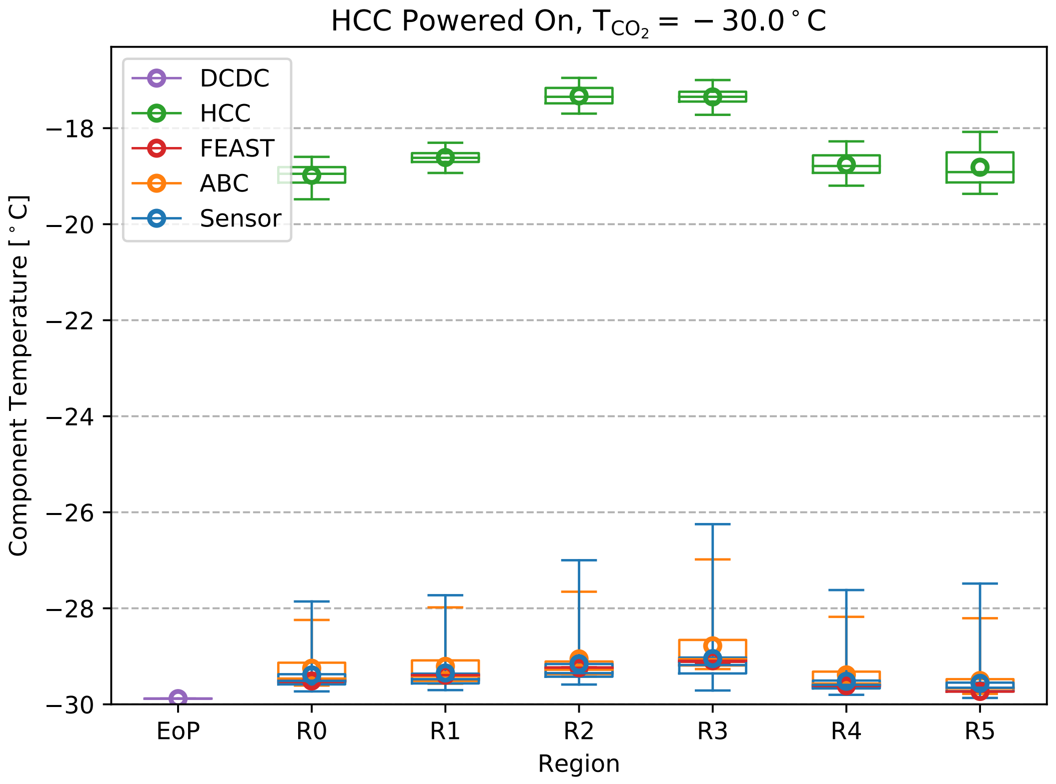
- Thermoelectric model is only as good as the inputs
- Important to understand the individual components of the module:
  - FEA Simulation
  - Data collection: chips, DCDC converters, regulators, etc.

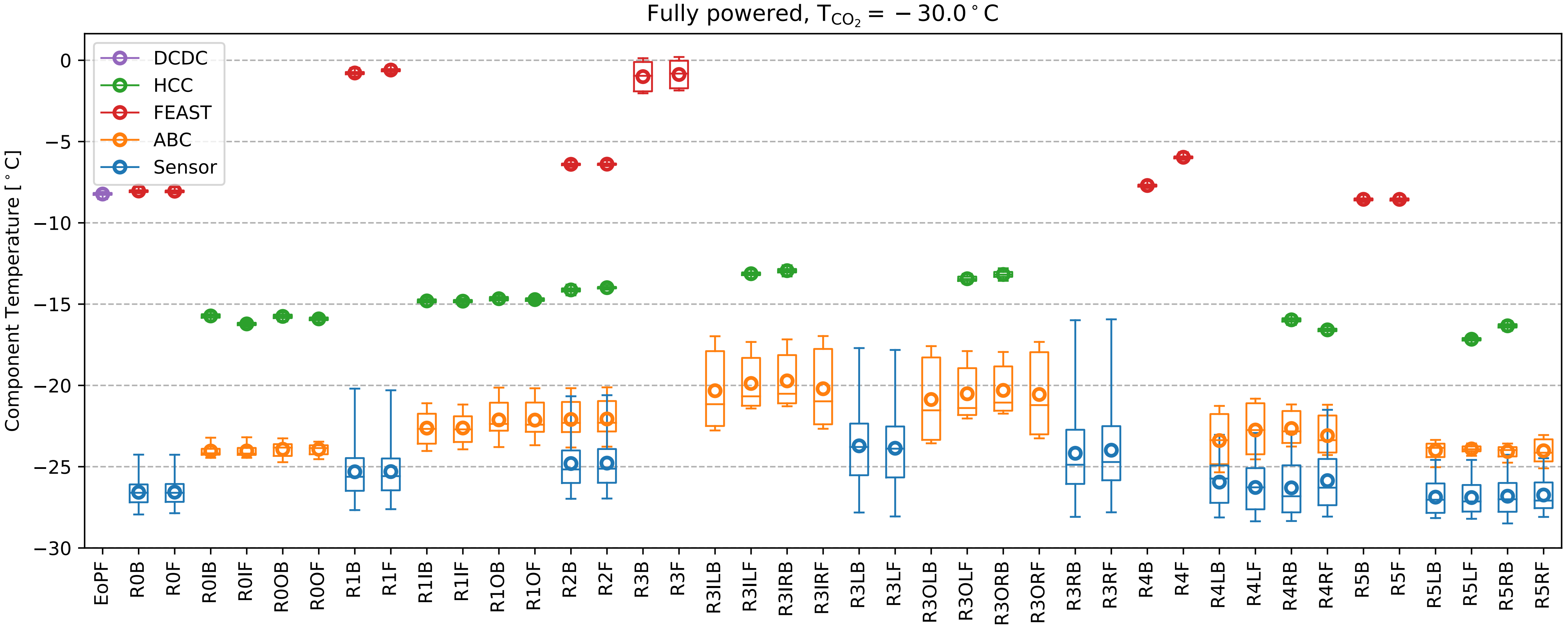
Backup

BACKUP

Full Endcap FEA results, T_{Coolant}=30°C







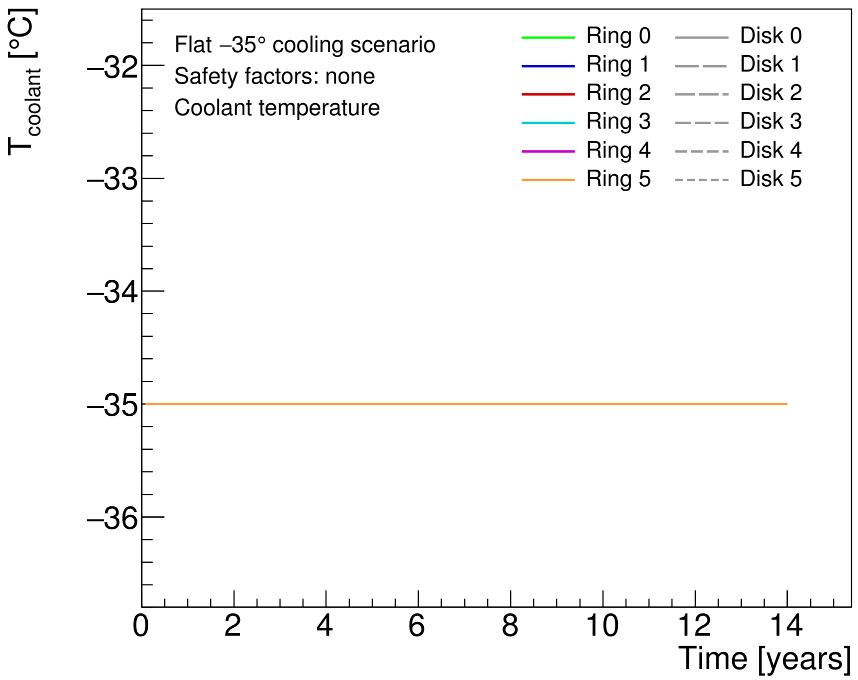
Thermal properties input to the FEA - Endcap

Table 2.3: Thermal properties used as input to the FEA [1].

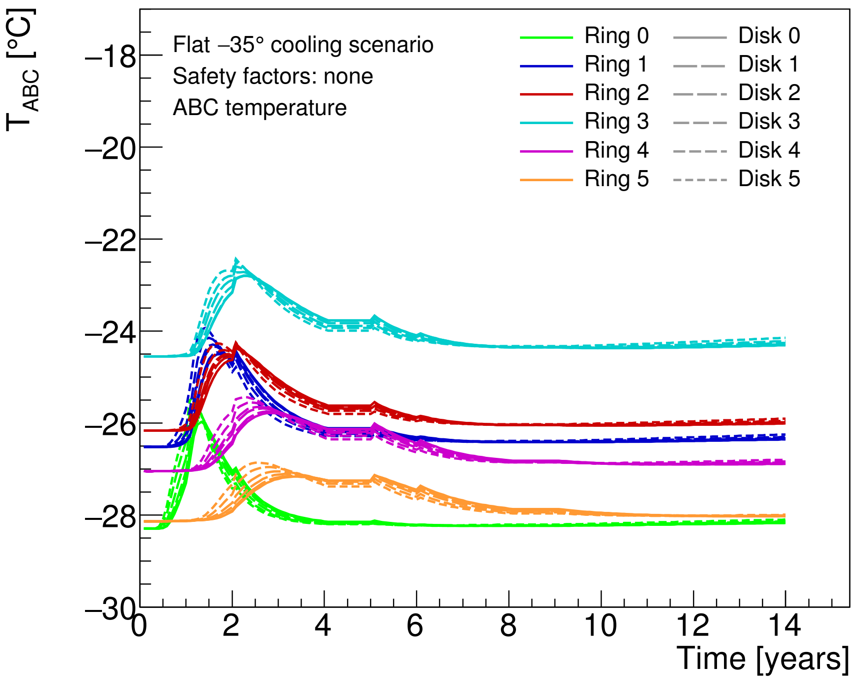
Part or Interface	**Material**	$K_x/K_y/K_z$ $[\mathrm{W\,m^{-1}\,K^{-1}}]$	**Thickness [mm]**	**Comment**
ASIC	Silicon	191 (250K) - 148 (300K)	0.30	
ABC to Hybrid	UV cure glue	0.5	0.08	50% coverage
HCC to Hybrid	UV cure glue	0.5	0.08	75% coverage
Hybrid PCB	Cu/polyimide	72 / 72 / 0.36	0.2	
Power PCB	Cu/polyimide	120 / 120 / 3	0.3	
PCB to sensor	FH5313 Epolite	0.23	0.12	75% coverage
Sensor	Silicon	191(250K) - 148(300K)	0.3	
Sensor to Bus	DC SE4445	2.0	0.1 - 0.2	100% coverage
Bus tape	Polyimide/ Cu/Al	0.17 / 0.17 / 0.17	0.24	
Bus to facing	-	(idealised)	-	co-cured
CFRP Facing	0-90-0 CFRP	180/ 90 / 1	0.15	K13C2U fibre, 45 g/m^2
Facing to Foam	Hysol 9396 + graphite powder	1.0	0.1	
Graphite Foam	Allcomp, 2g.cm-3	30	5 mm (core)	
Foam to Pipe	Hysol 9396 + graphite powder	1.0	0.1	
Cooling Pipe	Titanium (grade 2)	16.4	0.14-0.15 (wall)	2 mm inner dia.
Fluid film	Bi-phase CO_2	HTC 4.9 to 7.1 (at BoL) [a] $[\mathrm{kW\,m^{-2}\,K^{-1}}]$		simulated at -30 °C
Convection	Air	HTC 0 to 15 (13.7 °C) $[\mathrm{W\,m^{-2}\,K^{-1}}]$		adjusted to match

Endcap Temperatures, –35° C cooling scenario

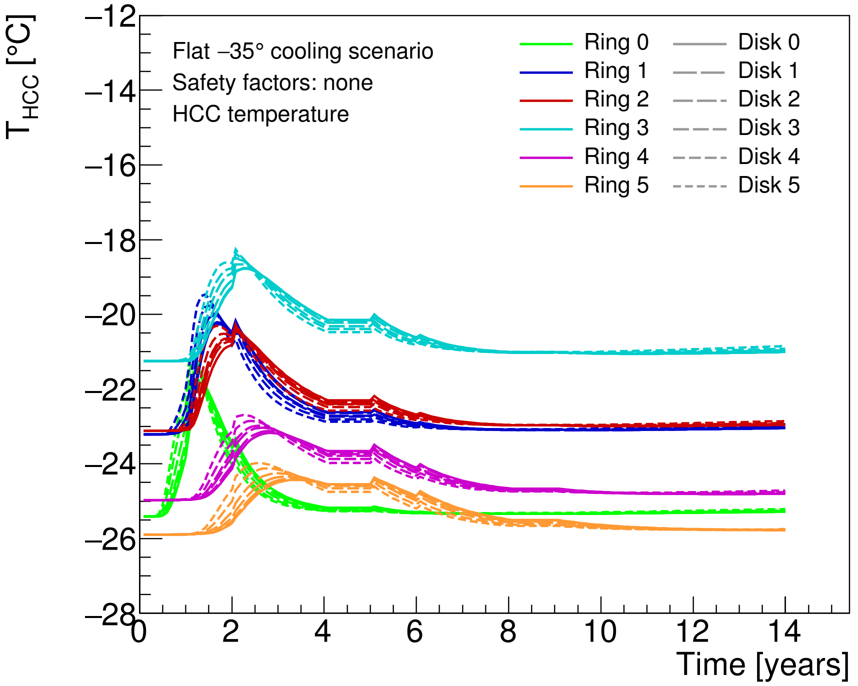
Coolant Temp



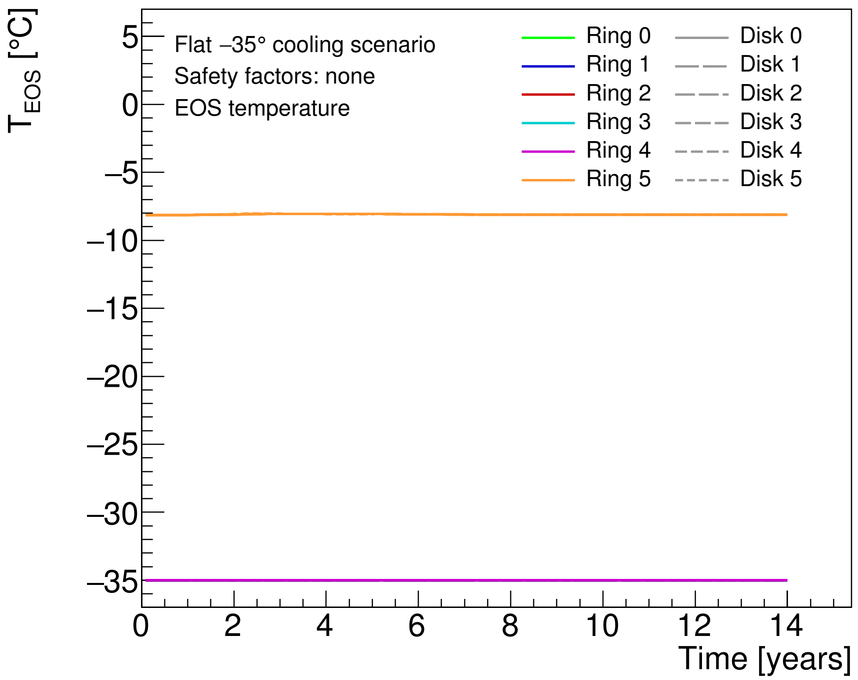
ABC Temp



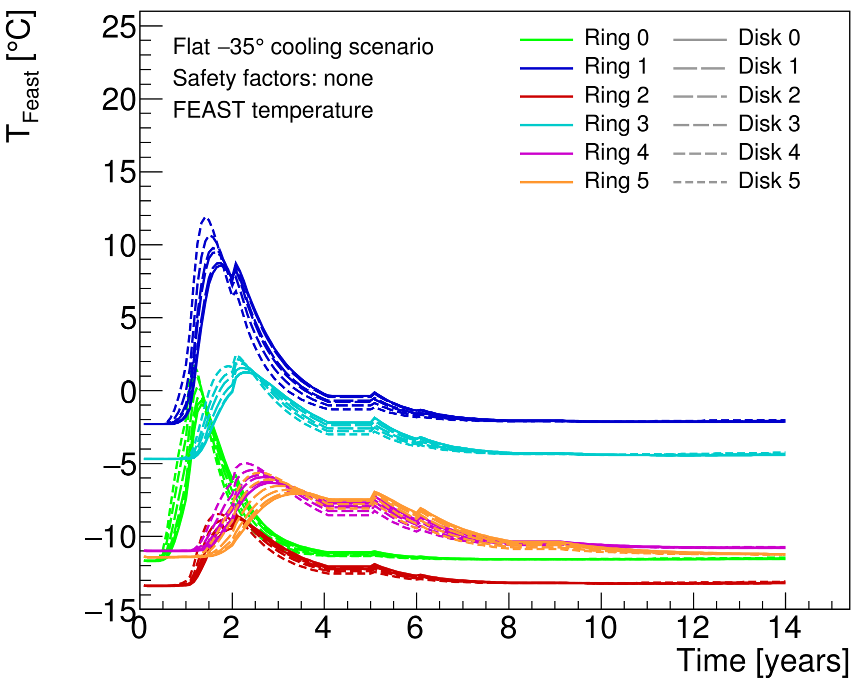
HCC Temp



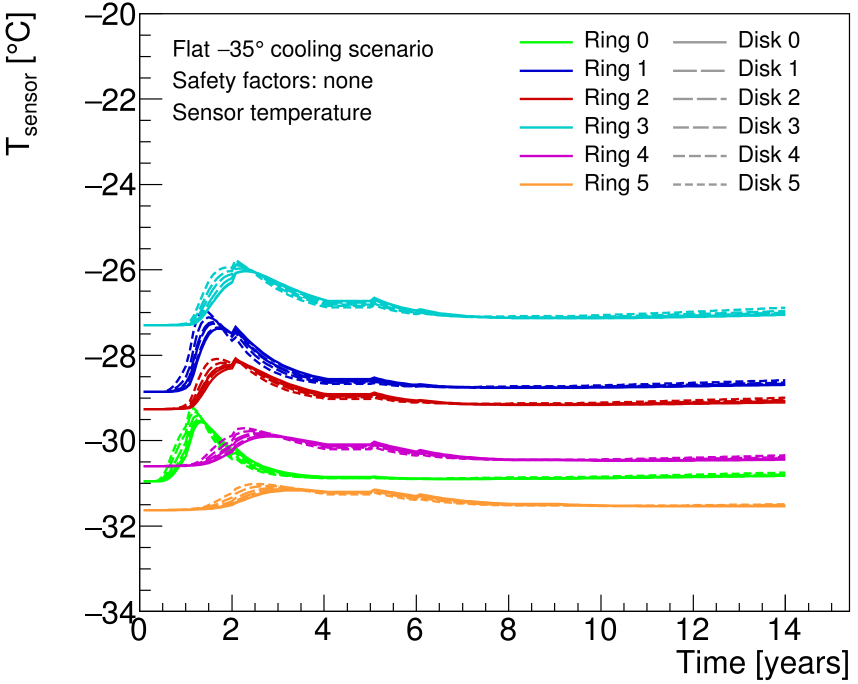
EOS Temp



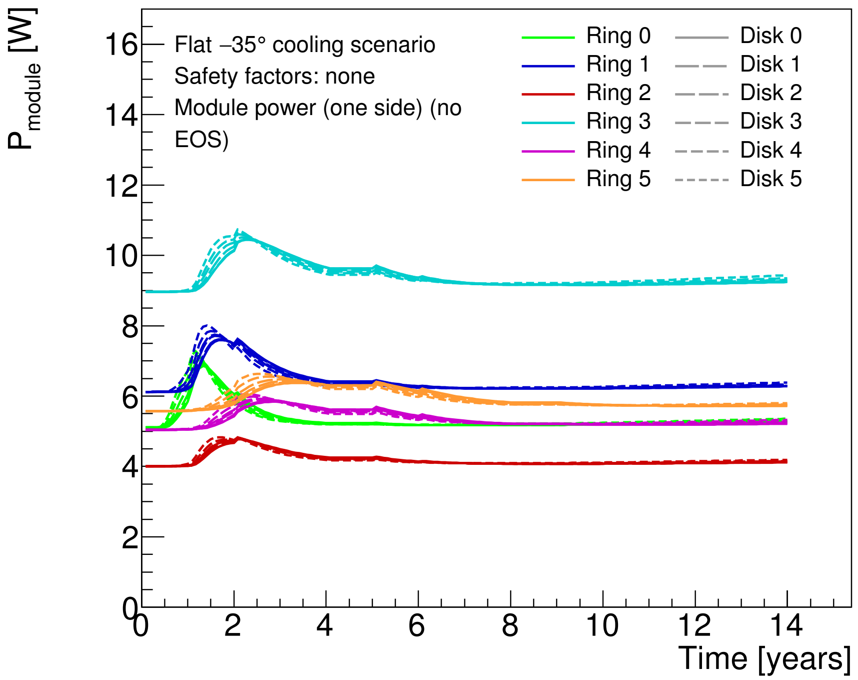
FEAST Temp



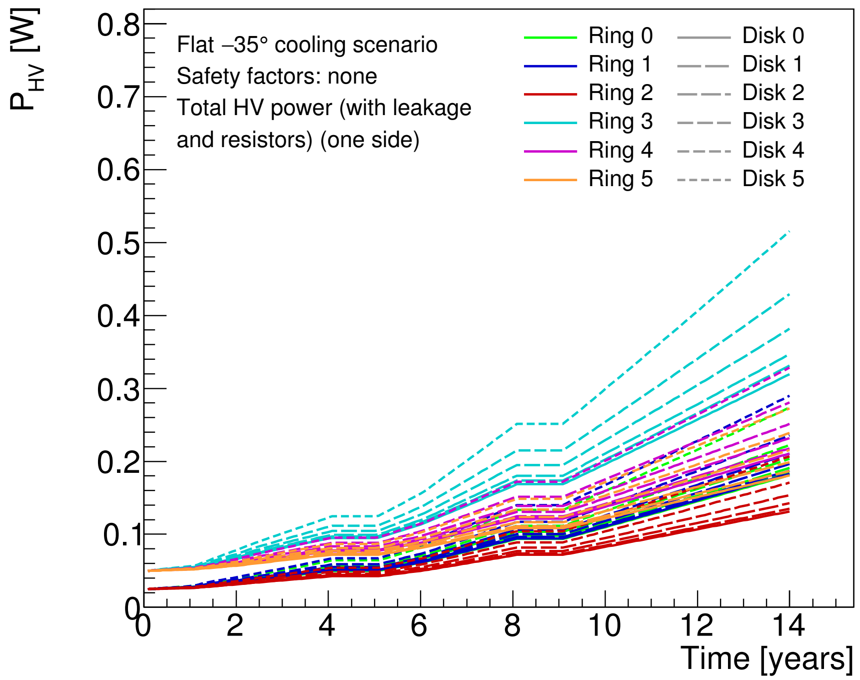
Sensor Temp



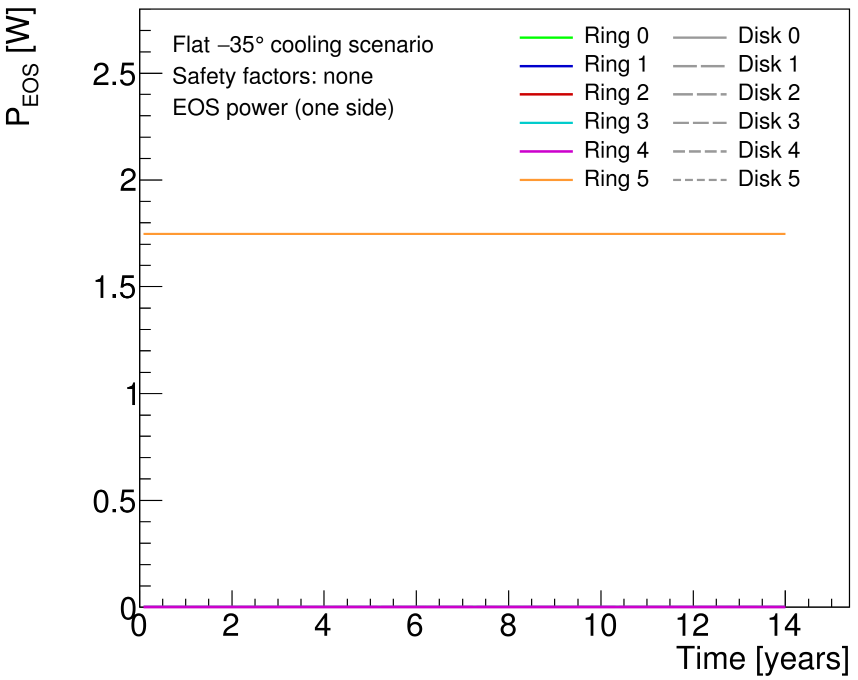
Endcap Power and current, –35° C cooling scenario



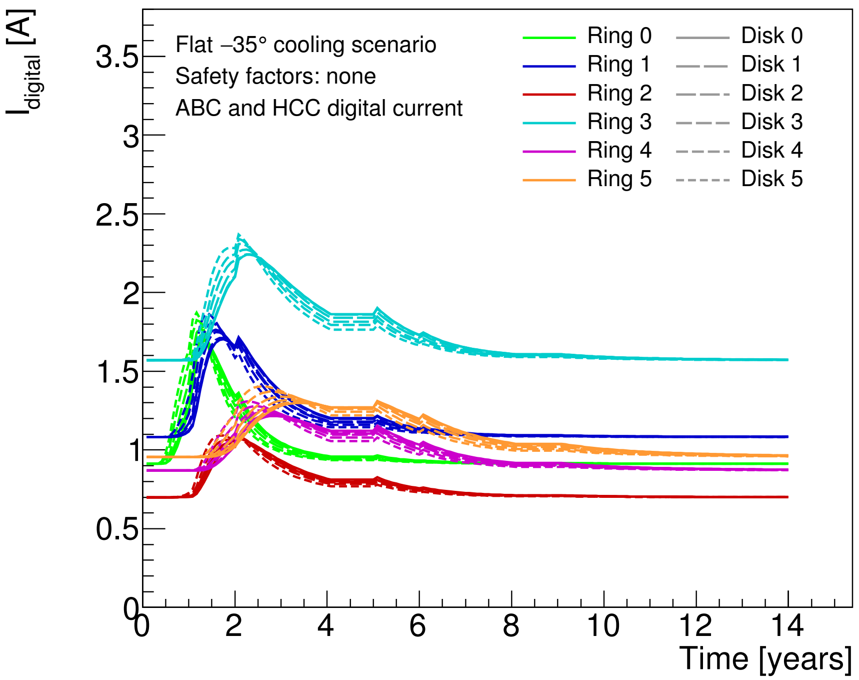
Module Power



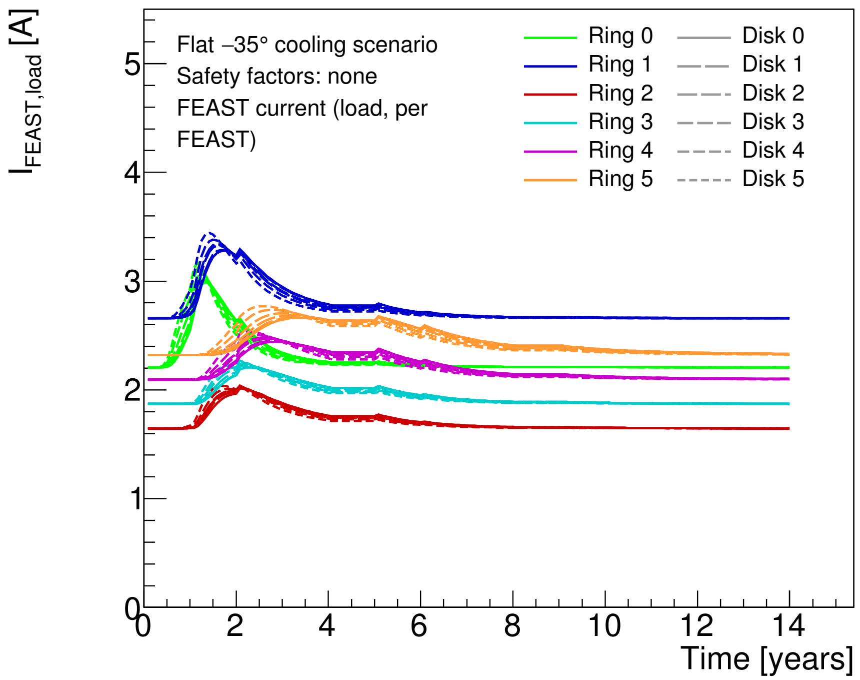
HV Power



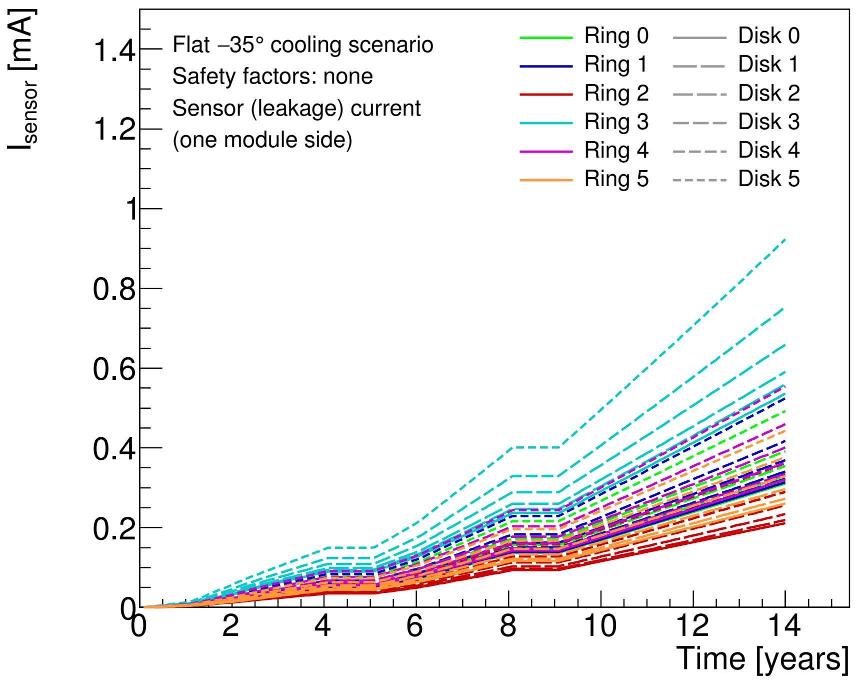
EOS Power



Digital Current



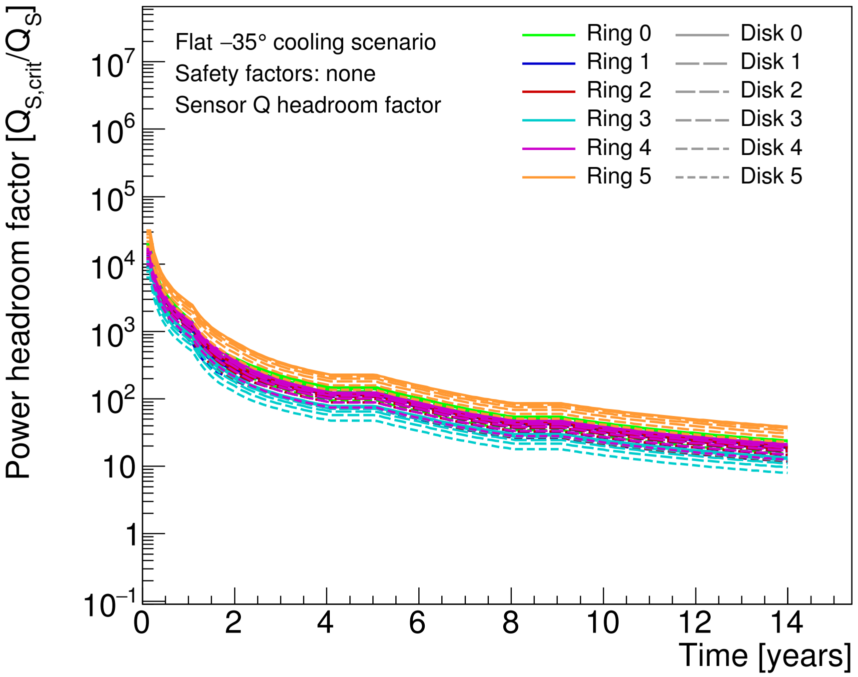
FEAST Current



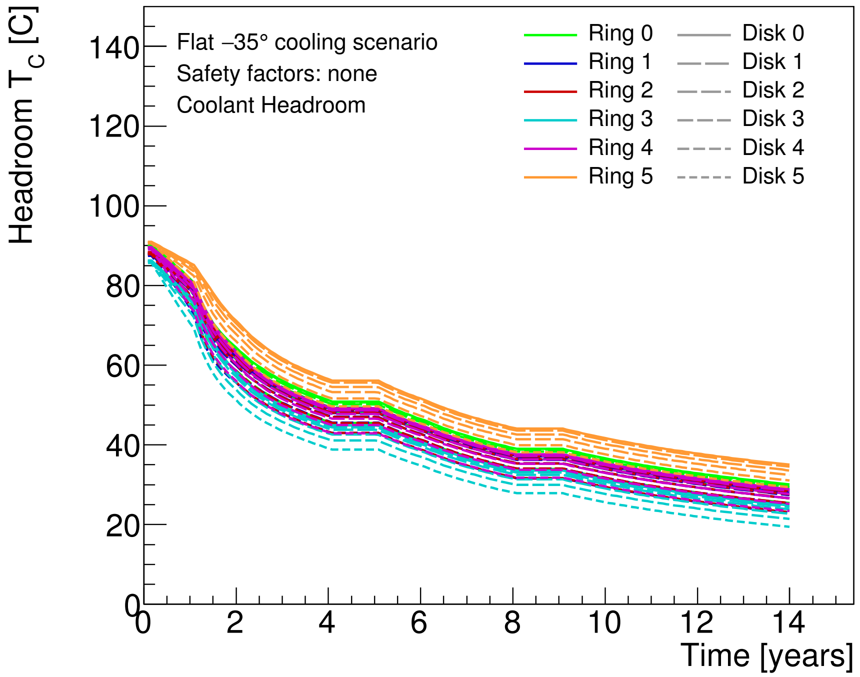
Sensor Current

Endcap – Other, –35° C cooling scenario

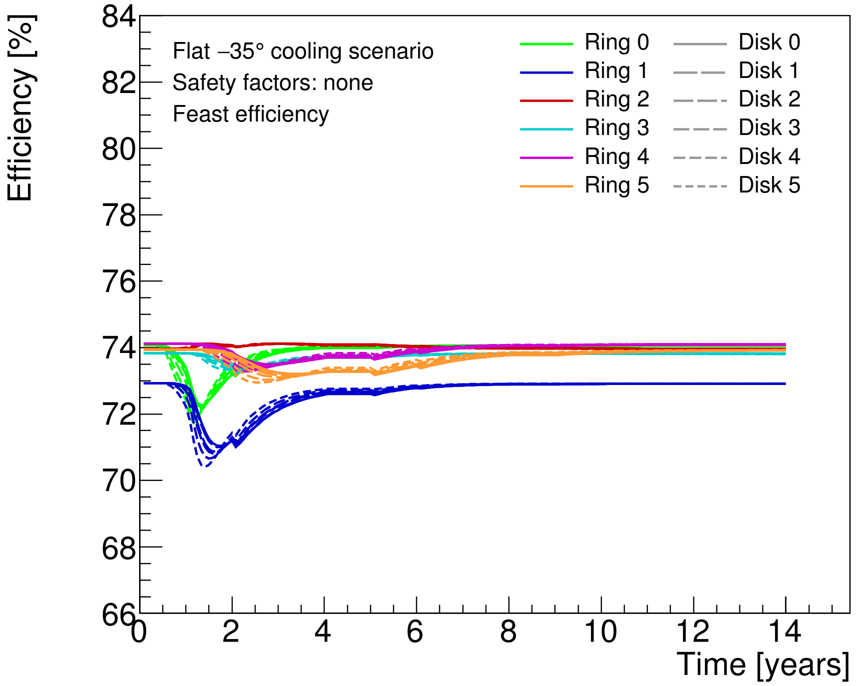
Sensor Power Headroom Factor



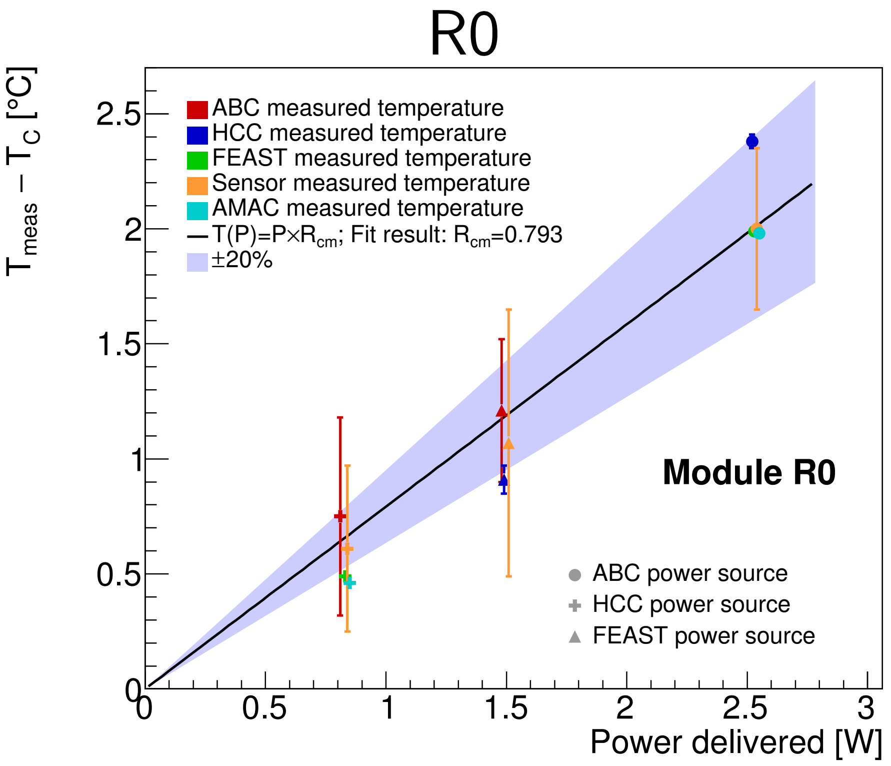
Coolant Headroom

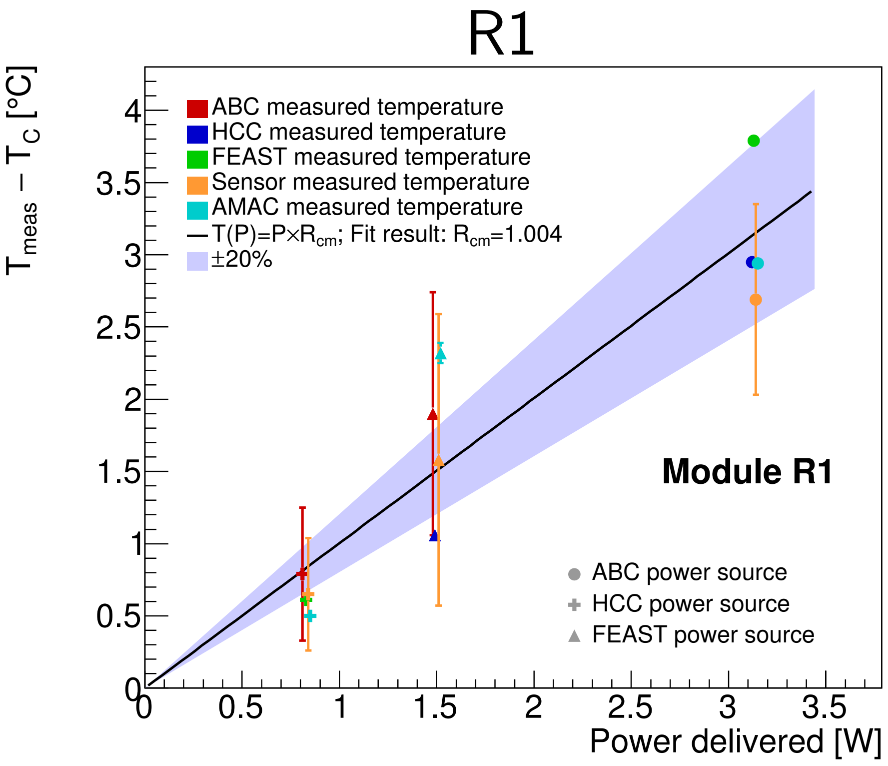


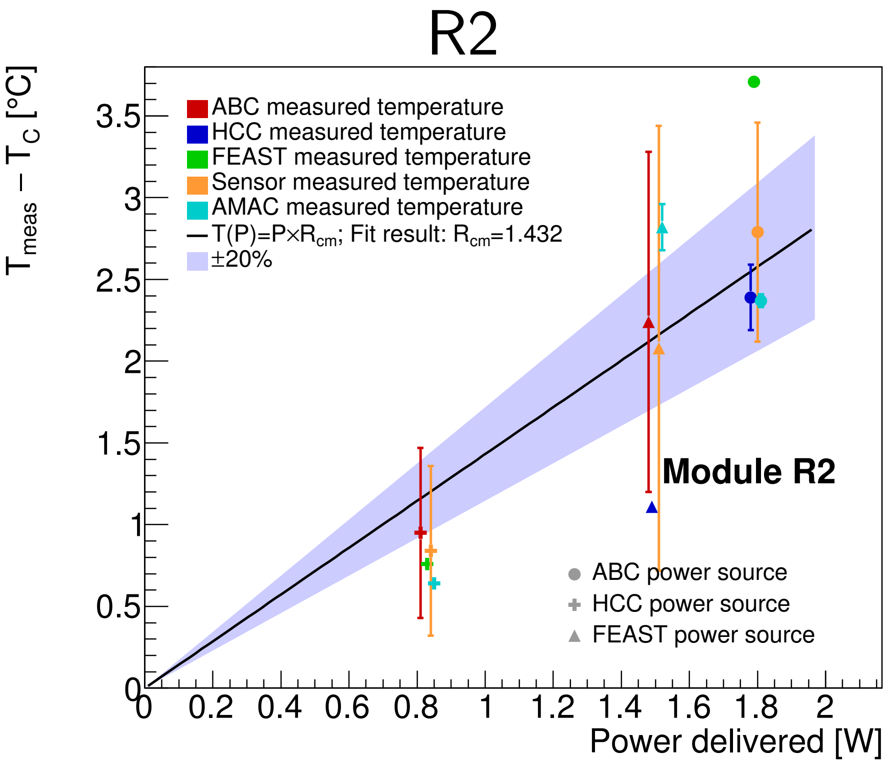
FEAST efficiency

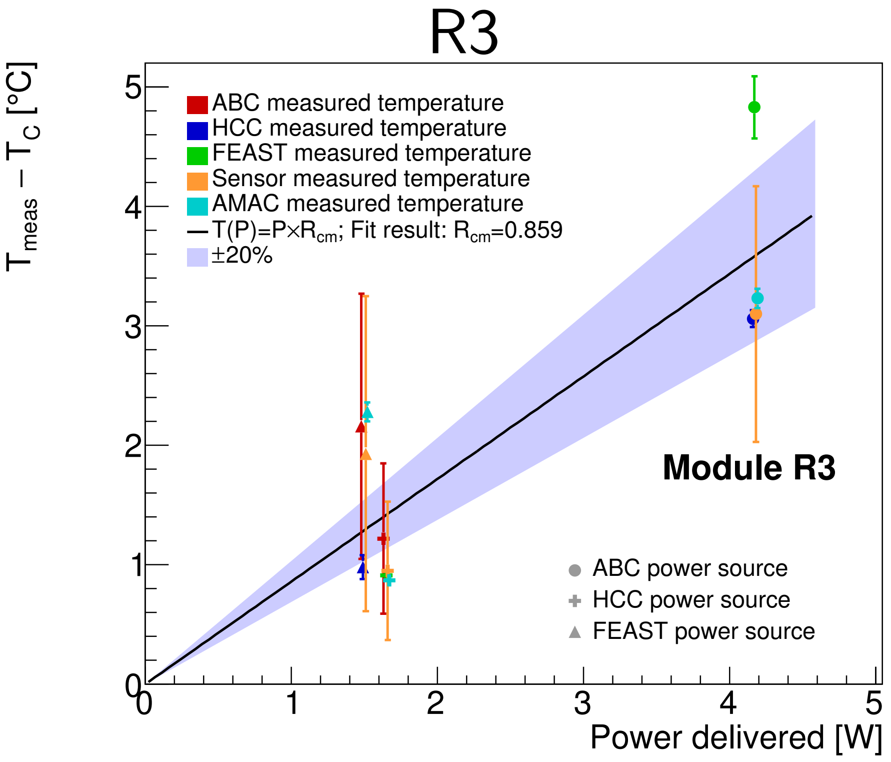


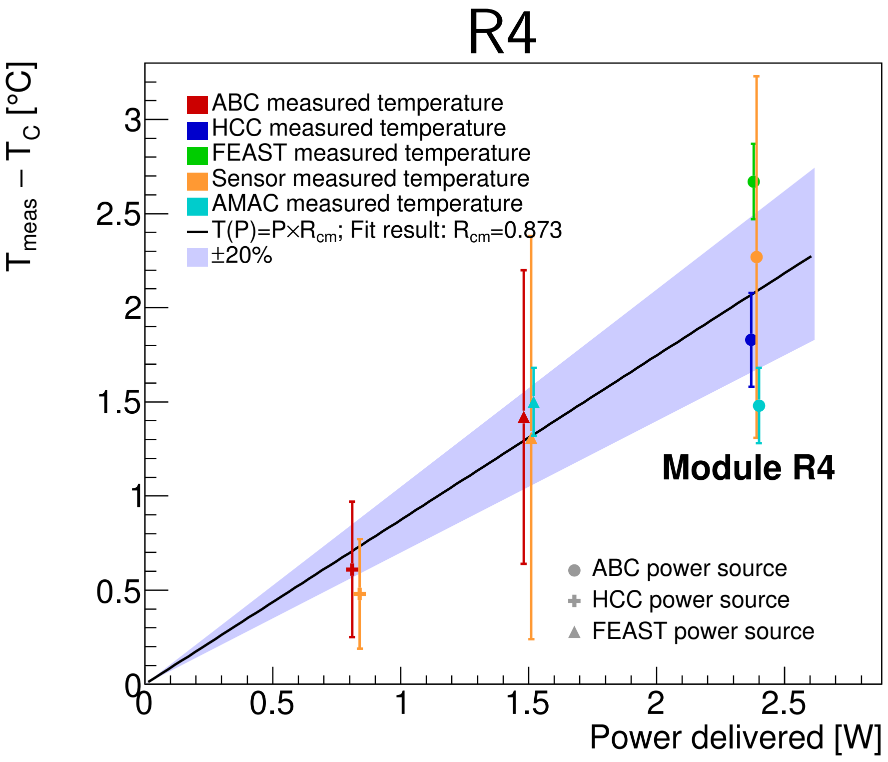
First Endcap R_{cm} Results

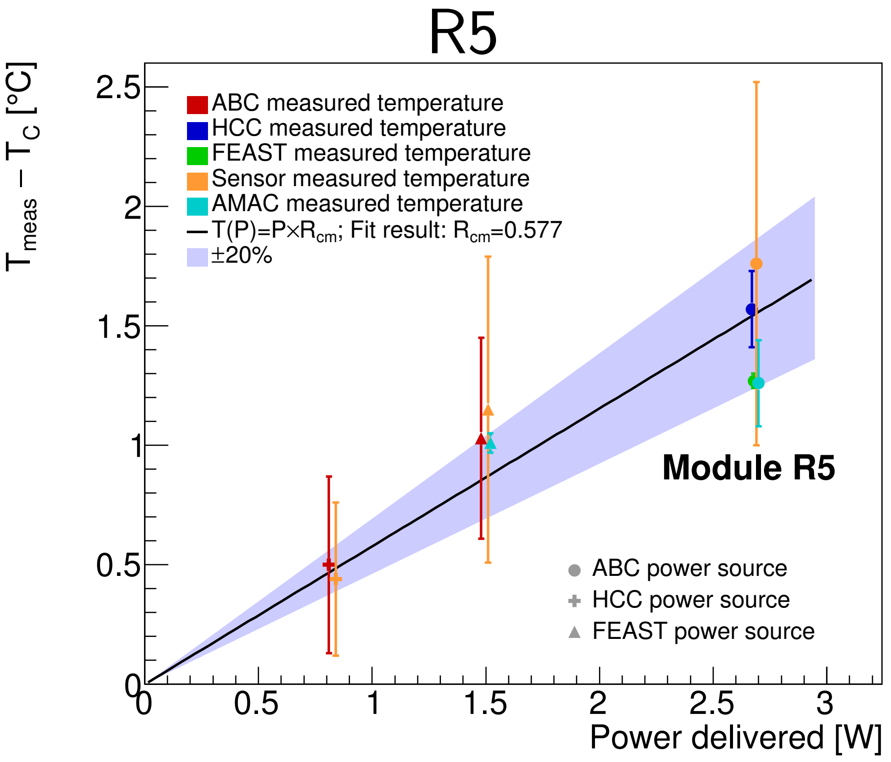

R0


R1

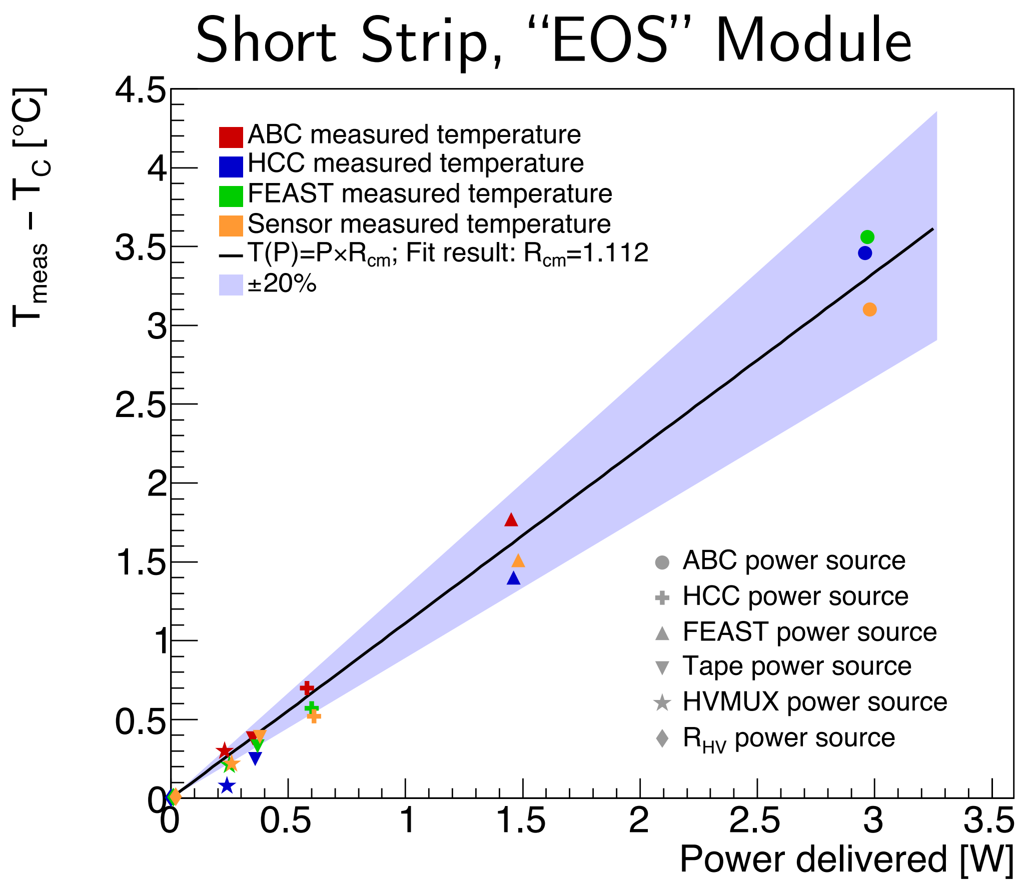

R2

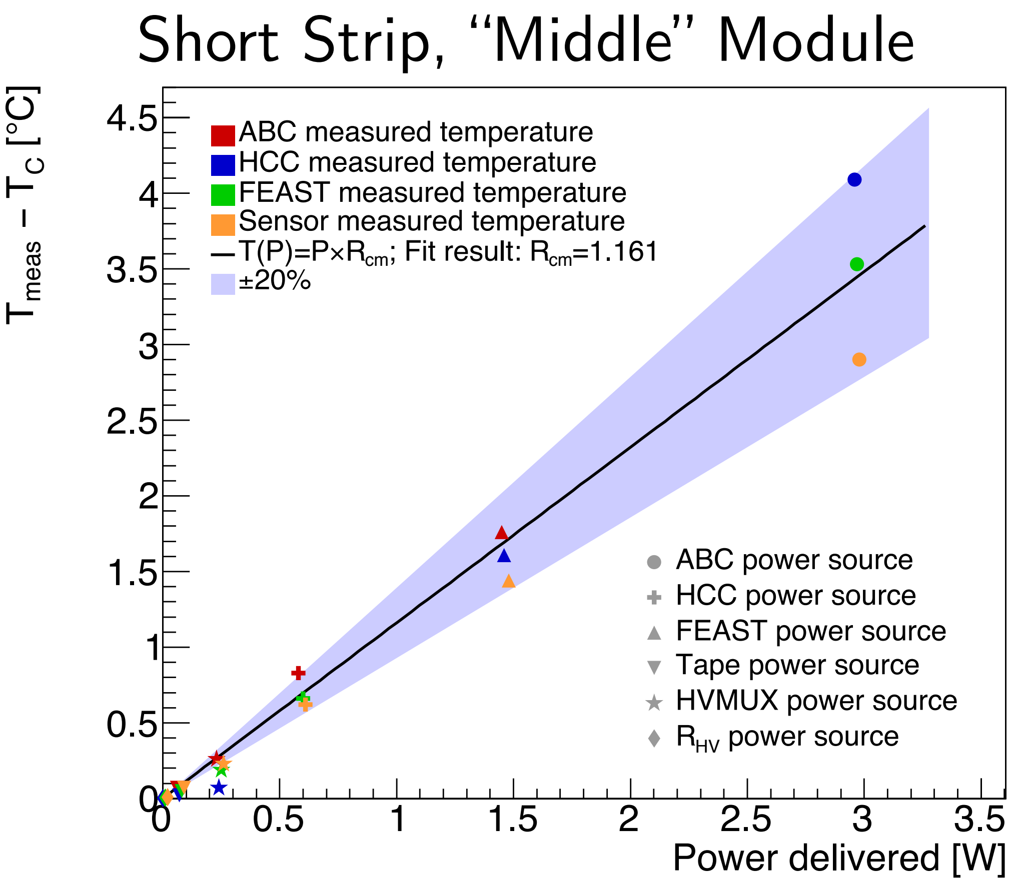

R3


R4


R5

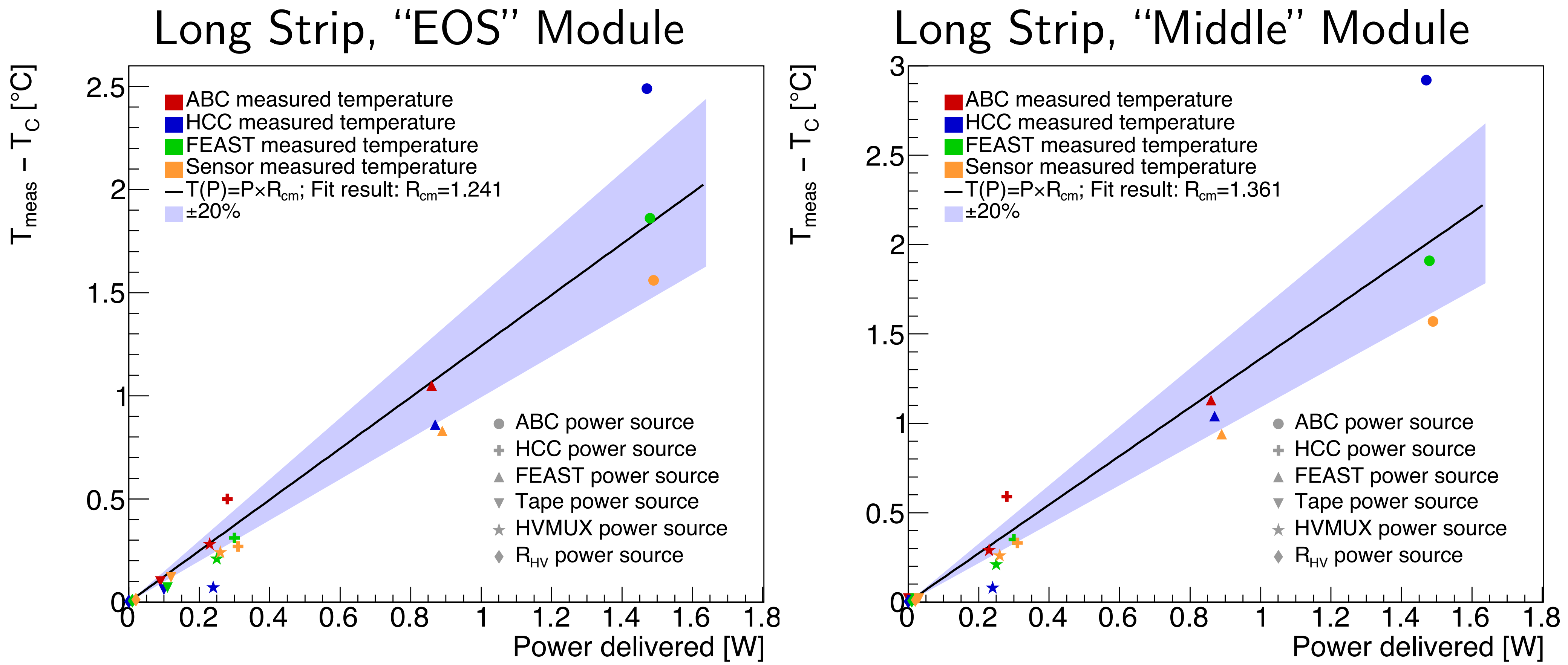
Fitting for R_{cm}: Barrel Results (Short Strip)


Short Strip, “EOS” Module


Short Strip, “Middle” Module

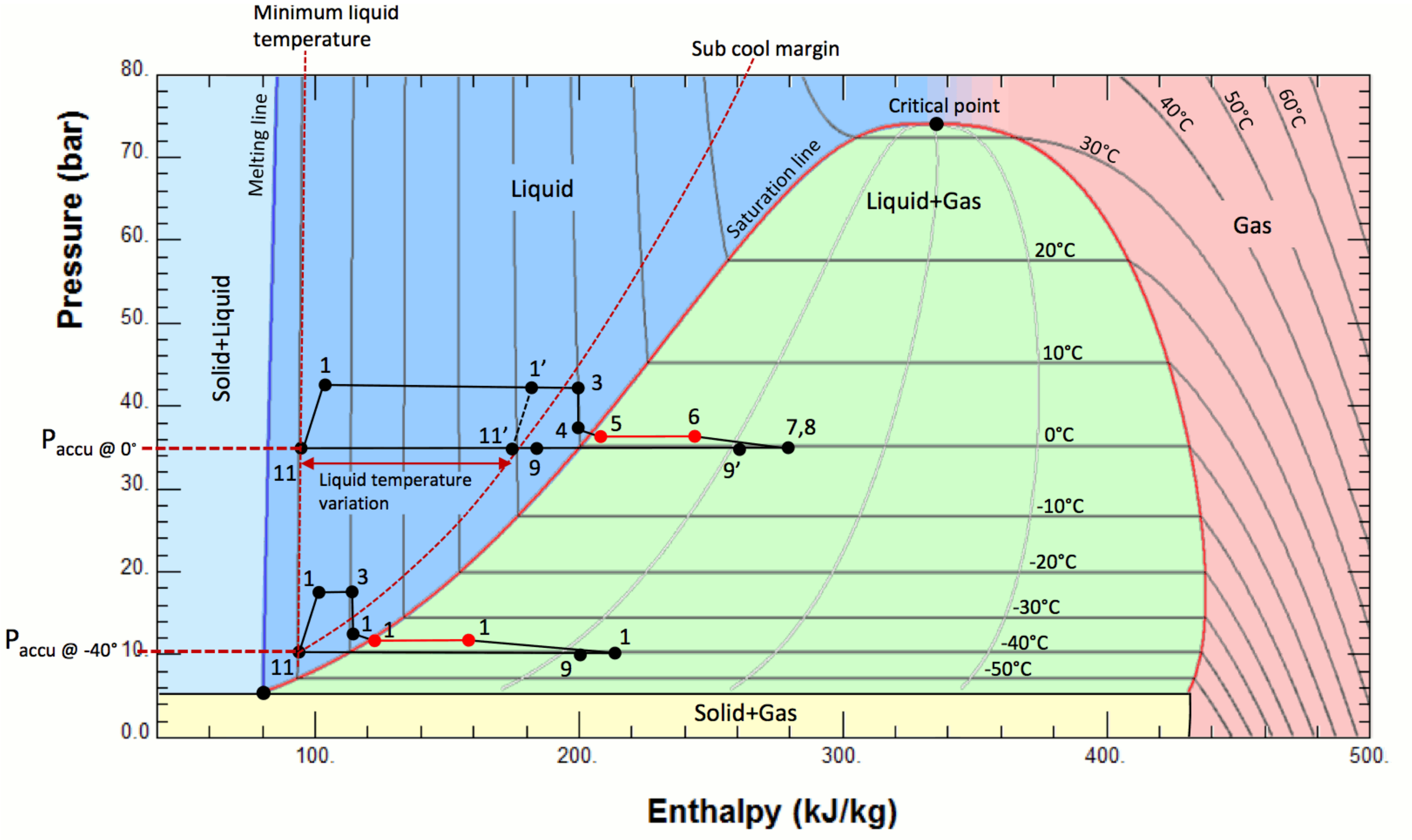
- Barrel also checks Tape, HVMUX, and R_{HV} power sources
- R_{CM} is relatively linear in these cases; 10% safety factors are used for the Barrel

Fitting for R_{cm}: Barrel Results (Long Strip)



- Same story – fit is decent.

CO_2 Cooling



- CO_2 cooling loop (2PACL system)

Cooling Scenarios - Backup