WG6: High Speed Links

CERN EP Department

R&D on experimental technologies – 1st Workshop

F. Vasey and P. Moreira (Convenors)

2018 / 03 / 16

WG6: High Speed Links

Mandate

- "Definition of the R&D needs in the field of High Data Rate Electrical and Optical Links for detector systems"

Convenors

- Francois Vasey and Paulo Moreira

Members

- 33 "Subscribers"

Activities

- Pre-meeting (9 February 2018)
  - Restricted to "selected" EP specialists:
    - Sophie Baron, Carmelo Scarcella, Szymon Kulis, Jan Troska
  - Explored *State of the Art*
  - Extrapolation to the 2020 – 2025 horizon
- 1st Meeting (5 Mar 2018)
  - Open to the HEP community
  - 26 participants (9 meeting room + 17 Vidyo)
  - Report on the pre-meeting
  - Community state of the art and future research
- 1st Workshop (today's meeting)
  - Synthesis of the 1st meeting
  - Challenges

Reports at this Workshop

- Szymon Kulis:
  - **High Speed Link Technologies state of the art and extrapolation to 2025**
- Paulo Moreira:
  - **Map of the Community and Development Activities, Challenges beyond HL – LHC**

High Speed Link Technologies

state of the art and extrapolation to 2025

Electronics: S. Baron, S. Kulis, P. Moreira

Opto: C. Scarcella, J. Troska, F. Vasey

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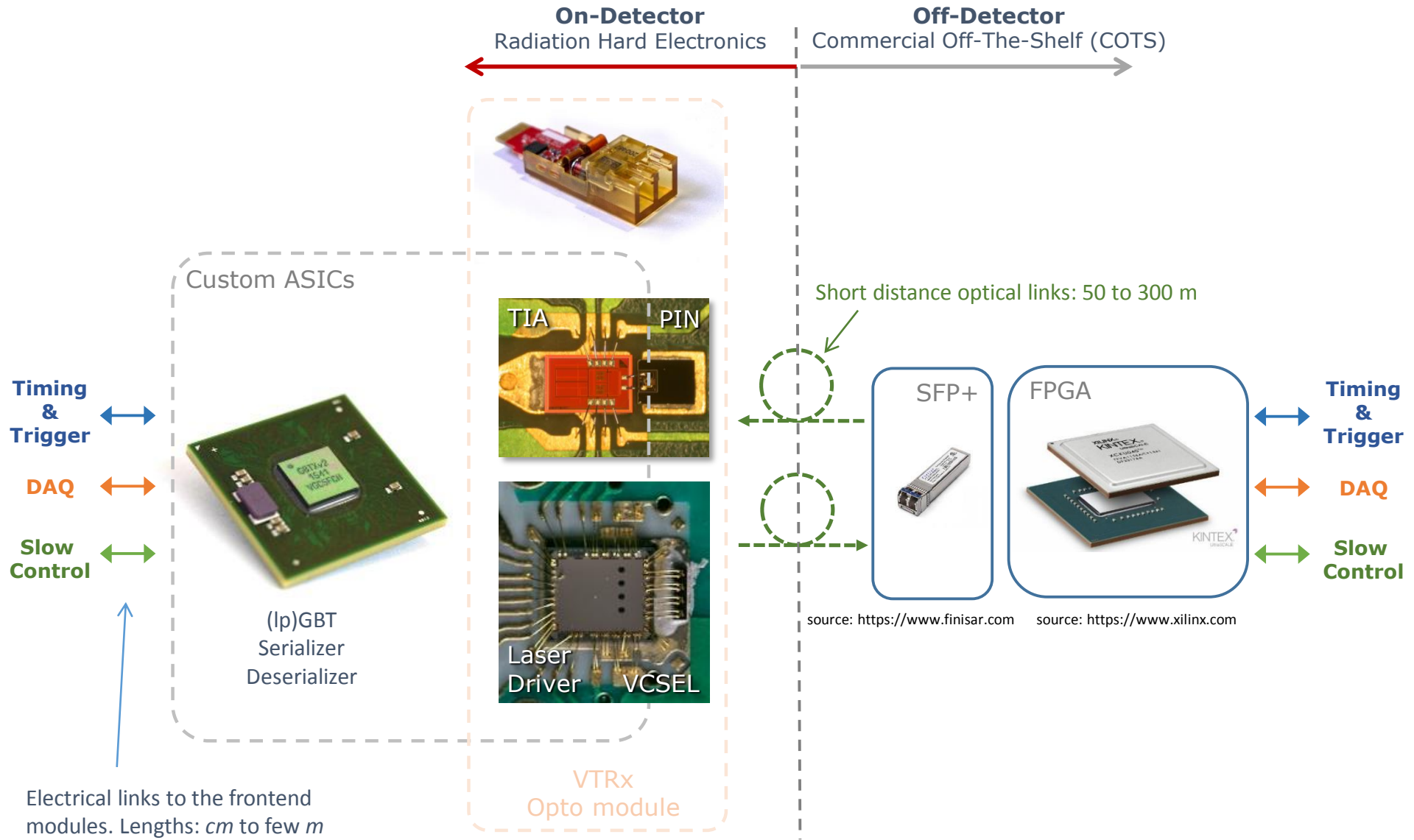
R&D on experimental technologies – 1st Workshop
16/03/2018 Geneva

High Speed Links in HEP



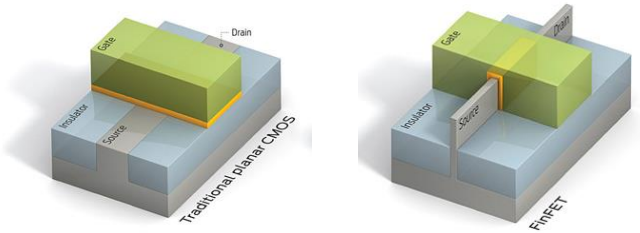
Foreword

- **Development of Links** is highly dependent on:
  - **Machine** being considered
    - Radiation environment
      - HL – LHC: > 100 Mrad
      - CLIC: < 1 Mrad
      - FCC: > 1Grad
    - Timing requirements (beam structure)
  - Type of **detector** (e.g. Pixel-Detectors, Trackers or Calorimeters)
    - Data rates / aggregation
    - Distances
    - Power consumption
- R&D program (2020 – 2025) it is likely to target the upgrade of HL-LHC ("LS4") which can then pave the way to more distant projects (ILC/CLIC, FCC, ...)
  - Link developments are thus likely **to target high data rates** applications, and in some cases **extremely radiation hard environments**!

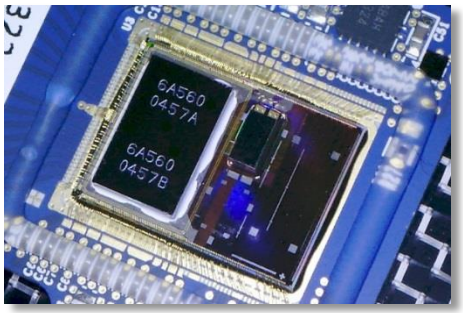
Radiation Hardness

- **Radiation hardness is** and will be the **major technical challenge**:
  - High-Speed (≥ 10 Gb/s) Circuits developed in the CMOS technologies currently being used by the HEP community will not survive TID doses higher than 100 / 200 Mrad
  - Experience in qualifying active optoelectronic components points to the exclusion of opto-devices for radiation environments exceeding 3×10^{15} n/cm^2

- Possible escapes are:
  - Explore **new commercial IC technologies**:
    - Large qualification work that has to be done wide across the HEP community *(Synergy with the IC Technologies Working Group is needed to identify possible solutions)*
  - Explore **new optoelectronic devices**:
    - e.g. optical modulators with external and remote laser source
  - Explore **electrical links** for extreme radiation environments:
    - Large bandwidths in low mass cables might be difficult to achieve.



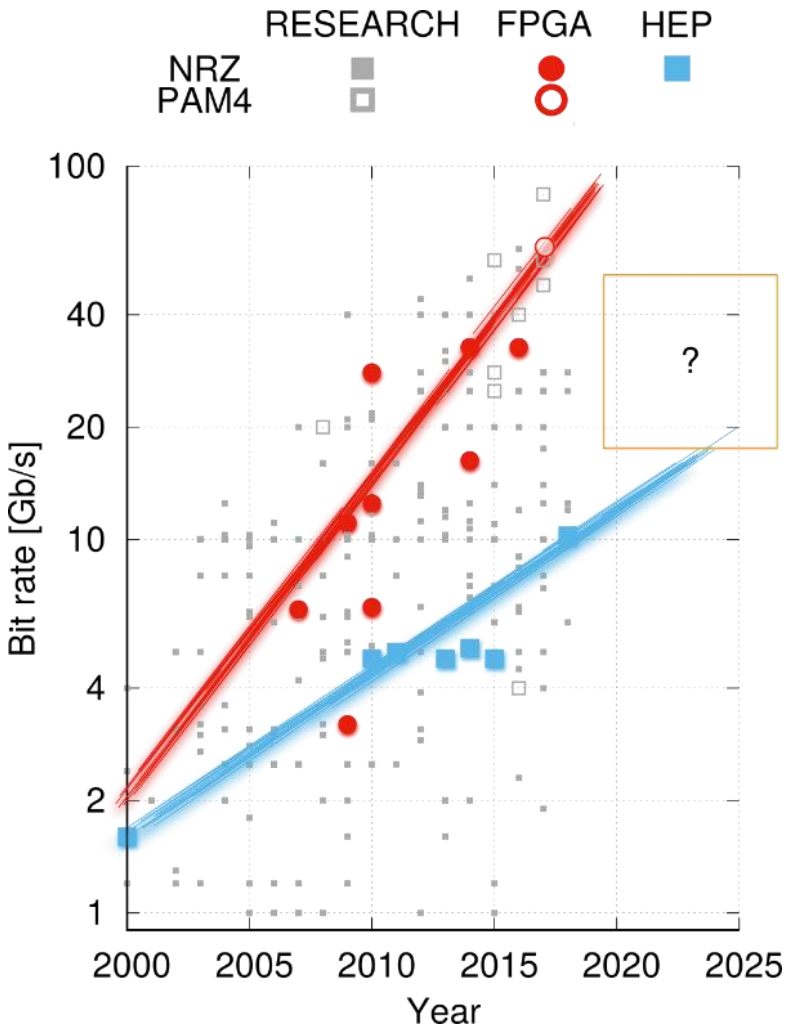
Source: https://spectrum.ieee.org



Source: http://www.luxtera.com

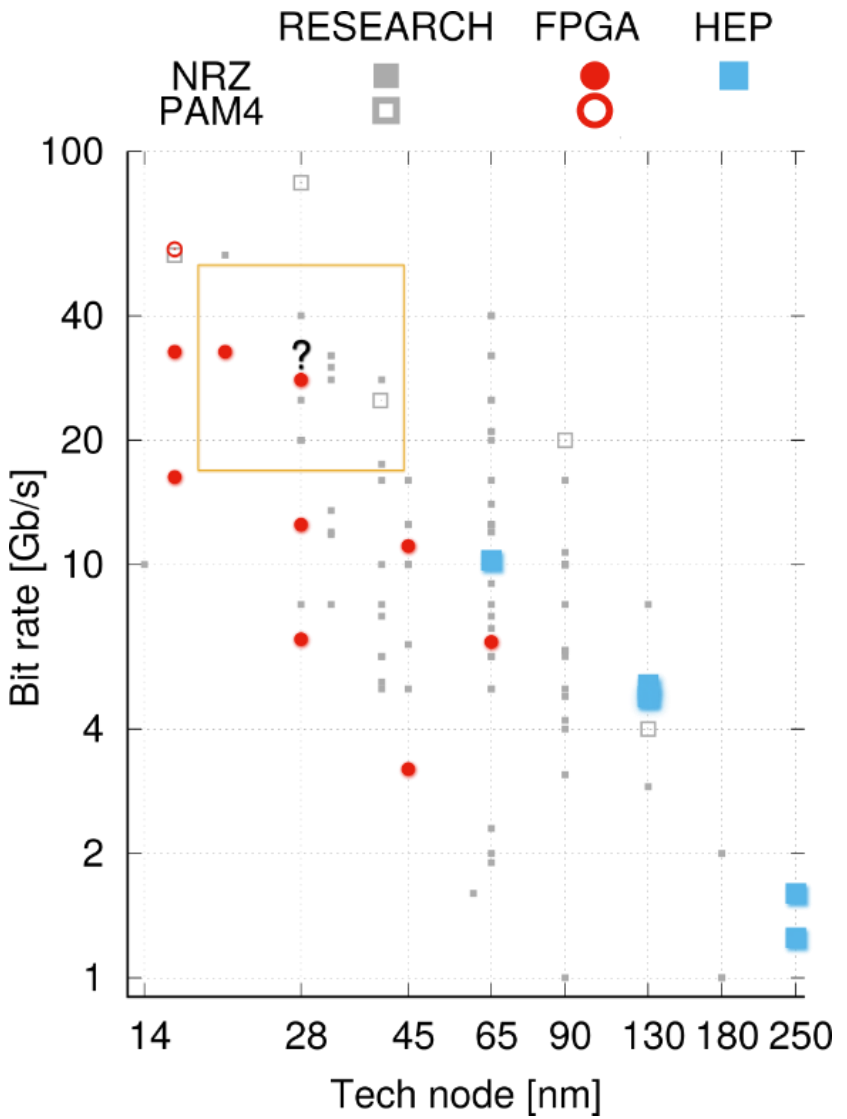
ASICs Technology : Serializer line rate trend

- **HEP systems are certainly lagging** behind research papers (for which the main aim is to demonstrate peak performance) and commercial systems (FPGAs)
- HEP ASIC **performance** tends to be **limited by**:
  - Long development cycles: **radiation qualification and reduced resources**
  - Use of relatively old technology nodes: **radiation qualification and prototyping cost**
  - Circuit techniques: **increasing radiation tolerance** to TID and SEU
- If a projection can be made in the horizon of 2020 to 2025 the HEP systems **should be targeting 20 - 40 Gb/s systems**:
  - Well within the capability of today's FPGAs



ASICs Technology : Technology nodes

- **Data rates are highly correlated with the technology nodes**
- **Shift in modulation format** (not technology) can be seen **for highest data rates** (NRZ -> PAM4)
- Research papers demonstrate 40 Gb/s NRZ to be possible for technology nodes ≤ 65 nm
- Commercial systems (FPGAs) introduced 30Gb/s + data rates for the 28 nm node and below



ASICs Technology : Overview

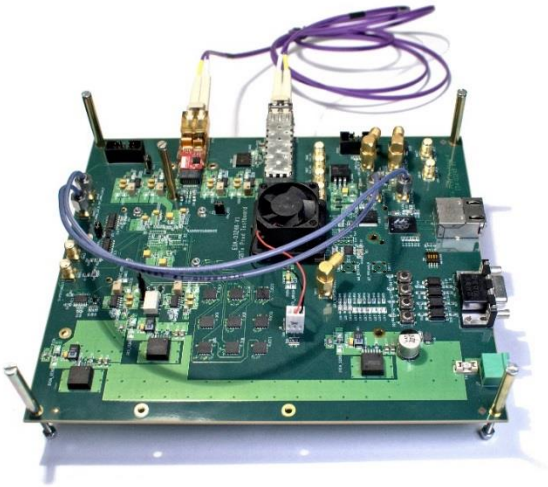
- The **technology scale trend is favorable to design high data rate circuits**
  It is however not clear that the technology scaling will yield (naturally) radiation hard ASICs
- Technology goes in the direction of using **lower supply voltages** that results in **better power efficiency** (advantageous for HEP applications)

- However lower supply voltages reduce the ability to:
  - Drive laser diodes or VCSELs (need 2.5V)
  - Drive Modulators (need 2V or above)
  - Bias PIN-diodes (need 2V or above)

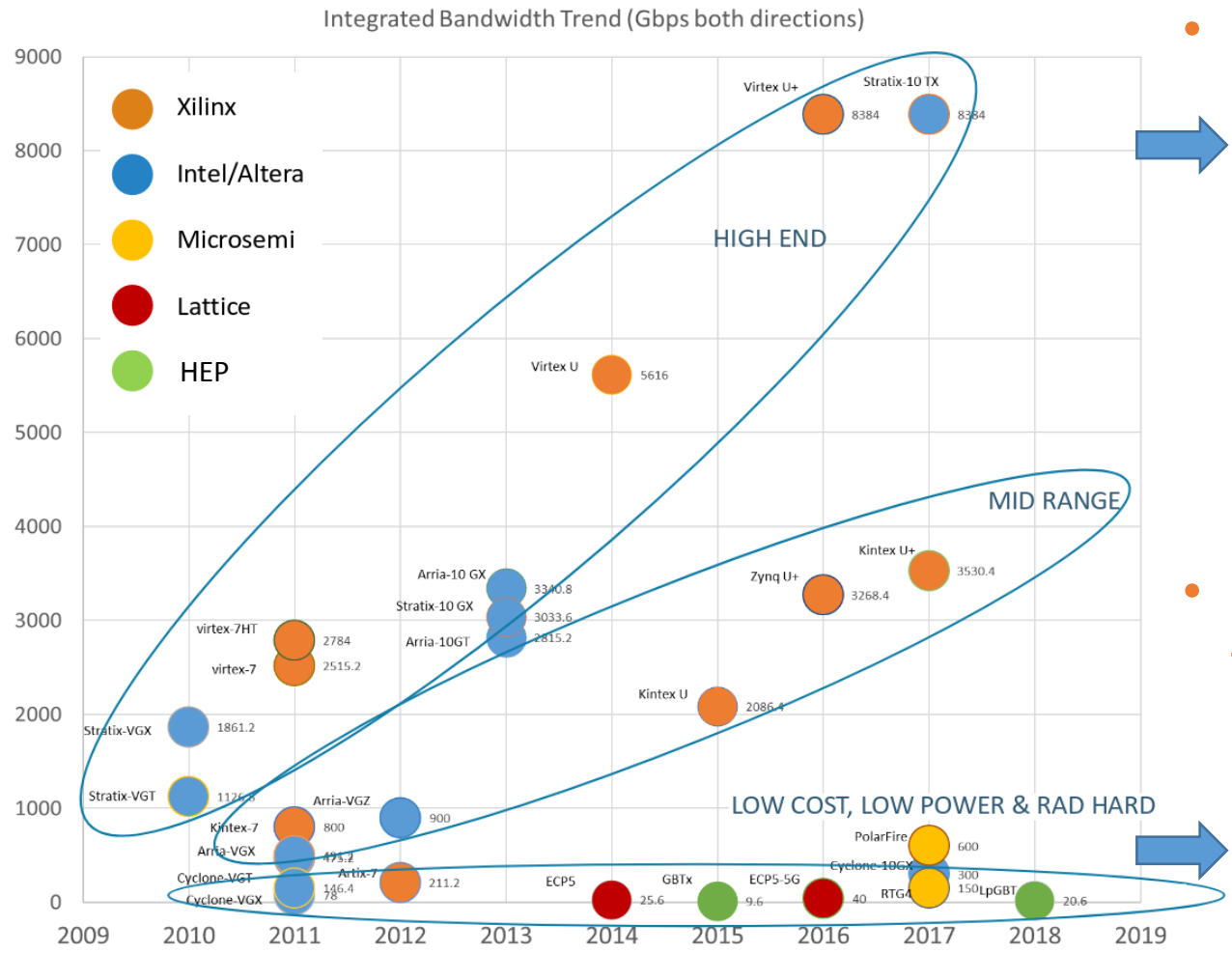
- The **choice** of which **technology** to use must thus be driven by:
  - The **radiation field** of the environment
  - The **data rates** to be achieved
  - The **type of optoelectronic device** to interface with

FPGA Technology : Introduction

- **HEP synergy with FPGAs** (counting room systems)
  - Last 2 generations of LHC projects used FPGAs in backend systems
  - Minimize the effort to develop test systems for the Links and ASICs
- HEP requirements for FPGA transceivers (so far so good)
  - Bypassing commercial protocols
  - Optimizing equalization
  - Controlling the latency of data & clocks (deterministic latency in CPRI protocol)
- **Links/ASIC developments should thus stay in track and maintain compatibility with the FPGA developments as much as possible.**

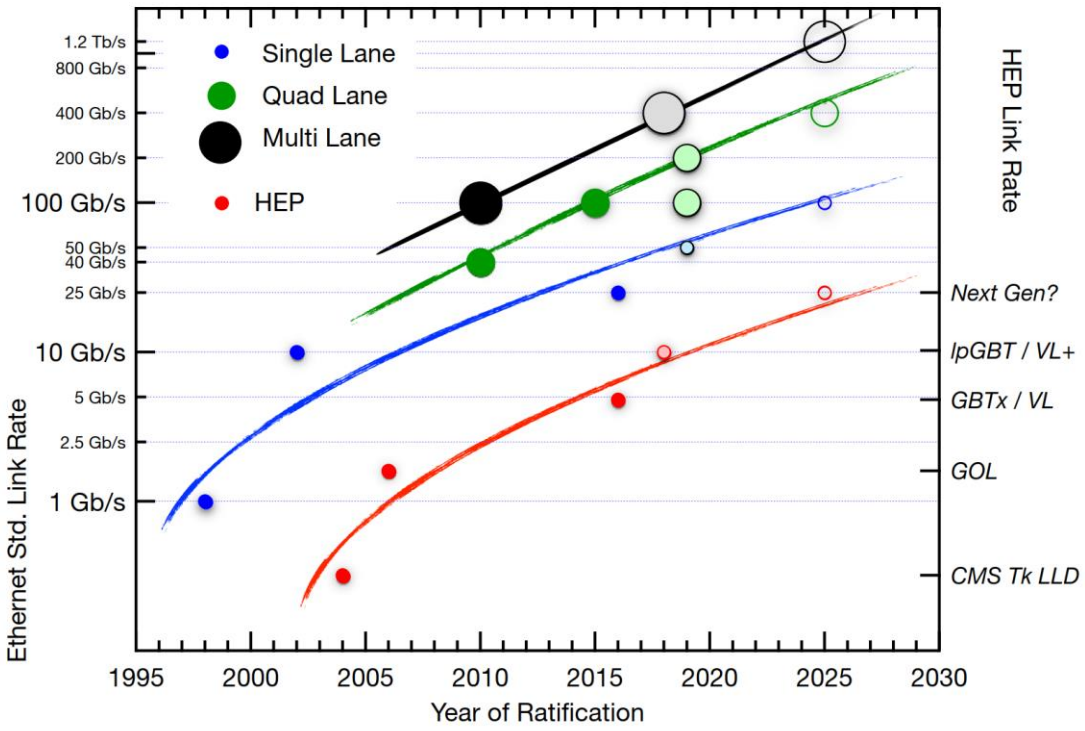


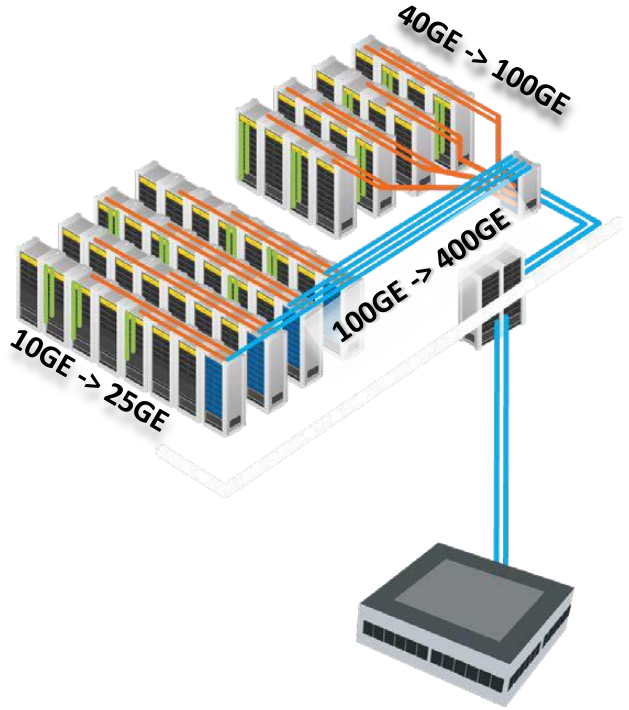
FPGA Technology : Trends



- Data centers, networking platforms:
  - Terabit interfaces
  - 56/58 Gbps PAM-4
  - Highest processing power & efficiency
  - Highest flexibility
- Internet of Things(IoT), 5G wireless:
  - Lower bandwidth (links speed to ~10Gbps)
  - Lower processing power
  - Low cost
  - Small form factor

Optoelectronics Technology : Trends





source: https://www.finisar.com

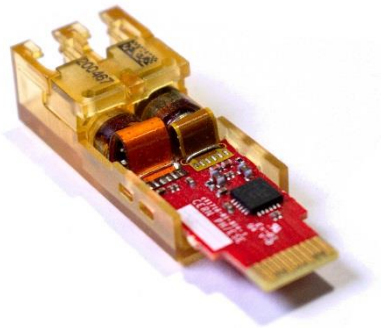
- Per-lane rates:
  - 10G NRZ, 25G NRZ, 50G PAM4 (25GBaud)
- Multi lanes to increase system bandwidth (×2, ×4, ×8, ×16)
- Distances > 500m are Single Mode

Data Center connections are moving:

- Within the Data Center Rack
  from 10GE to 25GE
- Between Data Center Racks
  from 40GE to 100GE
- Inter-Data Centers & WAN
  from 100GE to 400GE
  (being standardized now)

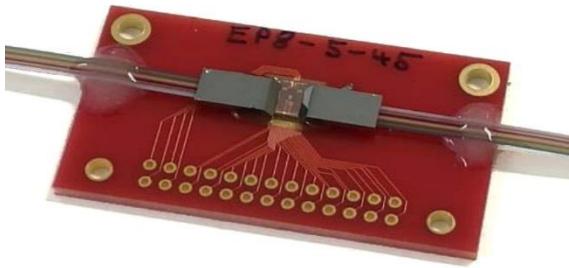
Optoelectronics Technology : Trends

- Radiation resistance is not changing with new generations of opto electronic components (in our observations)
- Commercial high speed driver ASICs are usually SiGe-BiCMOS based (not CMOS)
- Data rates in HEP have historically been limited by the serializer (Rad-hard GOL or GBTx)
- Time-division multiplexing hits a limit around 25-50Gbps (VCSELs)
  - Higher bit-rates achieved through
    - Wavelength multiplexing
    - Multi-level signaling (PAM-4 and others)
- Both Single Mode and Multi Mode links have been developed in HEP
  - SM/MM battle ongoing in datacenter applications. SM will be the ultimate winner, but at which crossover point?

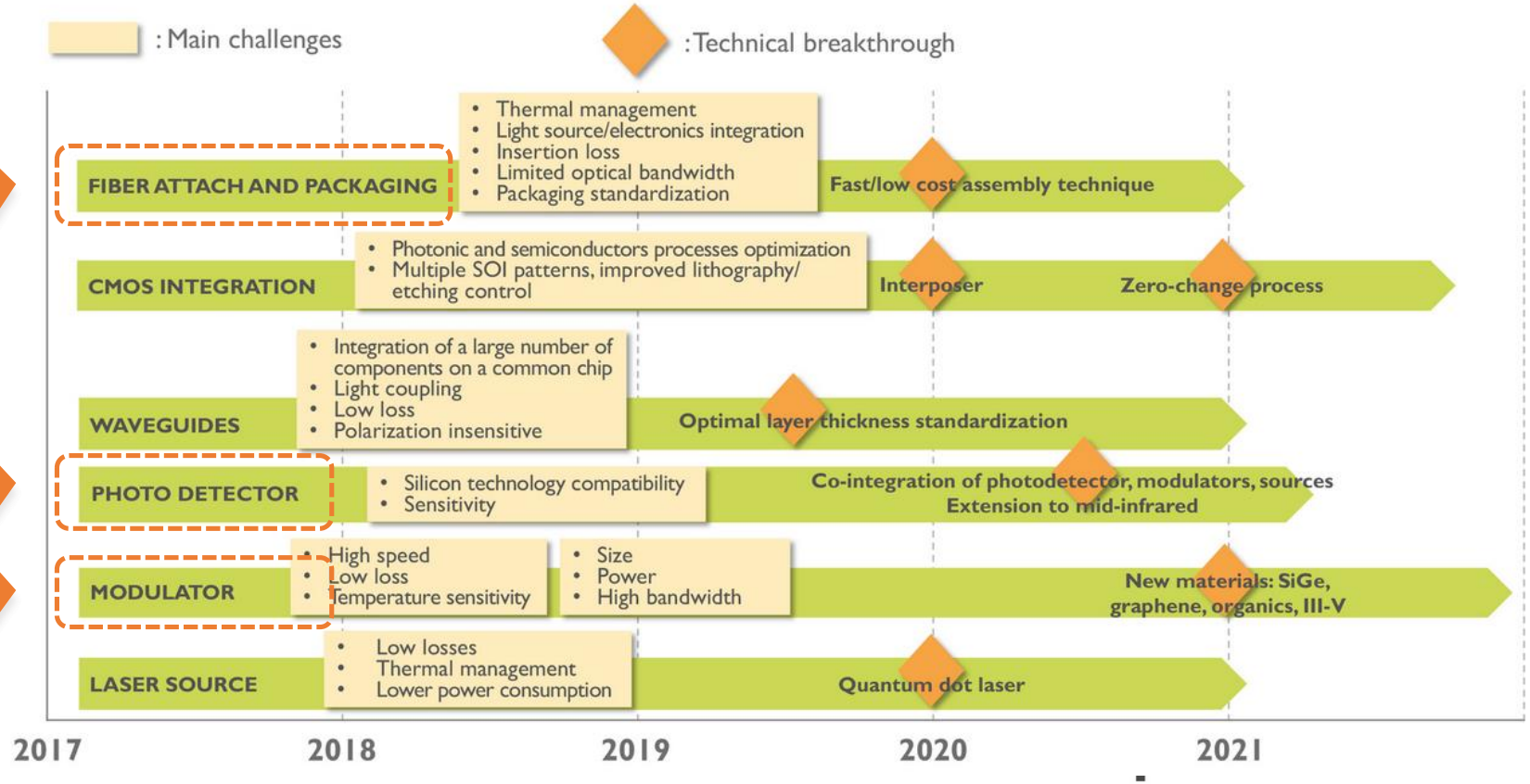


Silicon Photonics Technology : Introduction

- What is Silicon Photonics?
  - A photonic system using **silicon as an optical medium**
  - The silicon waveguide lies on top of a silica cladding layer (SOI)
  - Silicon is patterned with sub-micron precision into planar micro-photonic components
- So, why is Si-Photonics of interest to HEP?
  - Radiation resistance potentially as good as Si-sensors and CMOS electronics
  - Possibility to design custom circuits in MPW framework
  - Possible Co-integration with sensor and electronics
- Silicon photonics radiation resistance
  - **Not sensitive to displacement damage** :
    - Almost no degradation up to 5×10^{16} n/cm^2
  - **Sensitive to TID** :
    - Devices stay operational to ~200 Mrad



Silicon Photonics Technology : Roadmap

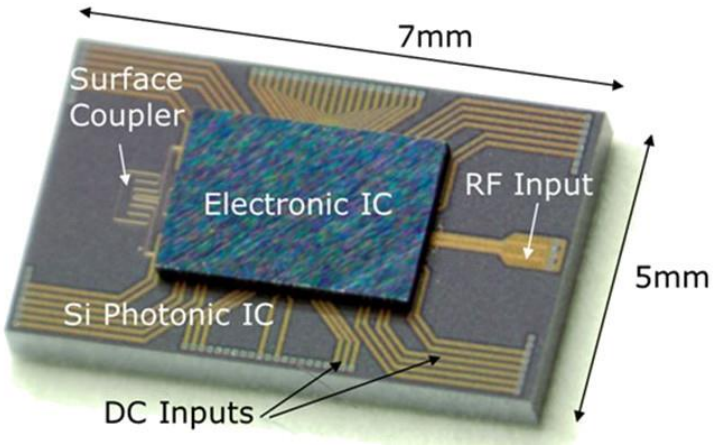


(Source: Silicon Photonics 2018 report, Yole Développement, January 2018)

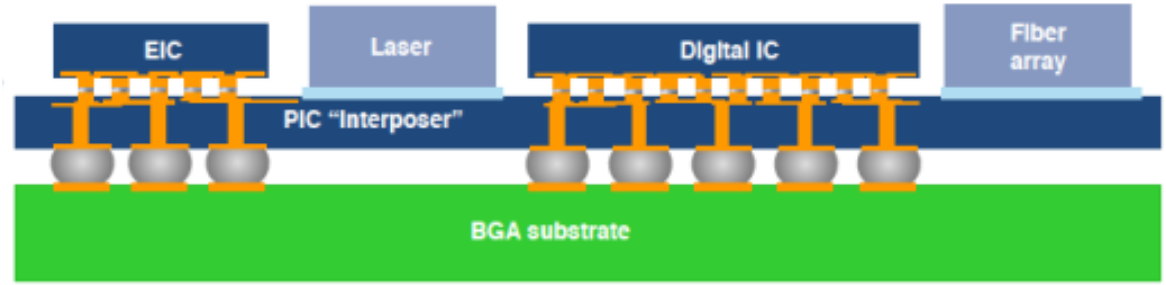
Developments ongoing at CERN

Silicon Photonics Technology : Packaging

- Nowadays the photonic IC size is generally larger than the electronic IC size
  - Free carrier dispersion modulators are relatively large devices > 1 mm
  - Fiber attachment has a large footprint onto the photonic chip
- Area on electronic IC is in general more expensive than on photonic IC
  - Hybrid integration is currently preferred to monolithic integration of electronics and photonics devices
- Through Substrate Via (TSV) to replace wire bonding and minimize parasitic?
  (Synergy with the Silicon detectors Working Group)



Source: "Silicon Photonics and FDMA PON: Insights from the EU FP7 FABULOUS Project" S. Abrate et all.

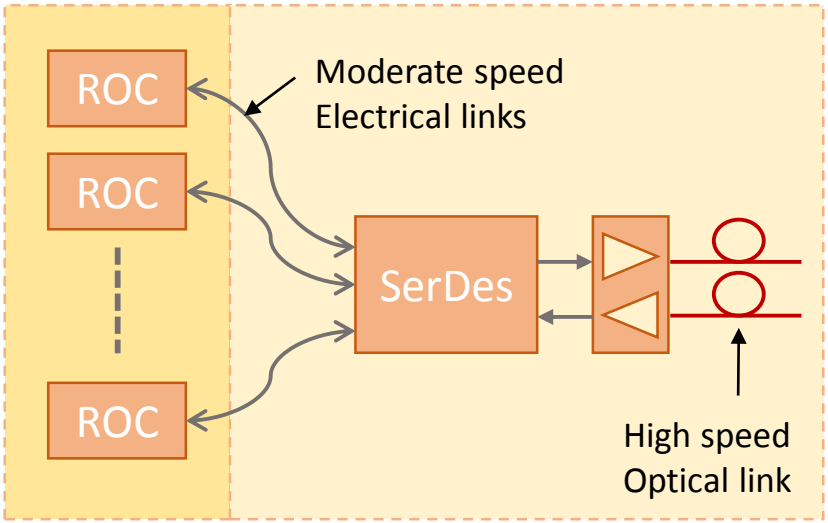


EIC & DIGITAL IC assembled with μ-Copper pillars an active PIC "Interposer"

Source: https://www.3dincites.com/2014/01/lessons-learned-trenches-3d-ic-manufacturing-sensor-applications/

Other Issues

- Systems implemented so far in HEP have rather distributed data sources
  - Moving to higher data rates usually means solving an aggregation challenge
  - Not clear that super high capacity is what is needed at the data source
  - Architecture and topology challenge? Need for copper fan-in network?



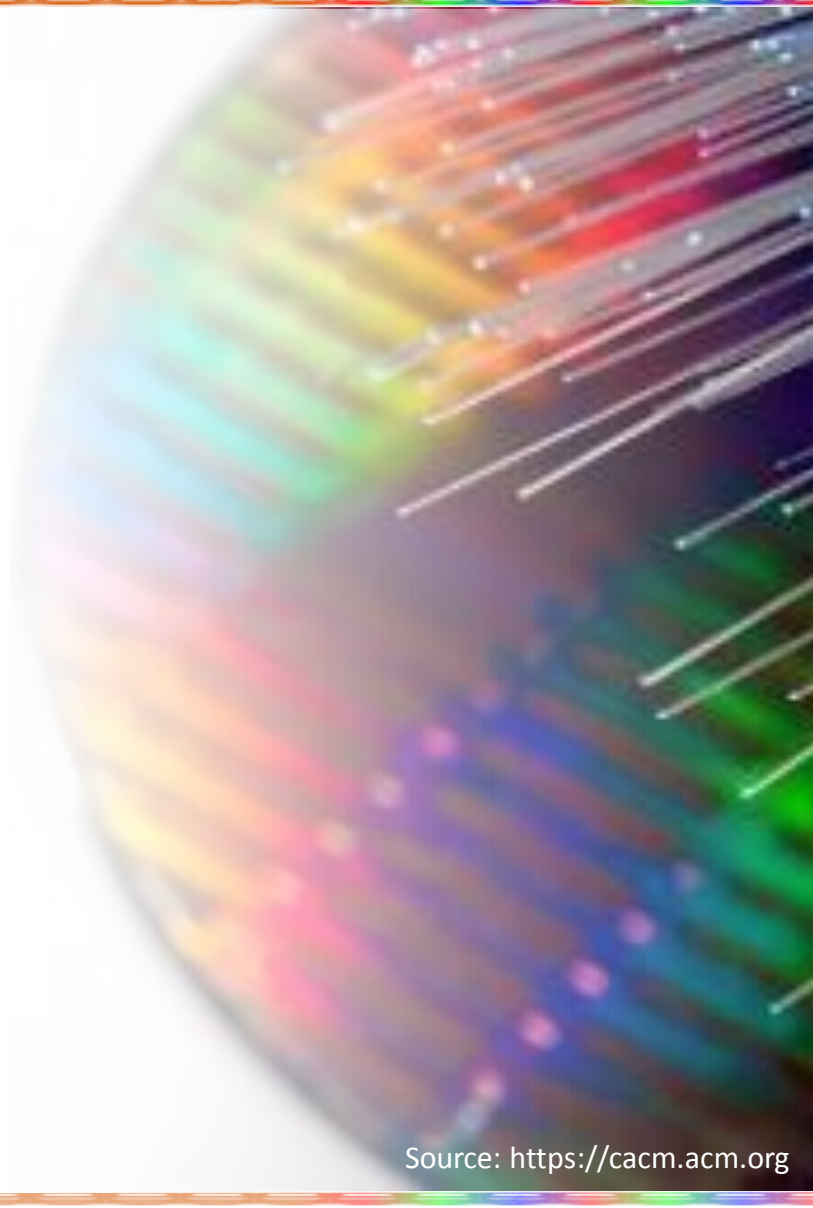
- Data rates are becoming asymmetric with the LpGBT system (10Gbps / 2.5Gbps)
  - A heresy in the commercial world
- Link systems become more power efficient (energy required to transmit a bit of information goes down). However, due to increase in the data rate, the power consumption of the link has tendency to stay constant.
- Link cost is a salient issue
  - Link cost is always part of the development equation for large systems
  - The benefit of fewer faster links must be compared to cheaper/slower links?

ASIC Development : Main Challenges

- **Very high radiation levels (TID) > 100 Mrad**
  - Explore **new down scaled commercial IC technologies**
  - High bandwidth electrical links over low mass cables might be a necessity so research on such a systems is also very much needed
- **Low supply voltages** and low breakdown voltages make difficult to drive optoelectronic components efficiently
  - **Alternative technologies** and architectures need research
- **Synergy with FPGAs** is crucial

Opto Development : Main Challenges

- **Very high radiation levels NIEL > 3×10^{15} n/cm ^{2}**
  - Relocate actives? Qualify Si-Photonics?
- Capped distance x bandwidth product
  - Above 10Gbps, identify rad-hard high-bandwidth MM fiber? SM?
- **Line-rates follow GbE standards in discrete steps**
  - After 10Gbps comes 25Gbps
  - FPGA IP to become narrowband as data rates increase
    - GBT++ rate = 25Gbps
    - PAM4 starts at 25GBaud
- **Multiplexing** allows to increase capacity without changing bitrate
  - Multi-level signaling (PAM4 in FPGA at 25GBaud and above)
  - Wavelength multiplexing (could ease the aggregation challenge)
- **Packaging** remains a **massive challenge** (try to benefit from COTS solutions)
  - Hybrid integration with electronics and sensors
  - Pigtailing



Source: https://cacm.acm.org

Map of the Community and Development Activities, Challenges beyond HL-LHC

CERN EP Department

R&D on experimental technologies – 1st Workshop

P. Moreira and F. Vasey

2018 / 03 / 16

Outline

- WG6 Contributors and Themes
- HEP Links
- Overview of the community activities and technology challenges
  - Summary of the 1st meeting (5th March):
    - Optoelectronics
    - ASICs
    - Optical “wireless”
    - RF
    - Si-Photonics
- “Development space” - CERN’s perspective
- Summary

Contributors and Themes

	CERN	INFN – Pisa*	KIT	SMU – EE	SMU – PH	WADAPT**
ASICs	✓	✓		✓	✓	✓
Electrical links	✓				✓	
FPGA systems	✓					
Optoelectronics	✓	✓			✓	
Free-space optics		✓				
RF						✓
Si-Photonics	✓	✓	✓	✓		

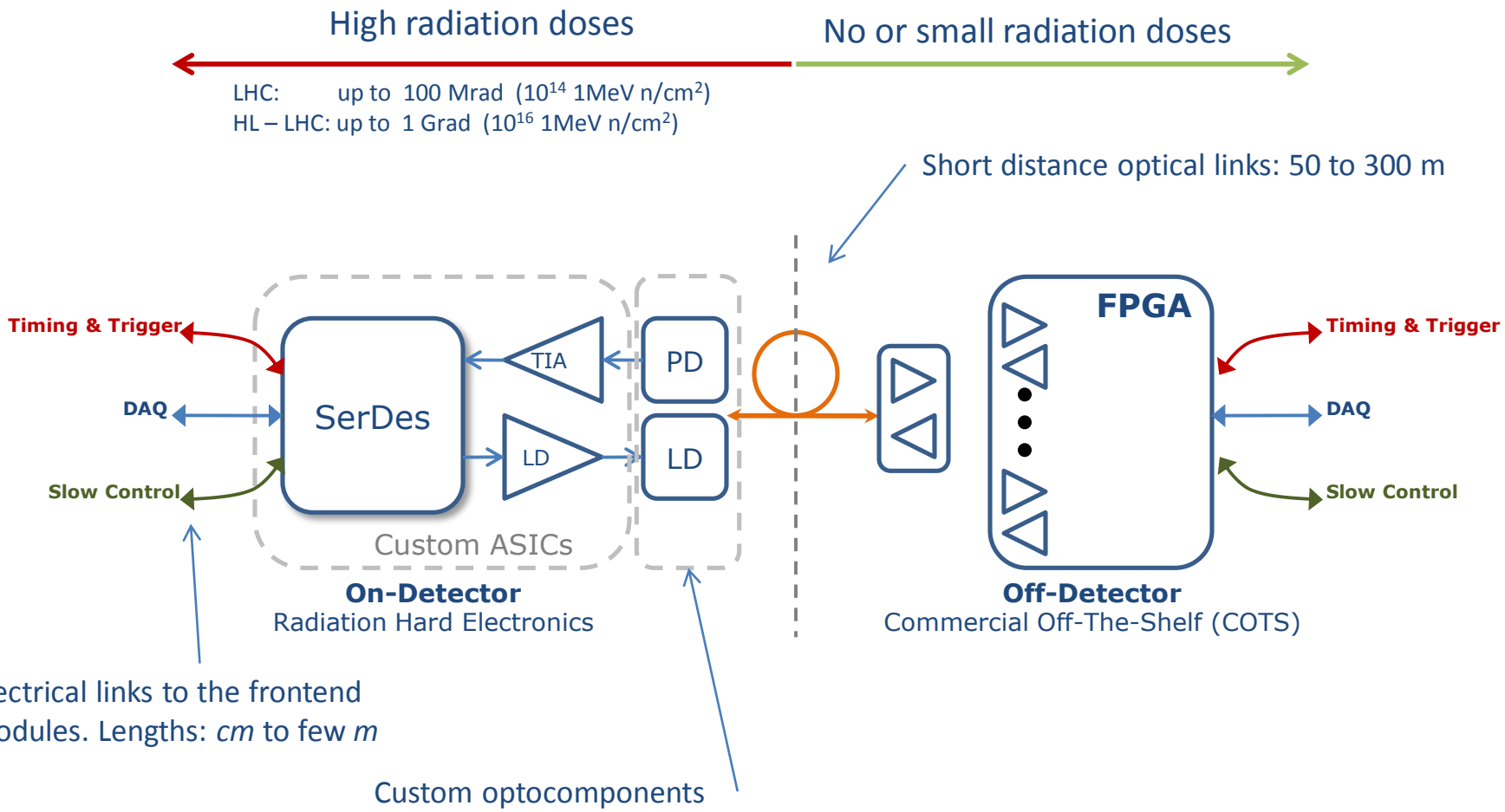
For details and credits please see the material presented in the "WG6-HighSpeedLinks first-meeting":
https://indico.cern.ch/event/706078/

Speakers:

CERN: Francois Vasey
INFN – Pisa: Fabrizio Palla
KIT: Marc Schneider
SMU – EE: Ping Gui
SMU – PH: Jingbo Ye
WADAPT: Pedro Rodriguez Vasquez

* **INFN – Pisa**: Scuola Superiore S. Anna & University of Pisa Engineering Department;
** **WADAPT consortium**: Argonne National Laboratory, Bergen University, CEA/LETI/DRT/DACLE/LAIR, CEA/DRF/IRFU/DPhP&Paris-Saclay University Gangneung-Wonju University, Heidelberg University, Uppsala University, Wuppertal University

Today's typical HEP Link Architecture



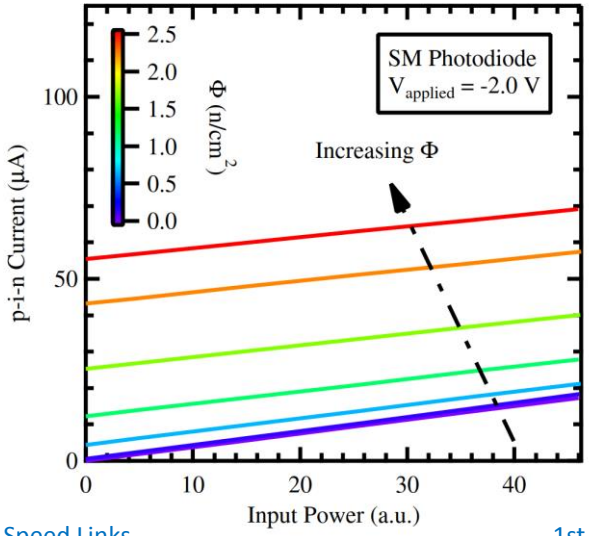
Optoelectronics

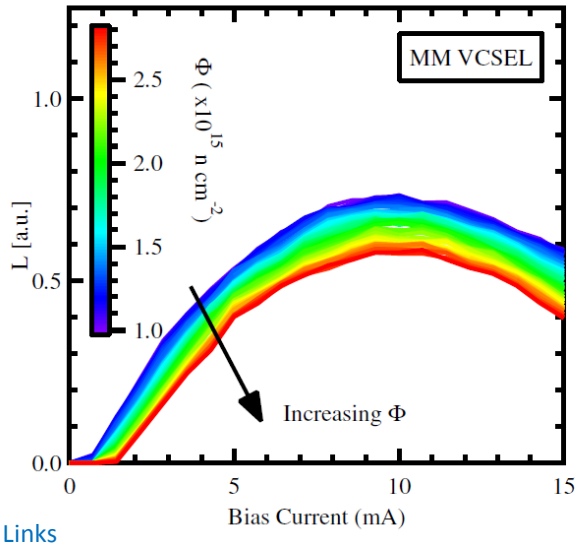
- **Radiation Damage in Optoelectronics**
  - Damage mechanism dominated by Displacement Damage (DD) caused by Non-Ionizing Energy Loss (**NIEL**) from heavy particles (neutral/charged hadrons, energetic leptons).
  - **"Radiation Tolerance Limit" for VCSELs and PINs: "a few" x10^{15} n/cm2**

- **PIN - Diodes:**
  - Reduction of the responsivity
  - Increasing of the dark current (pA to mA)

- **VCSELs:**
  - Increase of threshold voltage/current
  - Decrease of the laser slope-efficiency
  - VCSELs display higher radiation tolerance than EE diodes

- **Challenges:**
  - PIN needs "high" bias voltages to maintain low capacitance [end of life conditions]
  - VCSELs need high forward voltages





VL+ team:
CERN
Oxford
SMU
FNAL

ASICs

- The community has a large experience in the development of rad-hard communications ASICs
  - PLL & CDR: 4.8 / 5.12 GHz (65 / 130 nm CMOS)
  - Serializers/DeSerializers: 2.56 / 4.8 / 5.12 & 10.24 Gbps (65 / 130 nm CMOS)
  - Laser / VCSEL Drivers: 4.8 / 10.24 & 14 Gbps (65 / 130 nm CMOS)
  - PIN – Receivers: 4.8 Gbps (130 nm CMOS)
  - ADCs (building block for PAM4 receivers): 56 GS/s (28 nm CMOS)
  - Electrical cable drivers and receivers: 1.28 / 2.56 / 4.8 / 10.24 Gbps (65 / 130 nm CMOS)
  - RF mixers (for Rx & Tx): BW: 5.6 Gbps – OOK, Carrier: 60 GHz (130 nm BiCMOS)
    BW: 30 Gbps – BPSK, Carrier: 240 GHz (SiGe HBT)

- **Challenges**:
  - Maintain high-speed performance for very high radiation levels:
    - CMOS: TID > 100 Mrad
    - BiCMOS and SiGe: NIEL > 10^{15} n/cm^2
  - Some detector systems will need Low-Power ASICs
  - Some requirements "Incompatible" with CMOS technology scaling:
    - High voltages/currents required by VCSELs [specially at end of life]
    - High biasing voltages for PIN-Diodes [specially at end of life]
    - High modulation voltages needed to drive External Modulators
  - Should, in all cases, HEP follow the technology scaling?
    - Stay with older nodes for some applications?
    - Use more "exotic" technologies (BiCMOS, SiGe HBT, etc.)
      - Requires technology validation for rad-hard applications!
      - Does the community has the resources to deal with multiple technologies?

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KIT
KU Leuven
SMU – EE
SMU – PH
WADAPT

Electrical Links

- Electrical Links have been developed for:
  - Relatively short distances between frontends and SerDes ASICs
    - Up to 1.28 Gbps
    - Up to a few meters
  - Very short distances between SerDes and LD – driver / PIN – receiver
    - Up to 10.24 Gbps
    - ~ cm
- Can be a way to "escape" the relatively rad-hard environment of the central detectors [before going optical]
  - e.g. RD53 pixels: High-Speed transmission over low mass cables (high attenuation and low bandwidth)
    - ATLAS: Up to 6 m @ 5 Gbps
    - CMS: Up to 2 m @ 1.28 Gbps
- **Challenges**:
  - HEP needs the use of low mass cables with their inherent bandwidth limitations
  - 5 / 20 Gbps electrical links over distances of a few meters needed
  - Development of pre-emphasis & equalization to overcome the bandwidth limitations
  - PAM4 (4-level Pulse Amplitude Modulation):
    - To circumvent the limitations of the data transmission medium (10 / 20 Gb/s)
    - Plus equalization to minimize the channel impairments

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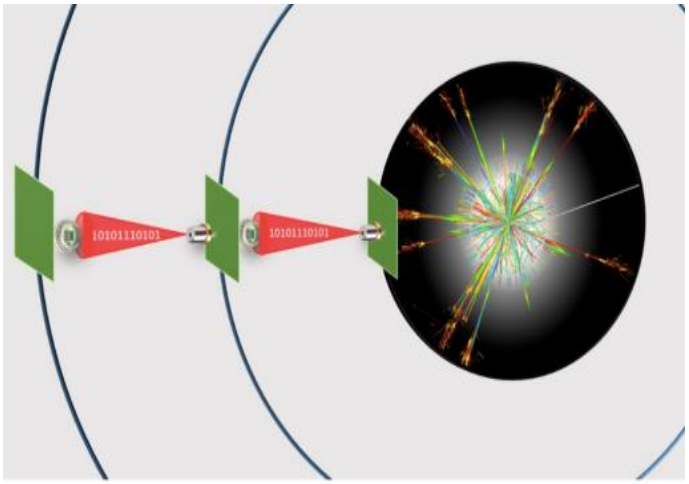
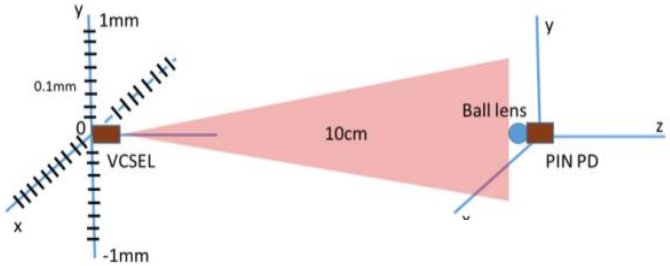
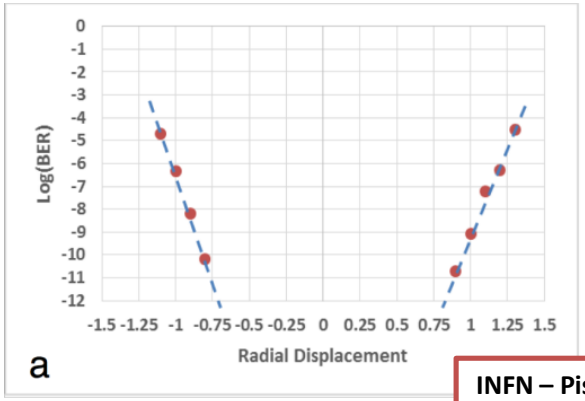
SMU – PH

Free-space Optics

- Principle:
  - "Line of sight" optical transmission:
    - Target distance: 10 cm
  - Data is repeated at each detector layer
    - Electrical – Optical - Electrical
- **Benefits**:
  - Enables inter-layer communications (e.g. Triggering)
  - Avoids the use and installation of optical fibers
    - Collimating structures (lenses) needed
- **Challenges**:
  - NIEL radiation effects on PIN / VCSEL
  - The "geometry" of the data transmission system needs to be built into the detectors:
    - Alignment: ±0.75 mm @ 4.25 Gb/s
  - Bandwidth increases every time a layer is crossed:
    - Data from successive layers add up
    - Either more bandwidth or channels needed in the outer layers
  - Regenerative repeaters are [likely] needed along the repeating chain to contain the BER
  - Links between the outer layer and the counting room are likely to be "conventional" optical links



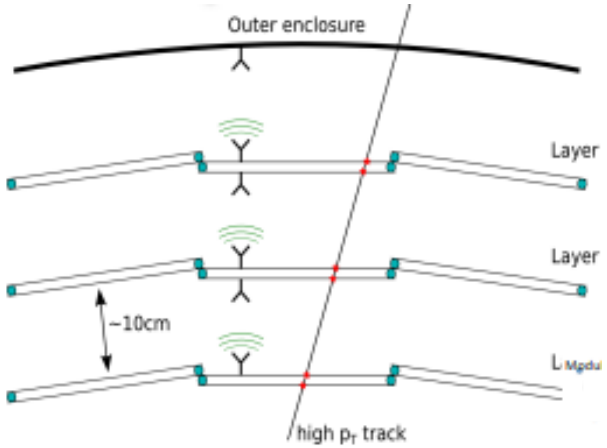


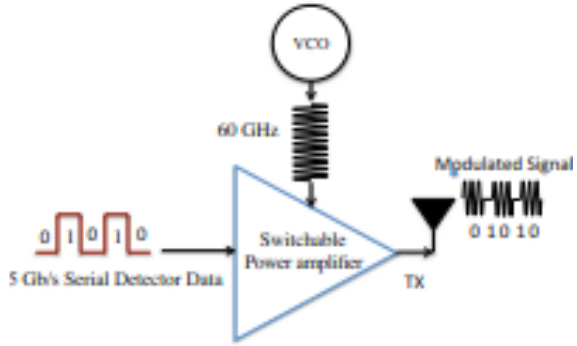


INFN – Pisa

RF

- Principle:
  - The signal is modulated on a high frequency carrier and transmitted (using antennas) between two successive detector layers
    - Data rate ≈ 1/10 carrier frequency (OOK, BPSK)
  - Data is repeated at each detector layer
- **Benefits**:
  - Enables inter-layer communications (e.g. Triggering)
  - No optoelectronics components needed
  - No optical fibers to be installed
- **Challenges**:
  - Needs the use of high-directivity antennas to avoid cross talk
  - Other challenges as for Free-space Optics (except no optoelectronics)



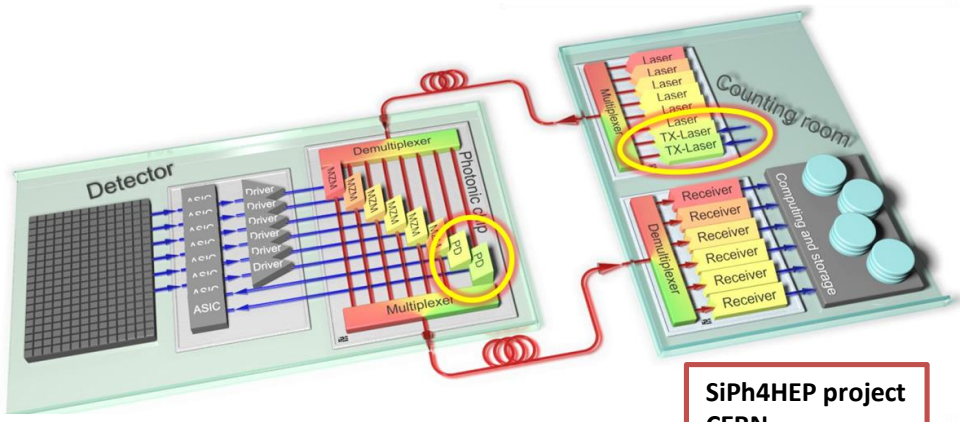


WADAPT

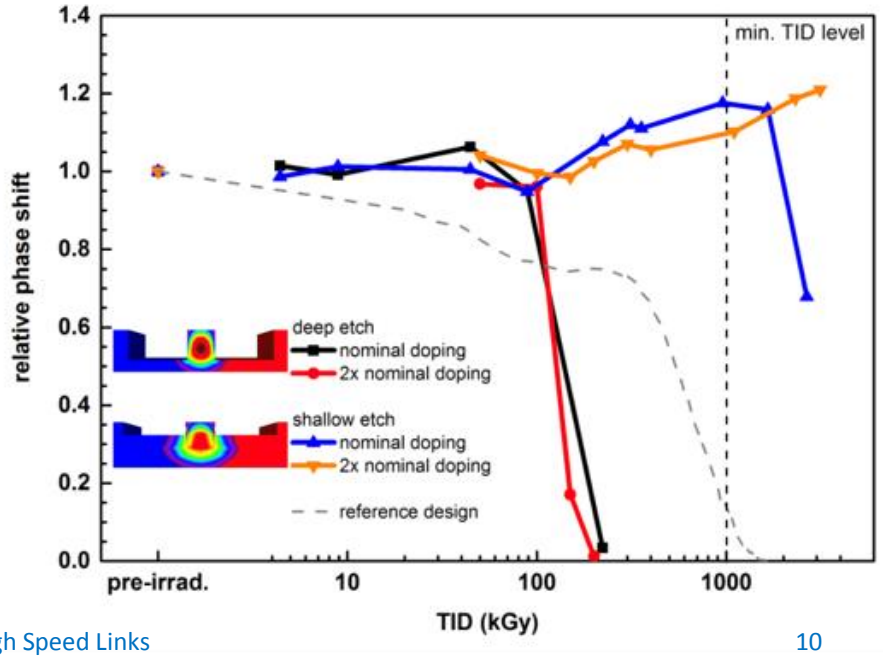
Si-Photonics

- Integration of optoelectronic devices in a “Photonic Si chip”
  - Wave-length-division multiplexers
  - Modulators
  - Photodiodes (Ge)
- **Benefits**:
  - Tight integration with FE ASICs possible
  - Laser kept out of radiation environments
  - Number of fibers drastically reduced
  - Potential for 40 Gb/s NRZ

- **Challenges**:
  - Still a maturing technology
  - Design tools lagging behind ASICs
  - MZMs require:
    - High modulation voltages (3 – 8 V_{pp})
    - Into 50 Ω
  - MZM insensitive to NIEL but sensitive to TID:
    - But progress has already been made in the community!

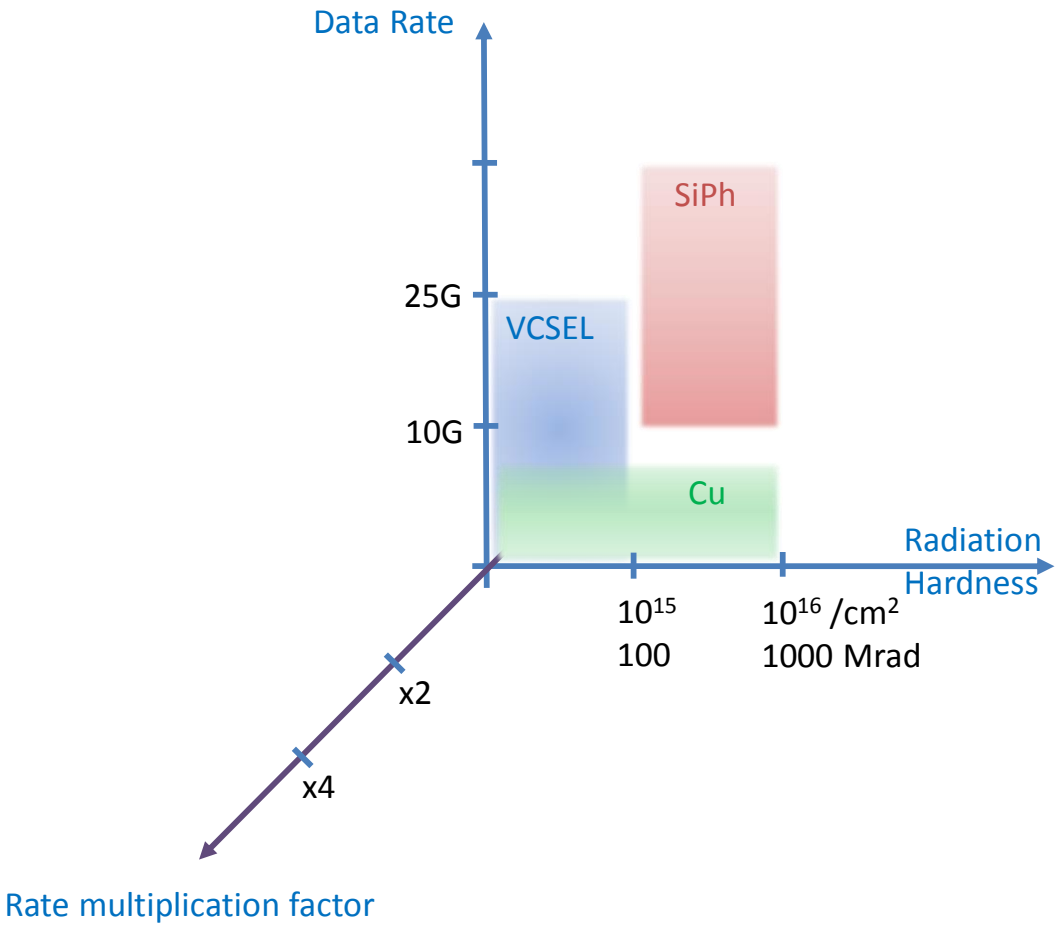


SiPh4HEP project
CERN
KIT
INFN
Bristol

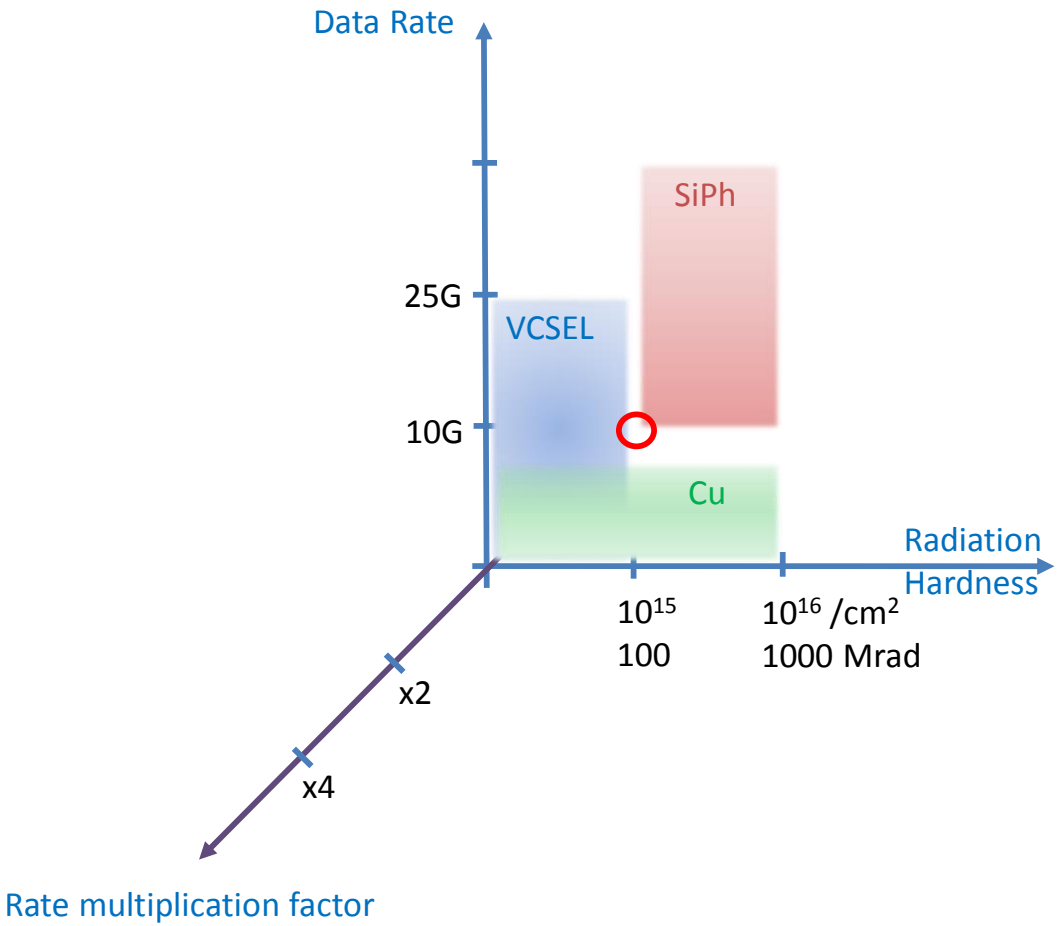


Development Space

Technologies

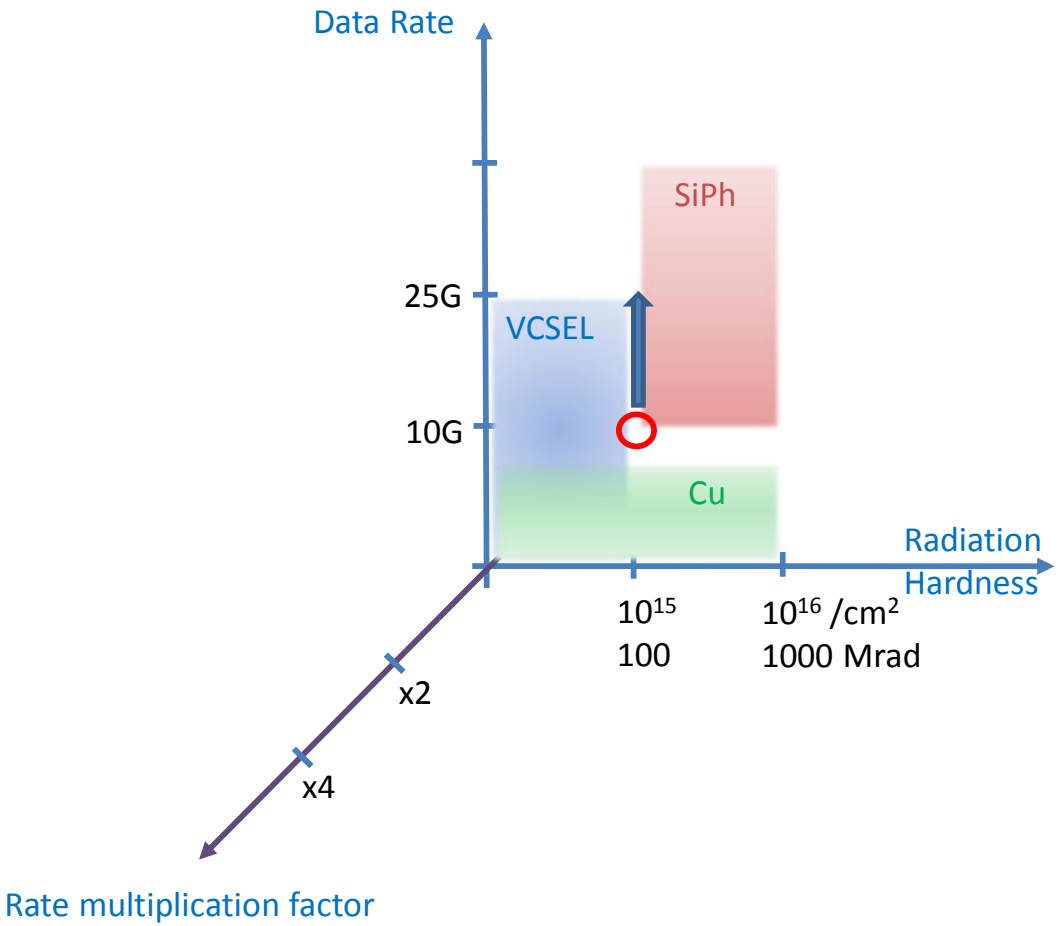


Current Developments



Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future: Higher Data rates

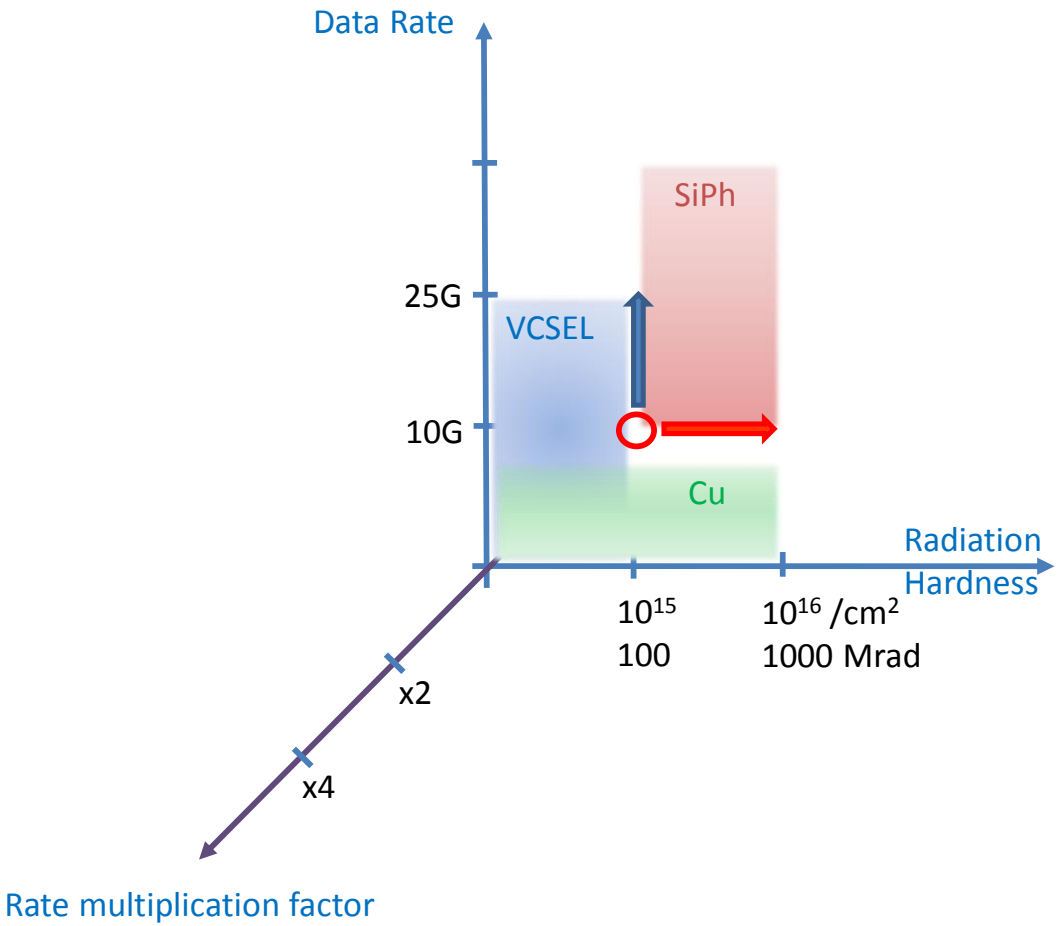


Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future developments:

1. Higher Data rates

Future: Si-Photonics



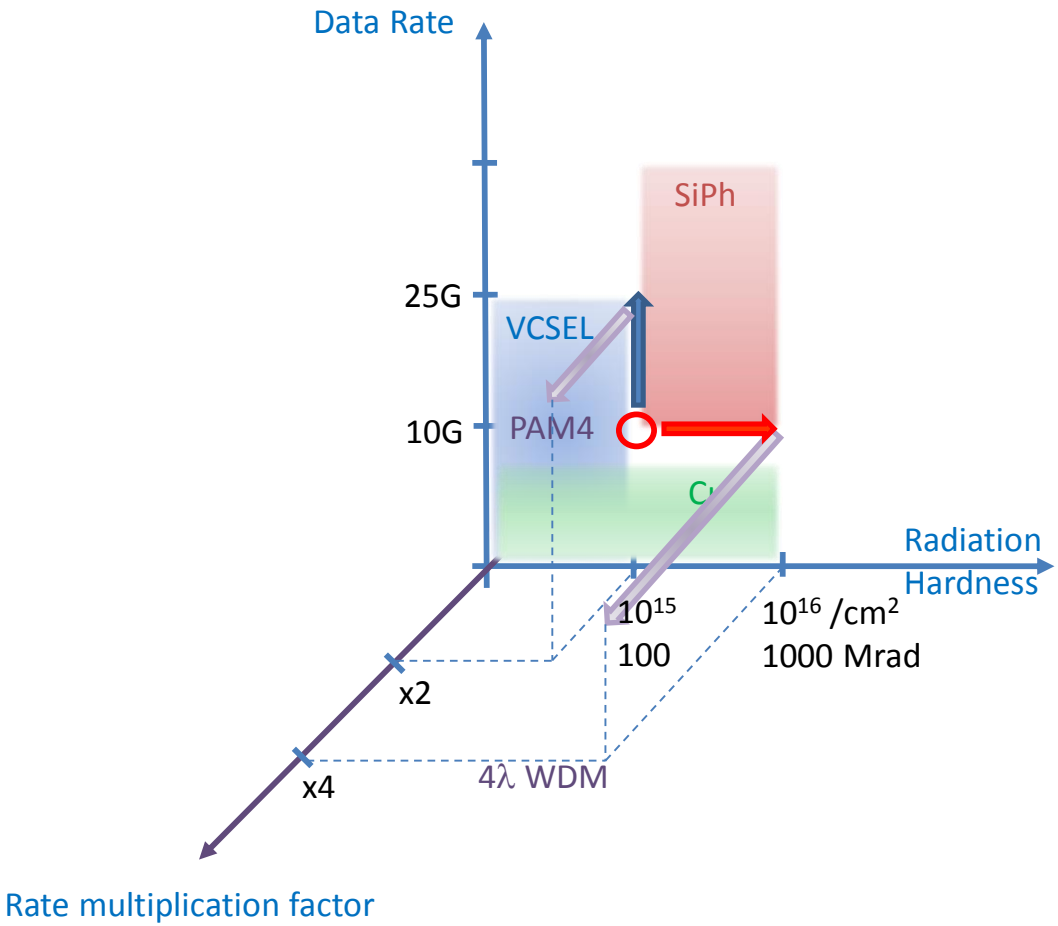
Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future developments:

1. Higher Data rates

2. Si Photonics:

Future: λ - Multiplexing & PAM4



Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

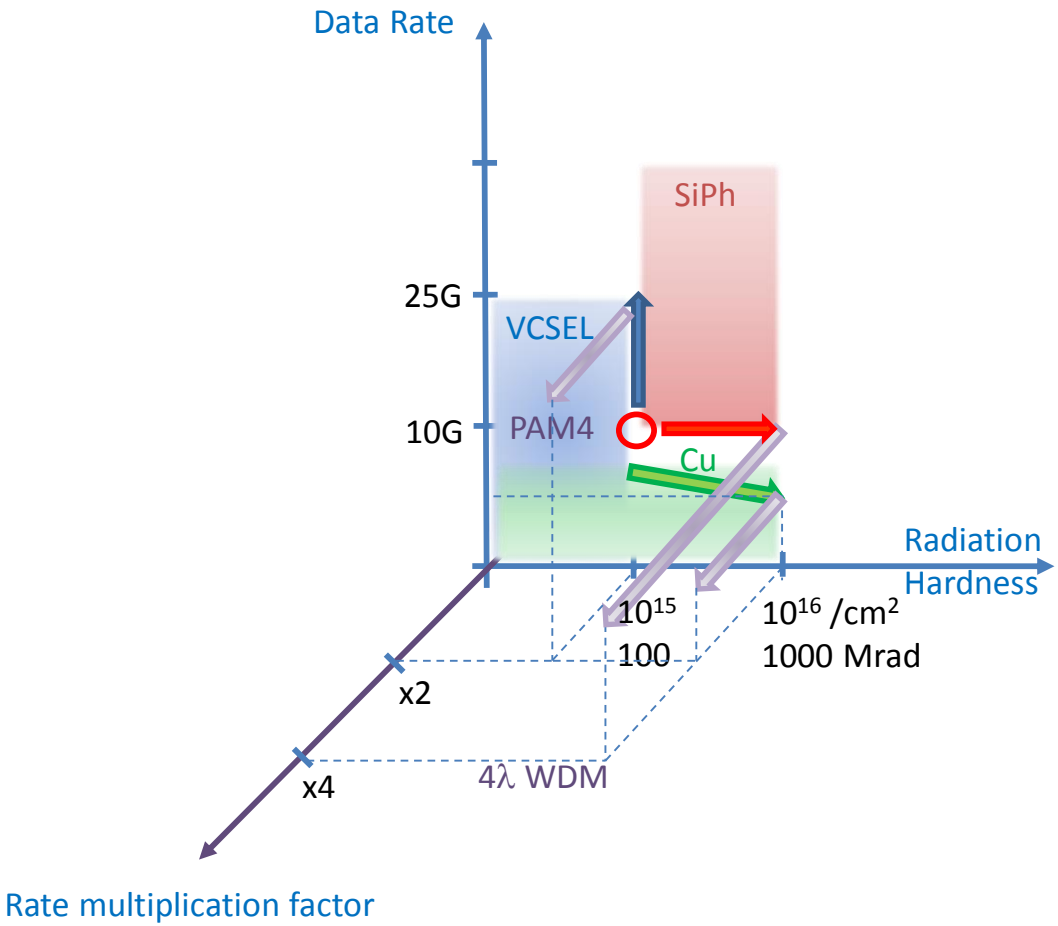
Future developments:

1. Higher Data rates

2. Si Photonics:

3. λ Multiplexing and multi-level signalling (PAM)

Future: Electrical over low mass copper



Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future developments:

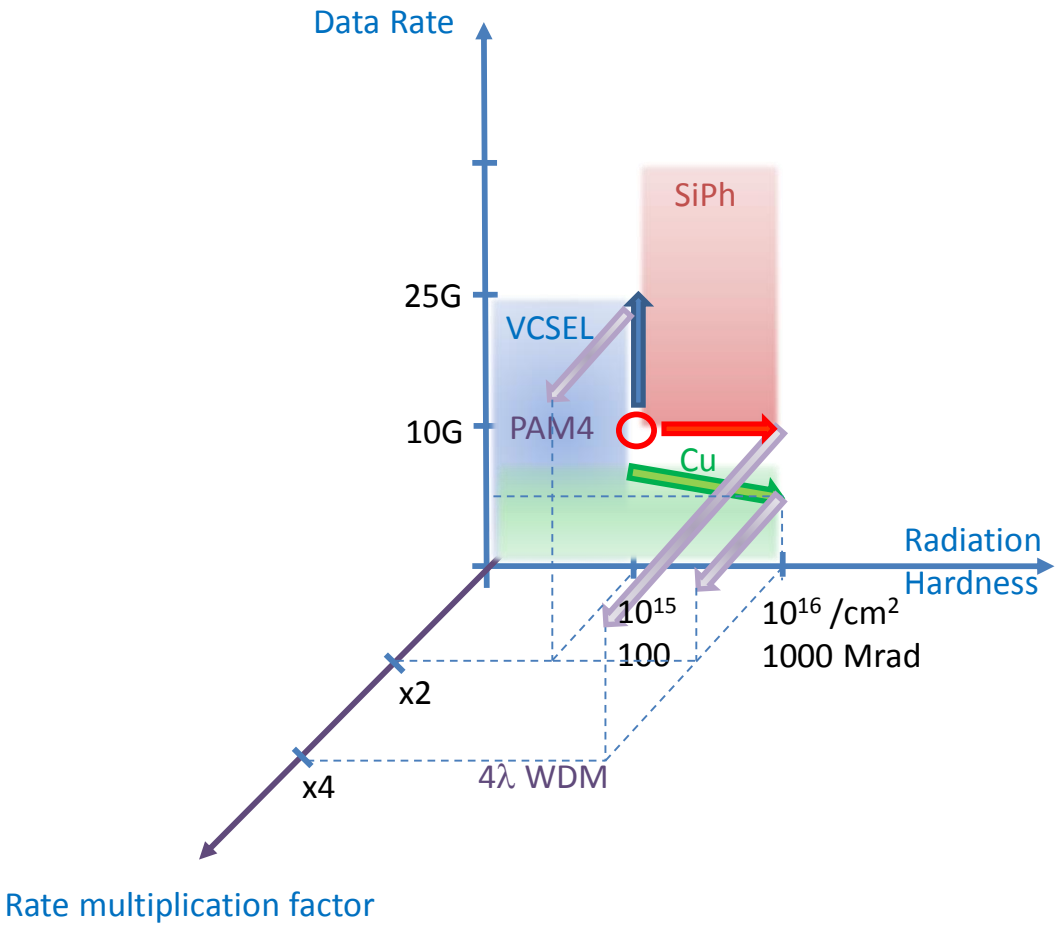
1. Higher Data rates

2. Si Photonics:

3. λ Multiplexing and multi-level signalling (PAM)

4. Low mass copper links and multi-level signalling (PAM)

Future: Electrical over low mass copper



Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future developments:

1. Higher Data rates
2. Si Photonics:
3. λ Multiplexing and multi-level signalling (PAM)
4. Low mass copper links and multi-level signalling (PAM)

The "missing dimension" is Power:

- Depending on the system, low power operation may be imperative!

Summary

- The community is exploring new [and old] ways to provide the bandwidth needed to read out detectors
- Some of the technologies are well know in HEP:
  - Optoelectronics / Electrical Links and Communication ASICs
  - In line with the industrial developments these paths can [and will] certainly be carried forward
- Newer technologies are also being considered:
  - Free-space optics / RF / Si-Photonics
  - The understanding of their potential in HEP is still at its infancy but they broaden the range of possibilities
- Building detector systems without FPGAs is not an option so their roadmap has to be closely tracked in HEP
- The over-riding challenge is radiation:
  - For CMOS, SiPh: TID > 100 Mrad
  - For Optoelectronics, SiGe: NIEL > 3×10^{15} n/cm^2
  - Need to define the target environment!
    - Solutions need to be tailored to Detector and Rad-Hard environment!
- Low-power operation needed for inner detector systems
- But, practical viability and “industrialization” effort can’t be underestimated when the target is producing 10k-100k links