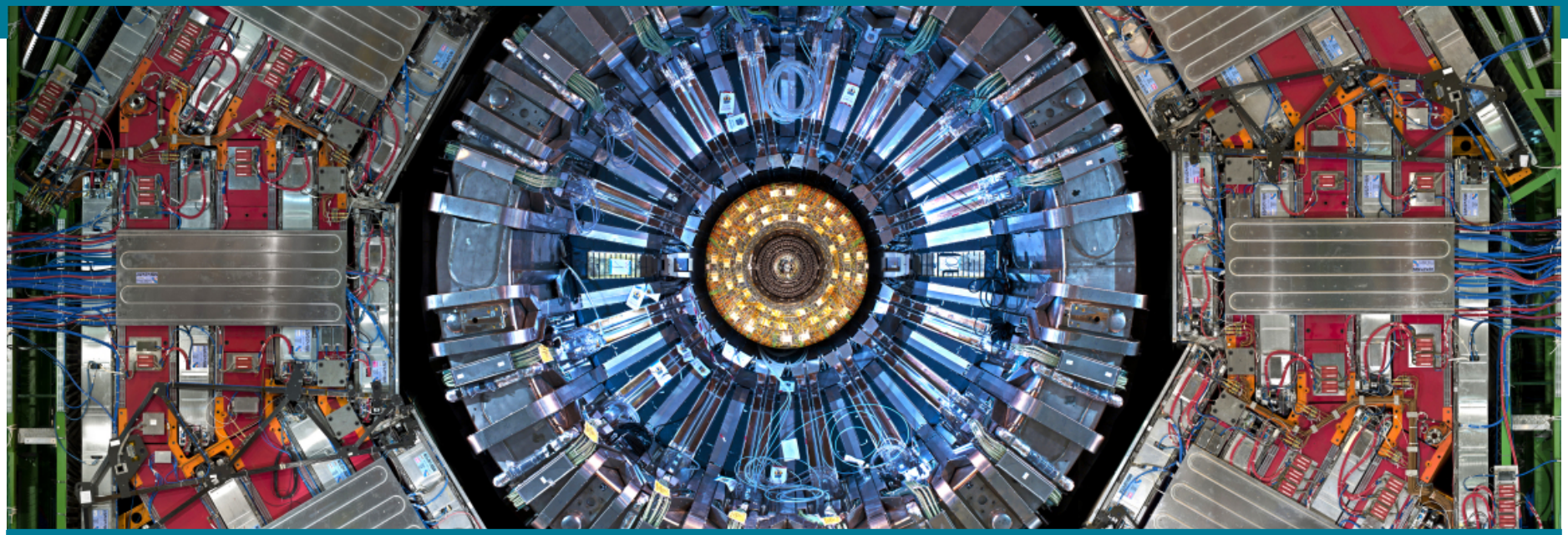
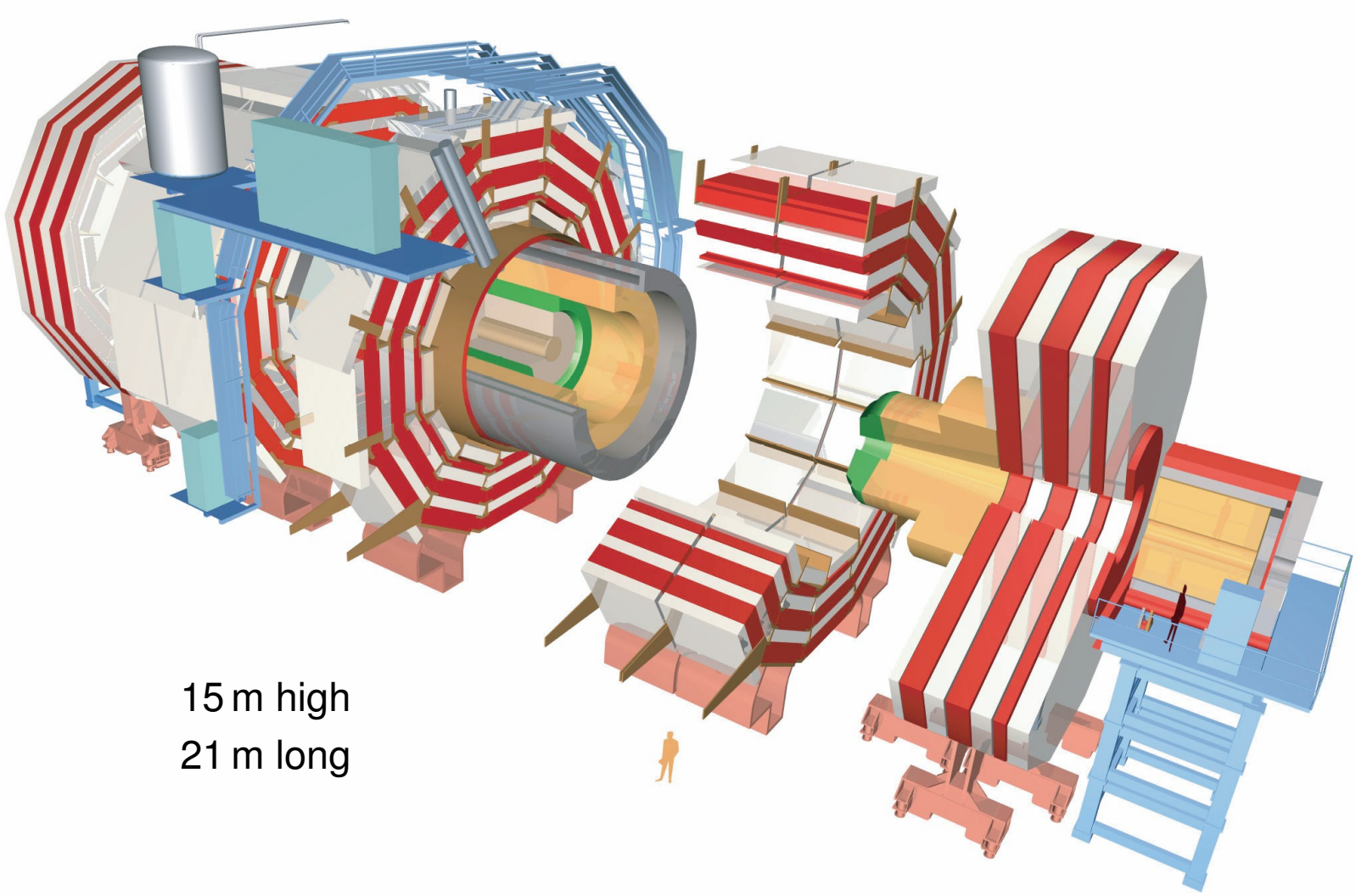
ETH zürich



Serial powering for the Phase 2 Upgrade of the CMS Pixel Detector at CERN's LHC

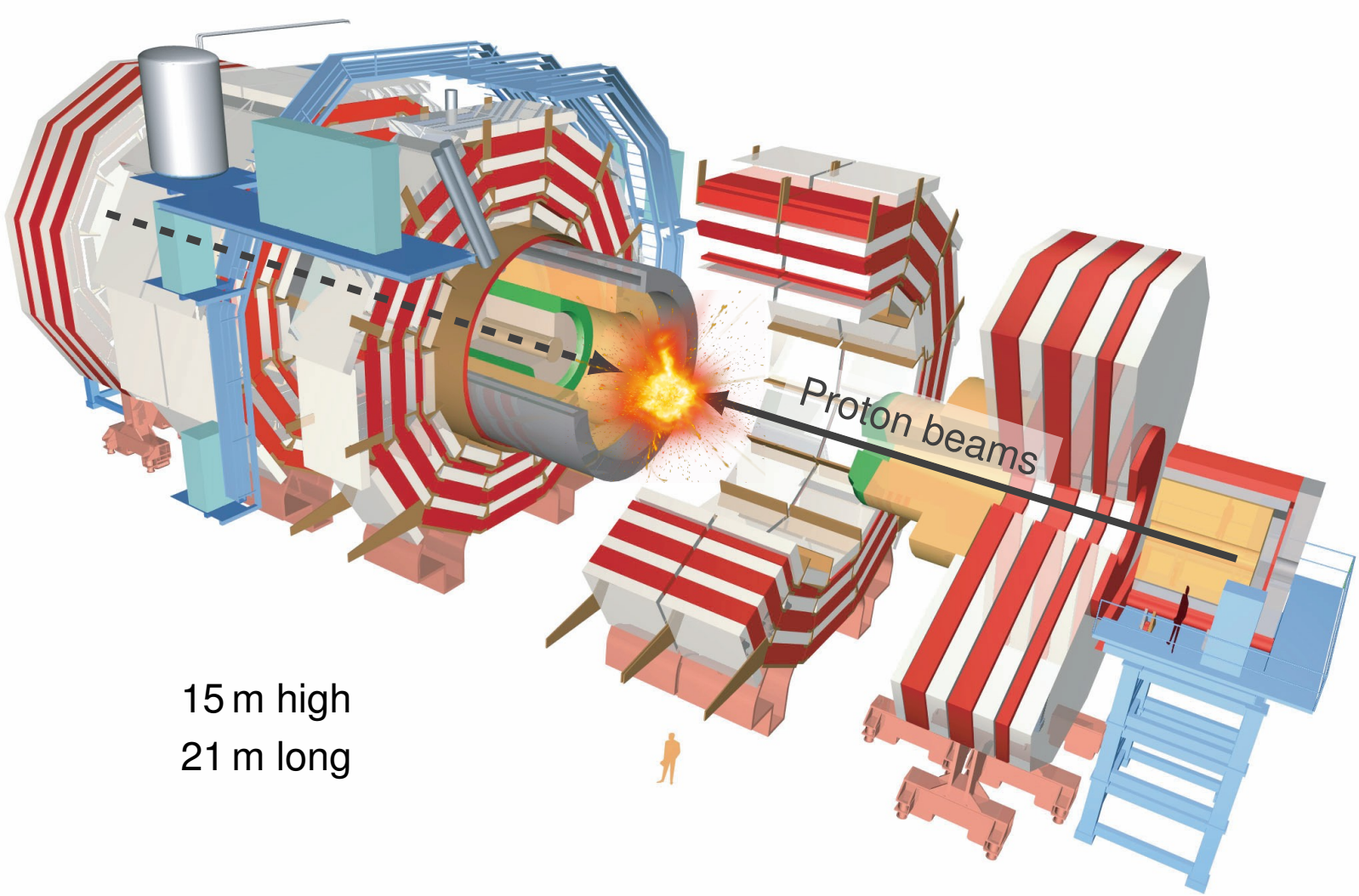
Daniele Ruini

The CMS detector at the LHC

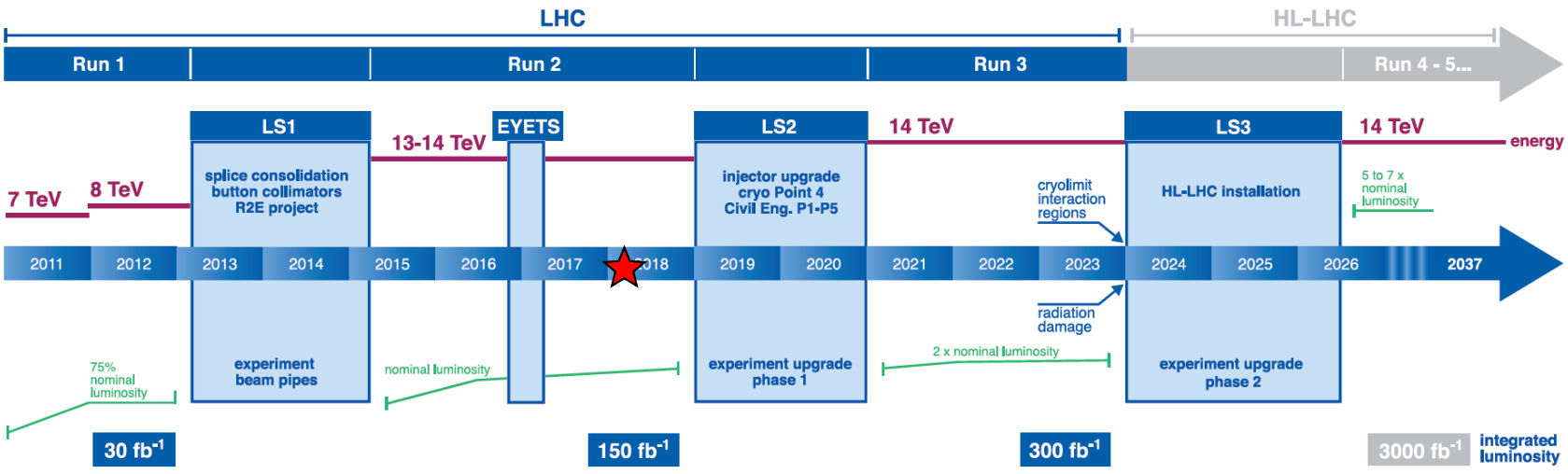


15 m high
21 m long

The CMS detector at the LHC

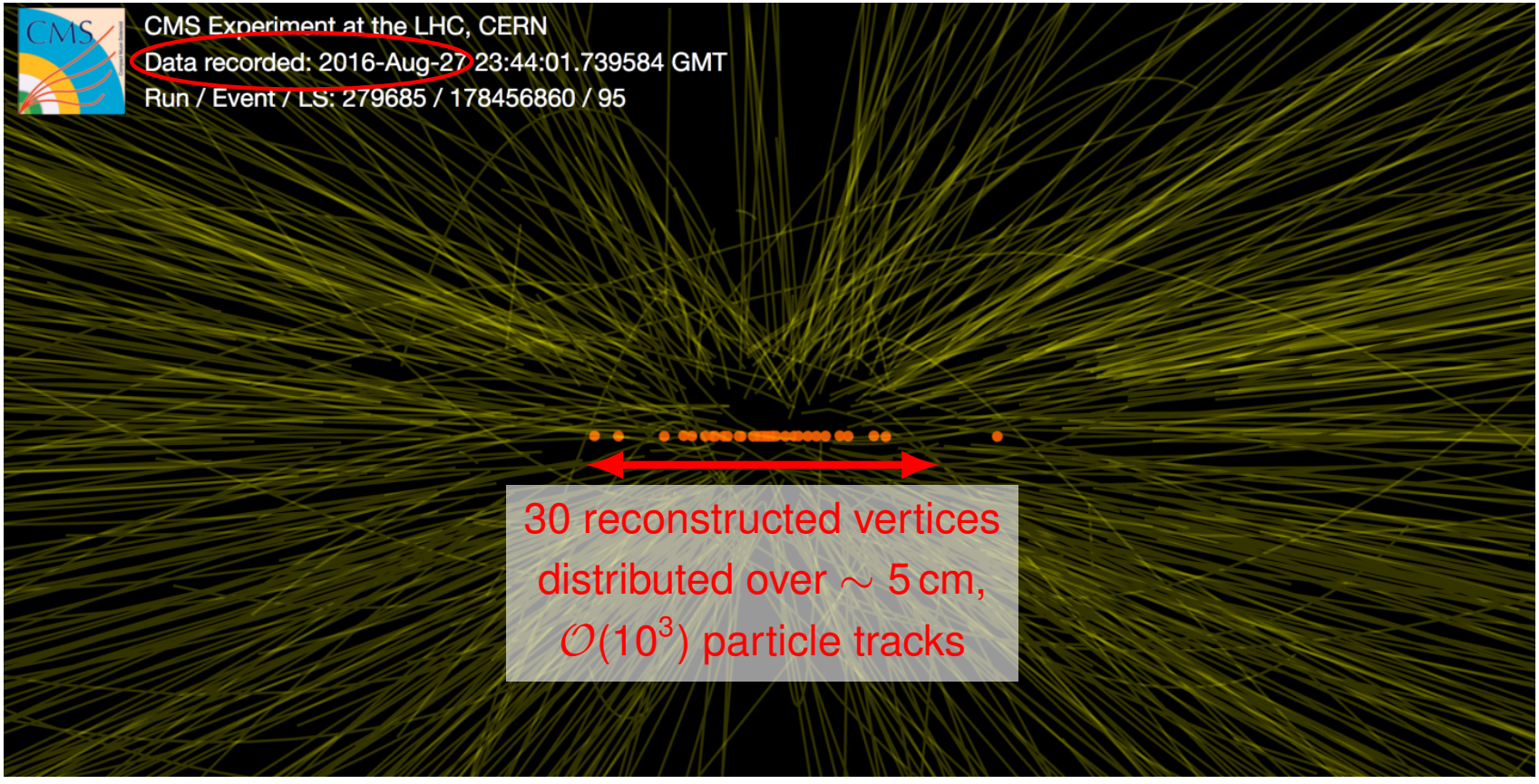


LHC / HL-LHC Plan



- After LS3 the instantaneous luminosity will increase to up to 7.5 times the initial design luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.
- New sensors and new electronics are necessary to further collect high quality data.

The challenges of High Luminosity



The challenges of High Luminosity, cont.

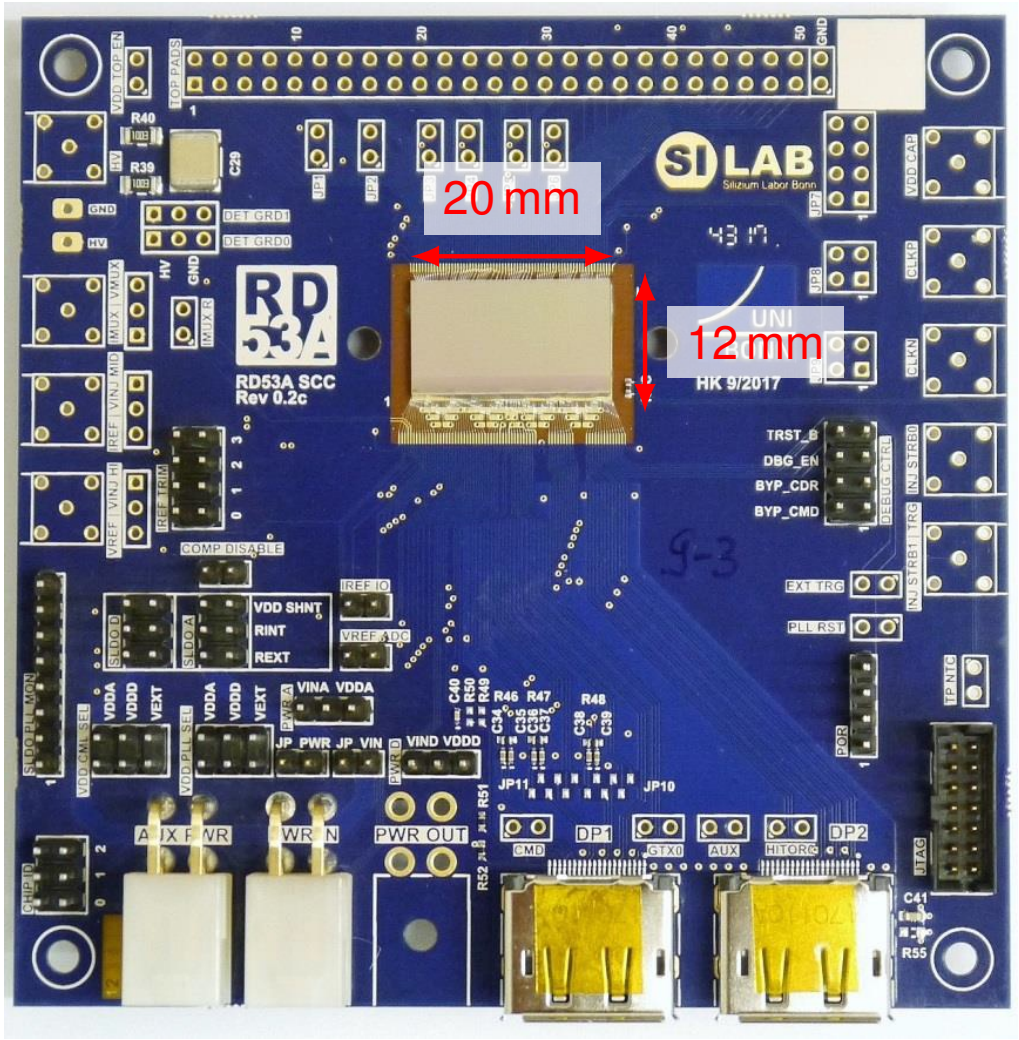
High Luminosity Upgrade means:

- Up to 200 simultaneous proton-proton collisions.
- $\mathcal{O}(10^4)$ particles produced per bunch crossing.

The detector must:

- Be able to handle the amount of data produced.
- Survive the extreme radiation doses.

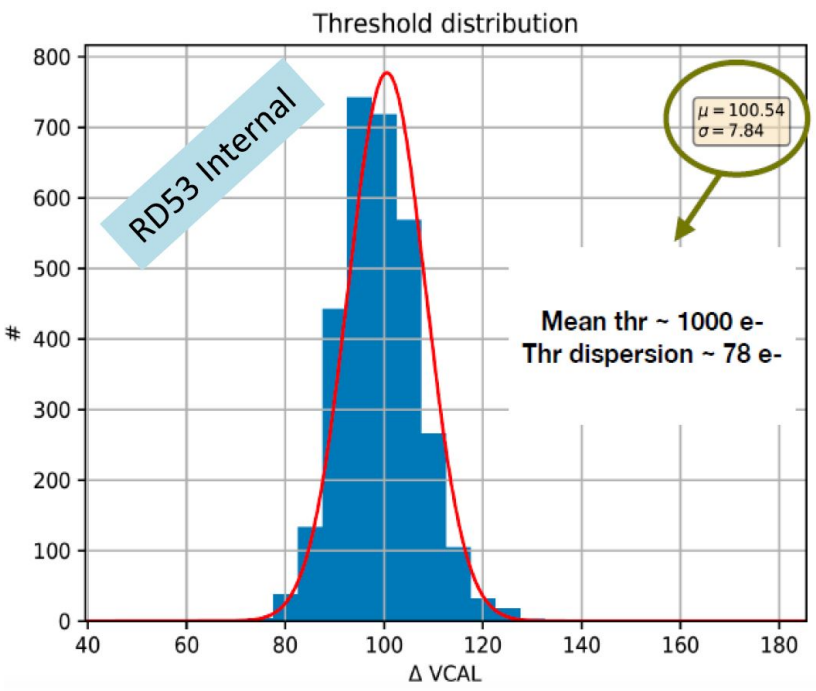
RD53A: a large format IC prototype for Phase 2

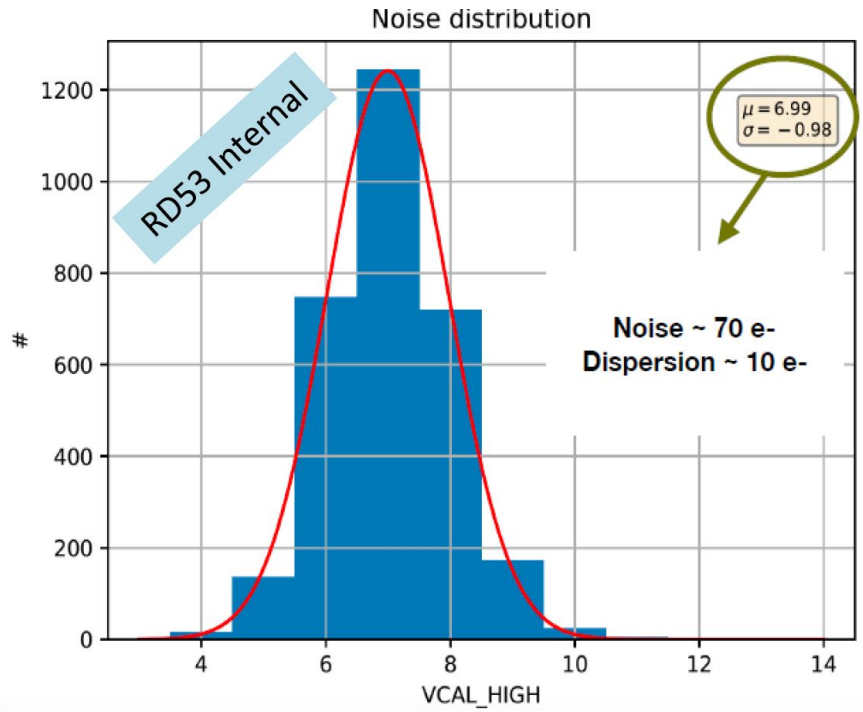


- Realized in 65 nm CMOS technology.
- Operates at 1 V and 2 A.
- Matrix of 192 $\times$ 400 pixels of 50 $\times$ 50 µm^2.
- Will soon receive some here at ETH.

The chip is alive!

- First tests of the chip are working as expected.
- An example: threshold measurement performed in Bonn.

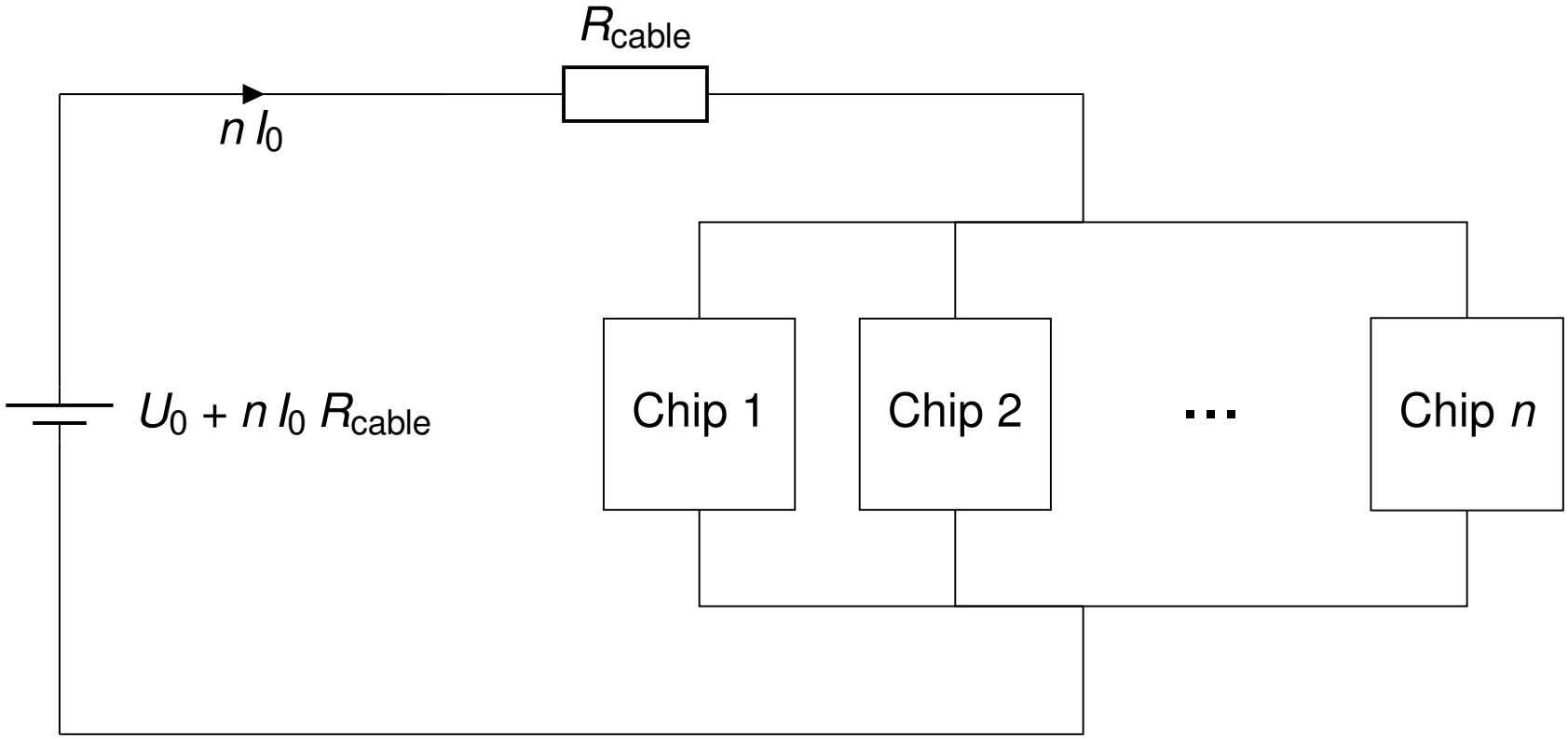




Powering the pixel detector

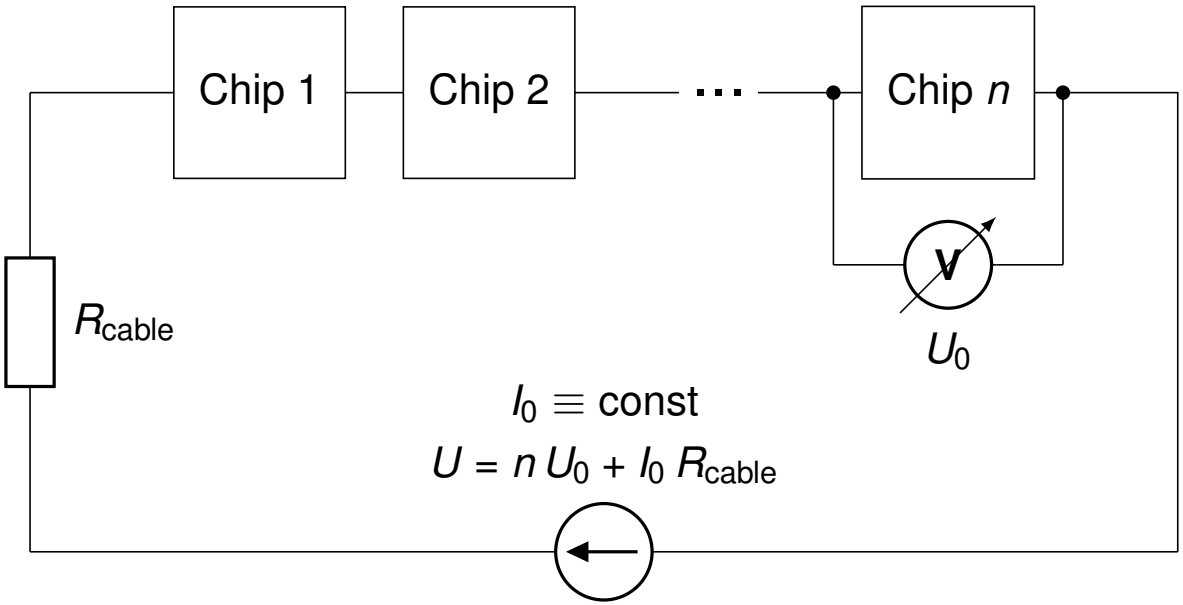
- The detector will consist of 13488 pixel chips.
- If powered in parallel: 27 kA.
- Solution: chains of several pixel modules powered serially.

A system powered in parallel



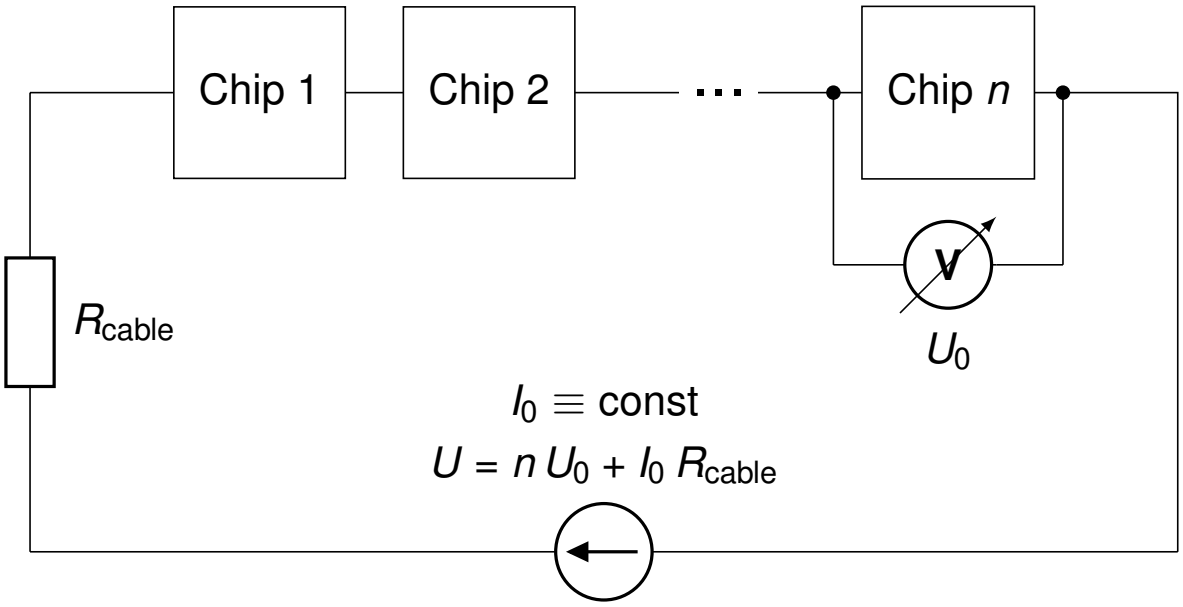
Power lost in the cables: $P_{\text{cable}} = R_{\text{cable}} \cdot (n\,I_0)^2 \propto n^2$.

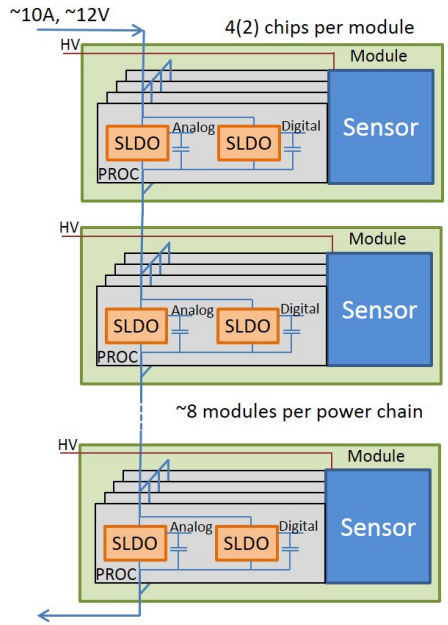
A system powered in series



In a serially powered system the chips share the supply current, which flows from chip to chip. $P_{cable} = R_{cable} \cdot I_0^2$.

A system powered in series





In a serially powered system the chips share the supply current, which flows from chip to chip. $P_{cable} = R_{cable} \cdot I_0^2$.

Serial vs parallel powering

Pros

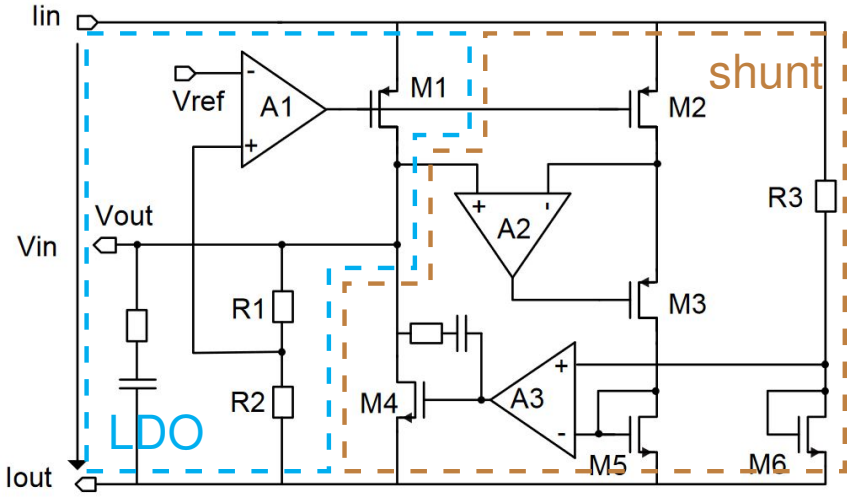
- Huge improvement in power efficiency w.r.t. parallel powering.
- Constant current consumption: avoids possibly lethal voltage transients.
- Only technically possible option to deliver power to the detector with an acceptable cable mass.

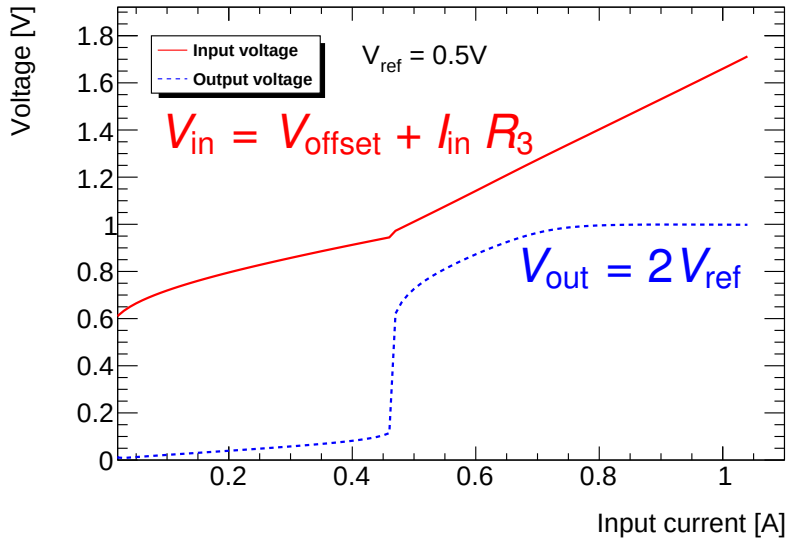
Cons

- Increased fragility: failure of one element could compromise the entire chain.
- Increased complexity: an on-chip regulator is required to convert the input current into a constant input voltage.

Shunt-LDO regulator (designed by M.Karagounis)

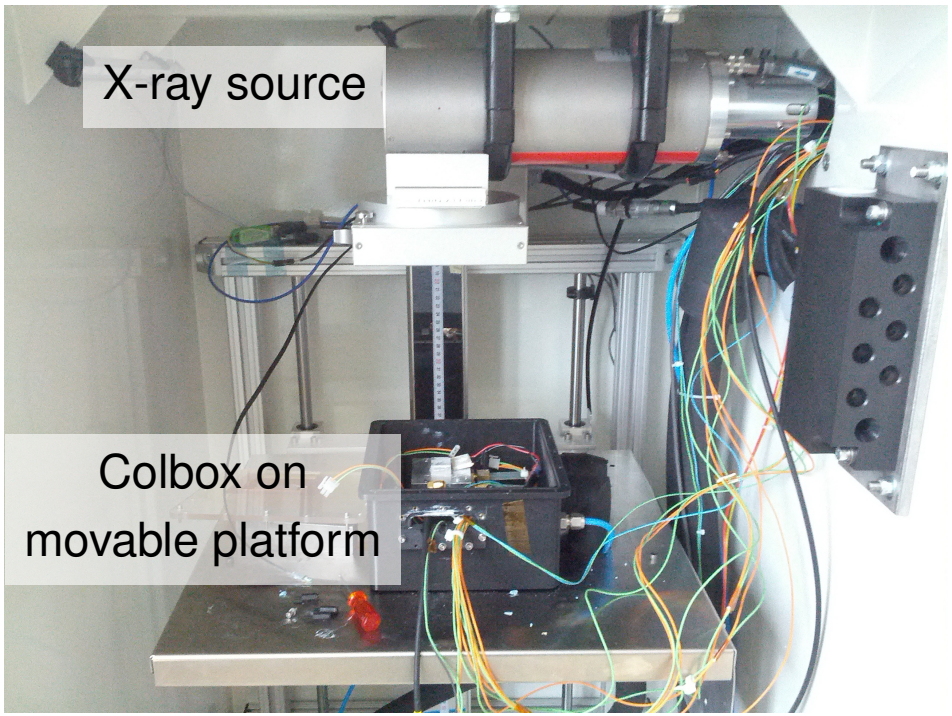
- Provides constant voltage to the load.
- Shunts excess current in transistor M4.
- Configurable effective resistance and offset.
- Circuit integrated in RD53A and ATLAS' FE-I4 chips.

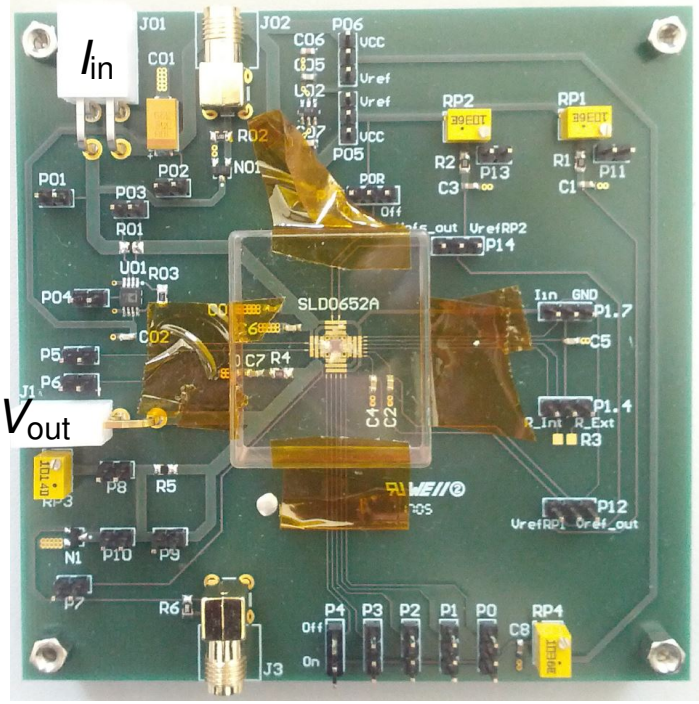




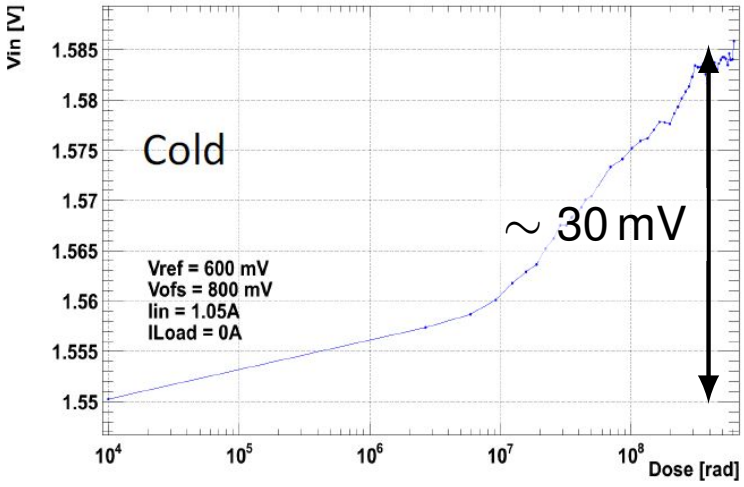
SLDO X-ray irradiation to 6 MGy at CERN

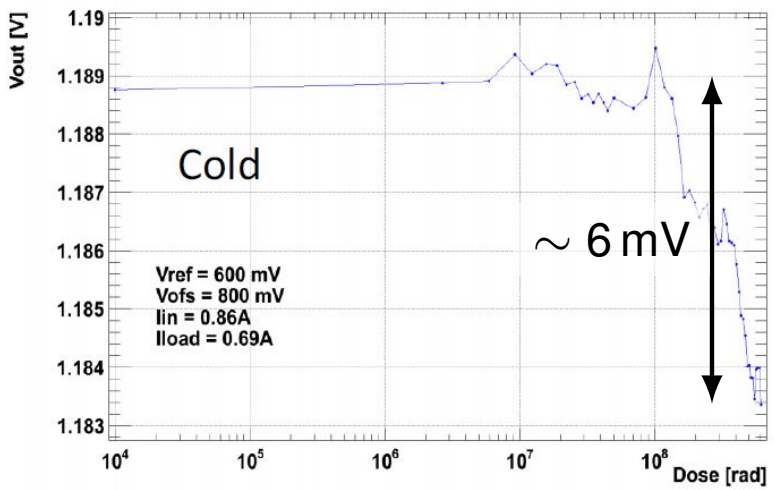
- Performance of a 65 nm, 2 A SLDO prototype has been tested for radiation hardness up to 6 MGy in April 2017.
- One chip irradiated at room temperature, one at $-10°C$.
- Only effect: very small changes in V_{in} and V_{out}

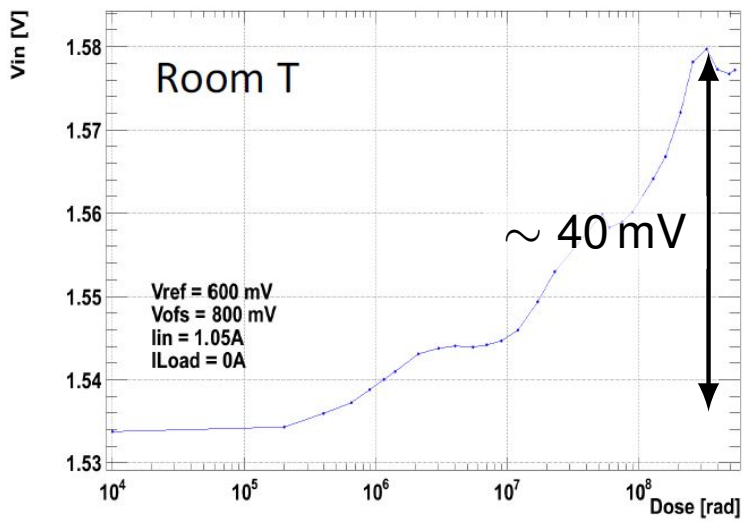


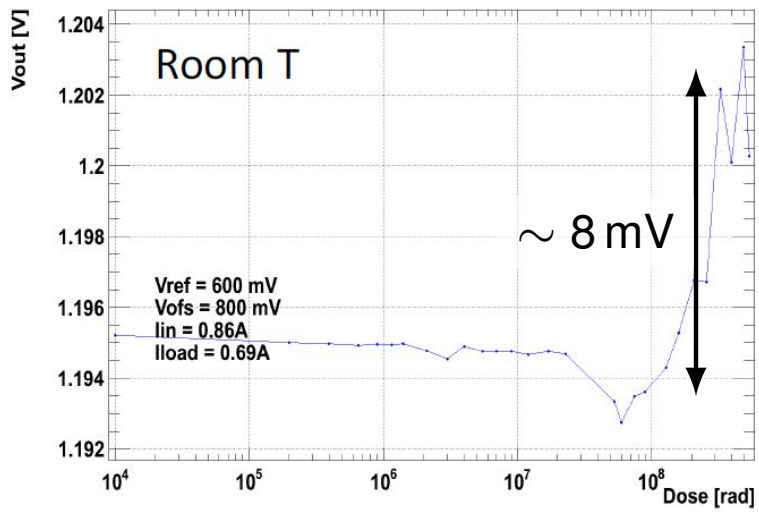


SLDO irradiation to 6 MGy at CERN: results

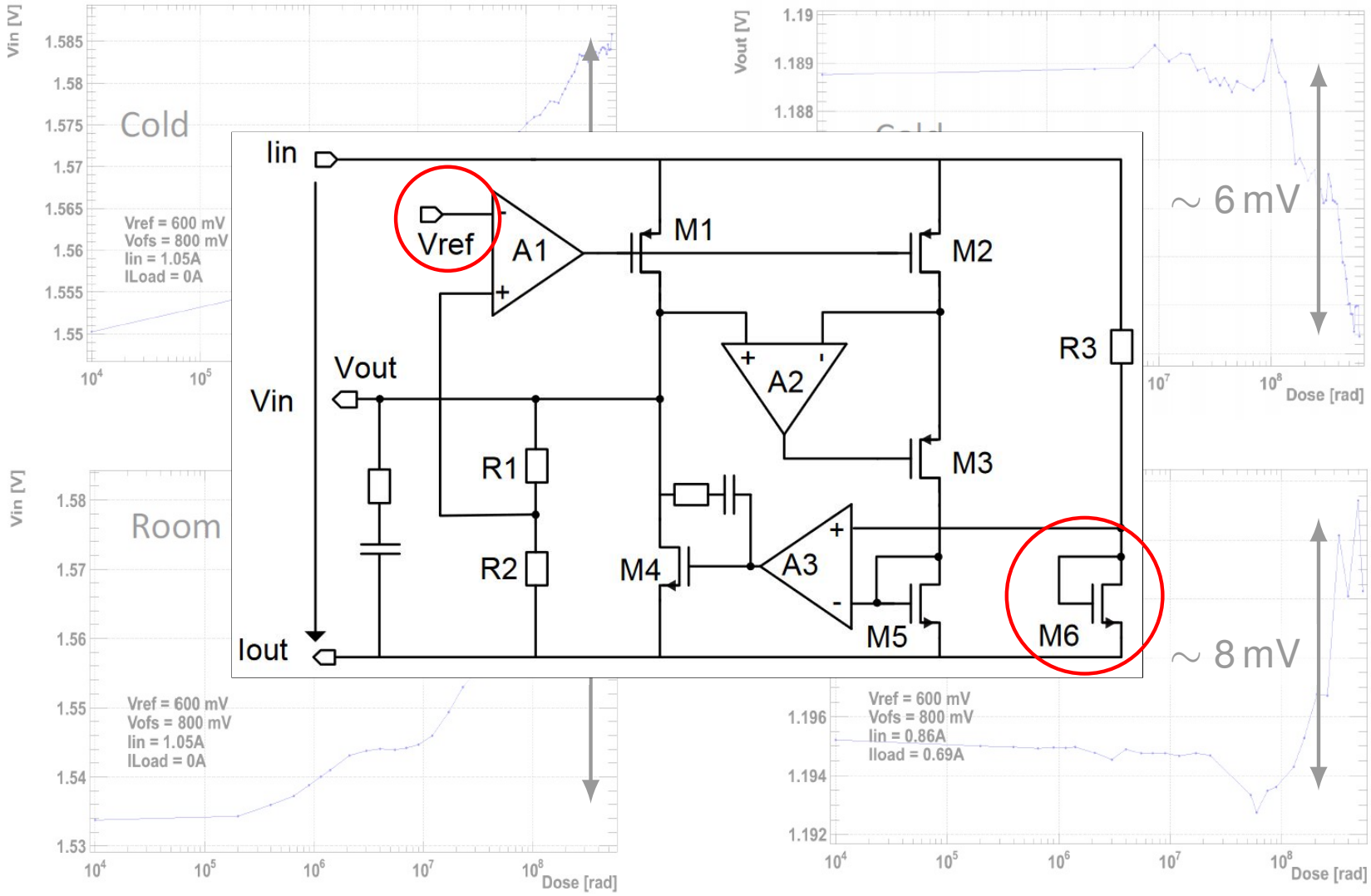




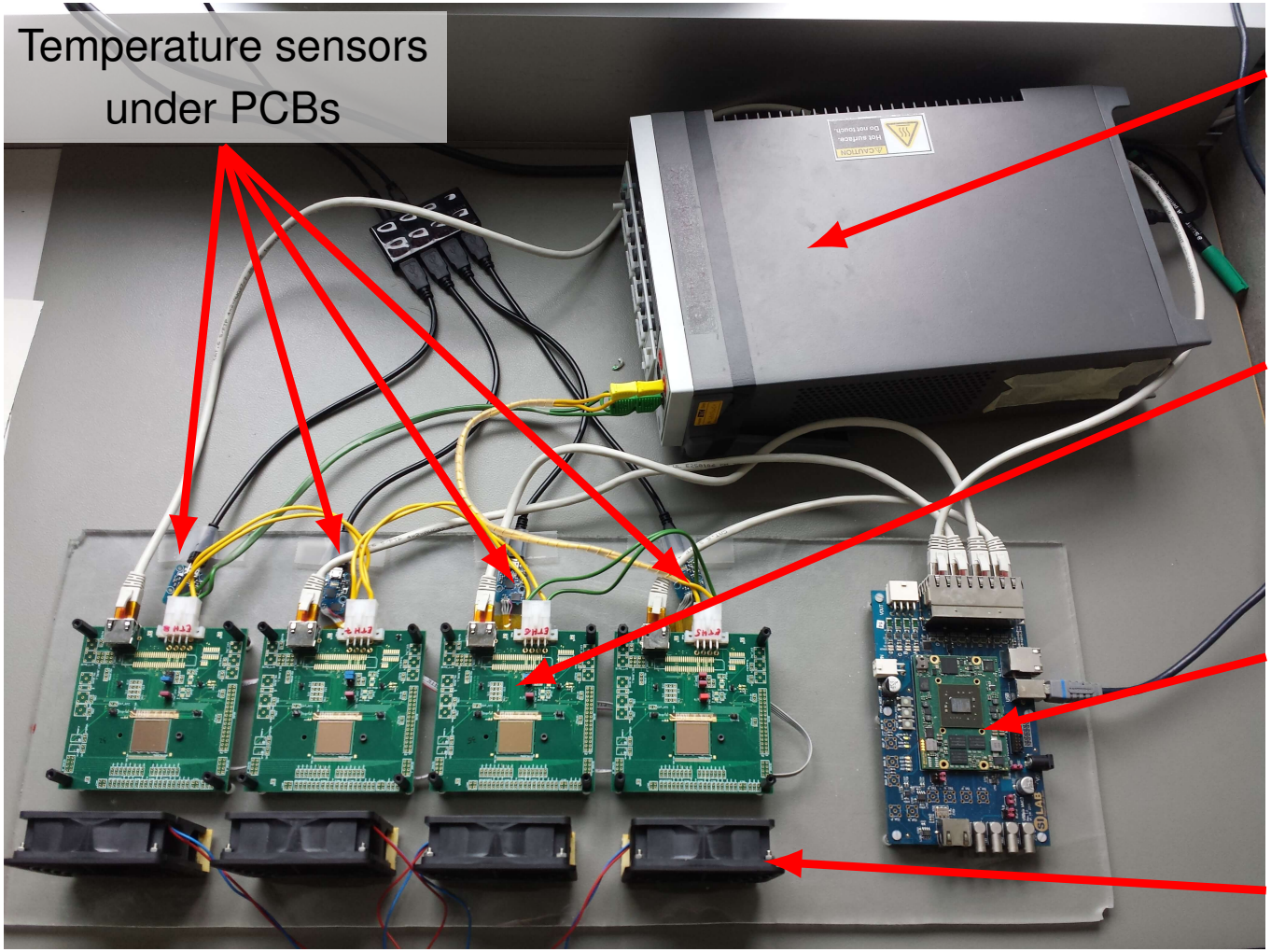




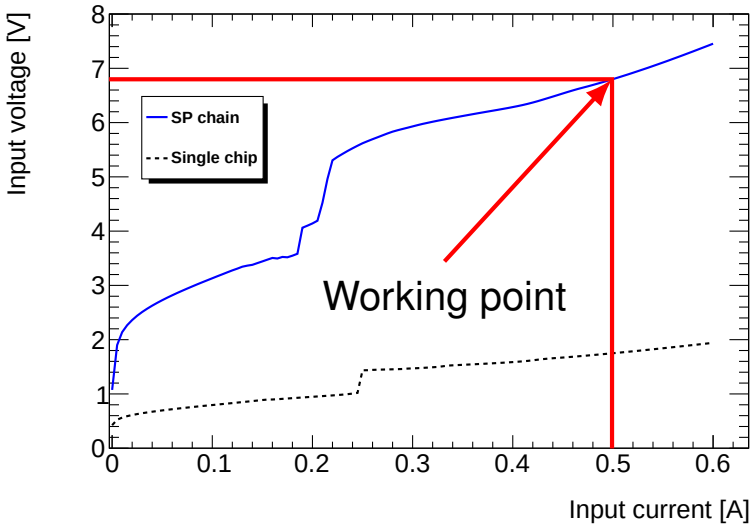
SLDO irradiation to 6 MGy at CERN: results

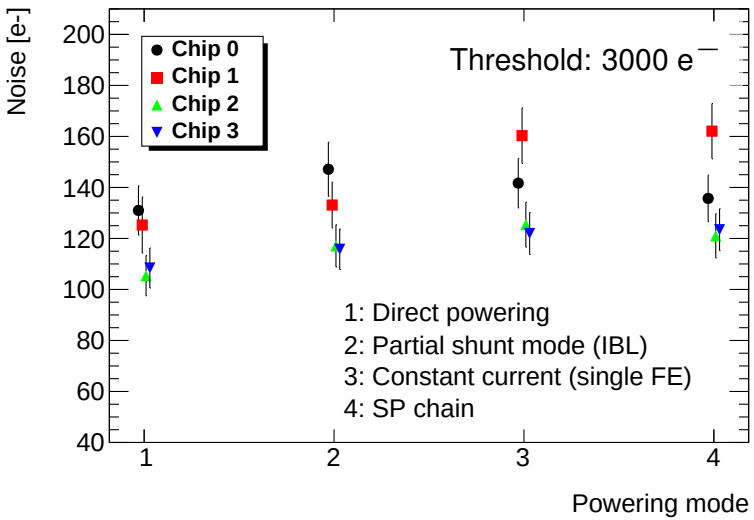


Serial powering setup at ETH



I–V and noise of the SP chain



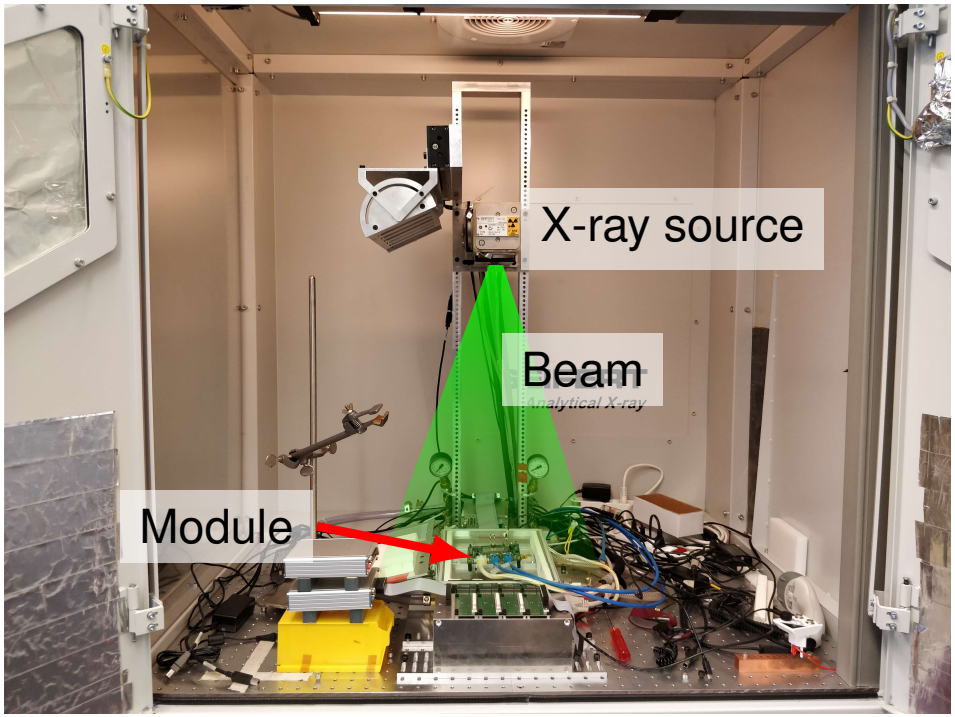


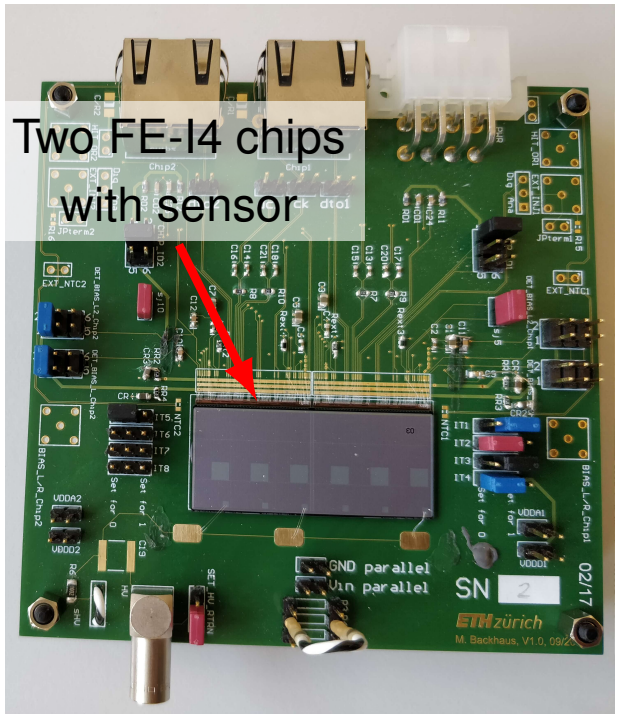
- I–V curve of the chain (blue) behaves just like a single chip (black).
- Linear (resistive) behaviour for $I_{\text{in}} \gtrsim 0.4\,\text{mA}$.

- The noise does not depend on the powering mode.

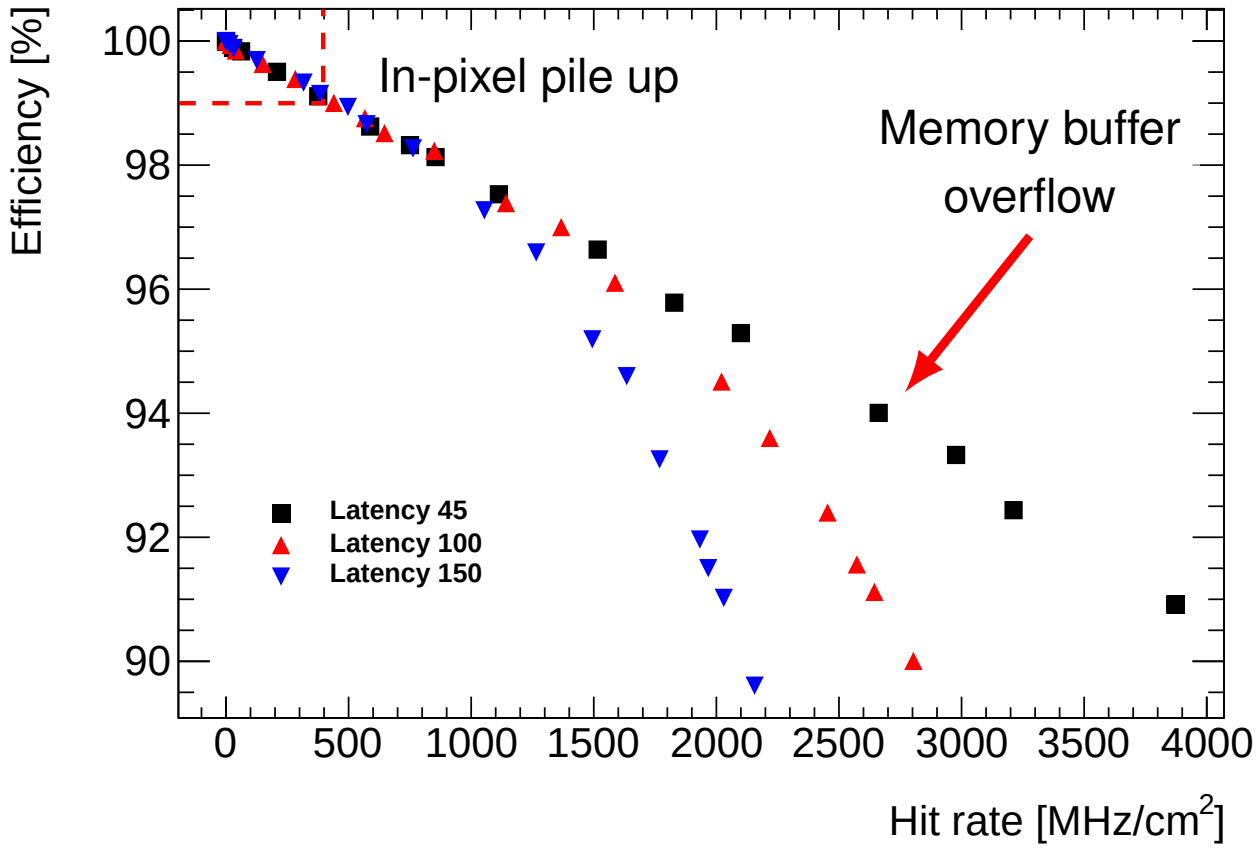
On-module serial powering and high rate efficiency

- Module of two FE-I4 chips in series.
- Measure the probability of receiving injected signals as function of the photon hit rate.
- Part of the Phase 1 module qualification.





High rate efficiency in serial powering



Chip specification (parallel powering): efficiency $>$ 99% at 400 MHz/cm^2.

Conclusions on serial powering

- Serial powering is the power distribution system for the Phase 2 Upgrade of the CMS pixel detector.
  - Affordable cable mass and power efficiency.
- Improved SLDO for on-chip voltage/current regulation.
  - 65 nm and up to 2.0 A current.
  - Radiation hard up to 6 MGy at room and cold temperature.
- Serial powering works!
  - Chain of four FE-I4 single chips.
  - High rate efficiency of on-module serially powered chips.
- Future:
  - RD53A prototype ready to be tested – good first results.
  - Repeat on RD53A the studies done with FE-I4.

Backup

Requirements for the Phase 2 pixel chip

as specified in the Technical Design Report

- Radiation hardness up to 1 Grad (= 10 MGy) and 2.3×10^{16} n_{eq}/cm^2 for an integrated luminosity of 3000 fb^{-1}.
- Occupancy $< 1‰$ for 200 collisions per bunch crossing.
- Efficiency $> 99\%$ up to 3 GHz/cm^2 hit rate.
- Long trigger latency (12.5 µs), in order to use tracking information in the L1 trigger.