AGH University of Science and Technology

Raport from the Hardware Working Group

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Main Objectives of Hardware Group

- Presently the main Hardware Goal is to build a prototype of Compact Multilayer FCAL Detector
  - Within the AIDA-2020 project it is also our deliverable with the deadline originally in first part of 2019, but after the extension of AIDA2020 by one year, the deadline will be moved forward by nine months.
- Proceeding with hardware R&Ds: on sensors, ASICs, mechanics, alignment, DAQ, back-end electronics, …
- Test-beam preparation and data analyses – topic shared with Software&Analyses group

Summary of meetings held
Technical info

- 6 meetings from the last (September 2017) FCAL Workshop at Belgrade – in total 37 meetings
- Duration: ~1-1.5 hour
- Participation: > 5 people

Recent topics and presentations:

- BeamCal sensors and readout
- Design of LumiCal prototype
  - FLAME readout ASIC
  - FPGA-based readout backend
  - Production of new tungsten plates
- Analyses of 2016 test-beam data and preparation of new test-beam

Summary of meetings held
Technical info

Presentations in 32-27 HWG meetings:

- BeamCal operation parameters, Sergej Schuwalow, 32 HWG
- BeamCal Specification Request, Angel Abusleme, 32 HWG
- Rad-hard sensors studies at UC, Bruce Schumm, 33 HWG
- Rad-hard sensors studies at JINR, Uladzimir Kruchonak, 33 HWG
- Ideas for different readout chip at teat-beam, Yan Benhammou, 33 HWG
- Discussion on EPJ paper, Aharon Levy, 34 HWG
- APV calibration with pulse, Oleksandr Borysov, 35 HWG
- Production of tungsten plates at JINR, Mikhail Gostkin, 36 HWG
- FLAME design status, Marek Idzik, 37 HWG
- Status of FPGA development at JINR Aleksandr Lapkin, 37 HWG
- Update on FLAME backend module prototype, Bartosz Dziedzic, 37 HWG
- Status of BeamCal readout design, Matias Henriquez, 37 HWG

BeamCal readout Specs

- Sapphire readout? Detector segmentation?
- ILC or CLIC signal time structure
- Number of channels
- Modes of operation
- Max input signal and gain (in mV/fC) for each mode
- Input capacitance or input cap range
- ENC for each mode of operation
- How to switch between modes of operation
- Baseline restoration requirements
- Asynchronous beam requirements
- How many bits of ADC resolution for each mode of operation
- Other features, e.g., sum of all channels
- Radiation tolerance
- Power dissipation
- Total IC count

BeamCal readout Specs...

Old specs for the readout (500 GeV center-of-mass energy ILC, classic sandwich design of BeamCal):

Input rate	3.25 MHz during 0.87 ms, repeated every 200 ms
Channels per ASIC	32
Occupancy	100%
Resolution	10 bits for individual channels, 8 bits for fast feedback
Modes of operation	Standard data taking (SDT), Detector Calibration (DCal)
Input signals	37 pC in SDT, 0.74 pC in DCal
Input capacitance	40 pF (20-pF detectors and 20-pF wires)
Additional feature	Low-latency (1 μs) output
Additional feature	Internal pulser for electronics calibration
Radiation tolerance	1 Mrad (SiO_2) total ionizing dose
Power consumption	2.19 mW per channel
Total ASIC count	2,836

We have agreed that it is better to have now simpler not perfect ASIC (only ~8-16 chan, static gain change, only analog readout,...), than wait for the final (params, technology, complex design). Mathias showed first project and sims, Angel will give the status during the workshop...

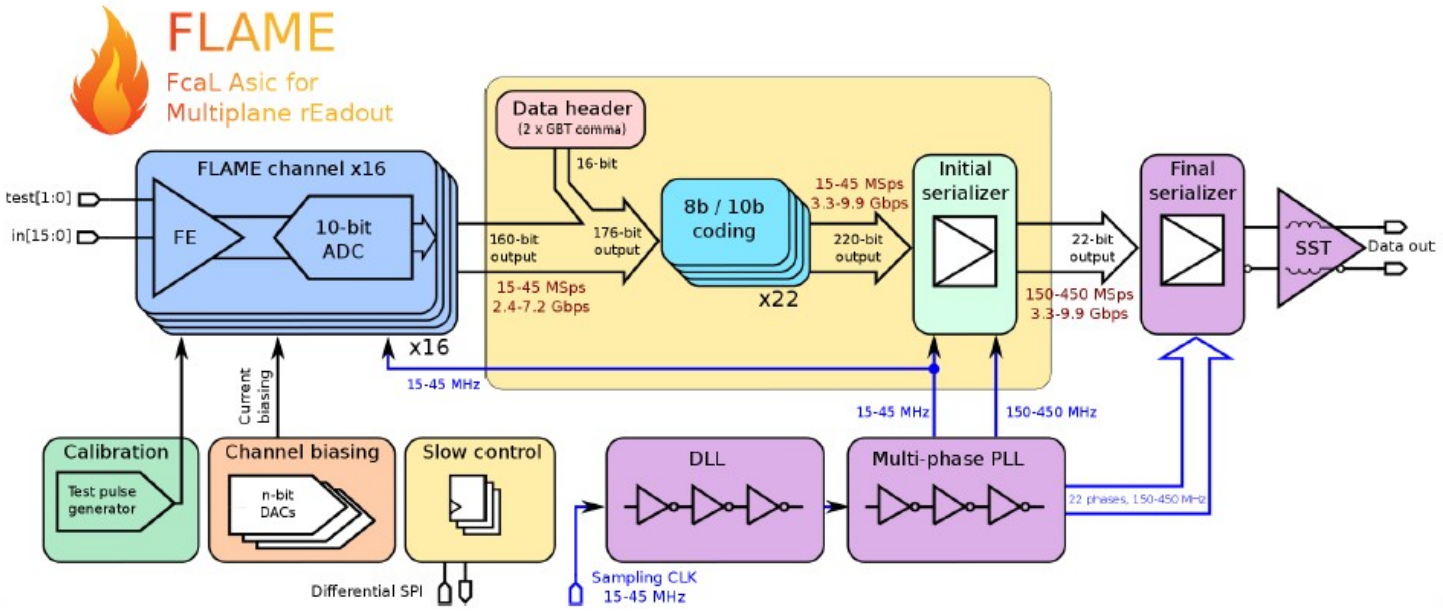
Rad-hard BeamCal sensors

- A lot of work on rad-hard sensors (GaAs, Si, Sapphire, Silicon Carbide) irradiated up to several hundred Mrads, at different temperatures, was done at UCSC and JINR
- There are many slides/results in Bruce&Uladzimir presentations (see the meeting webpage)… - in fact Collaboration suggested Bruce and Uladzimir to prepare publication(s) with these data – Bruce has already done!

In principle both GaAs and Si can be used as BeamCal sensors, although precise comparison of S/N with final readout electronics is not yet possible. For Si sensors, the cooling to negative temperatures would be needed to maintain S/N. Bruce will give the present status during the workshop...

Design of LumiCal prototype
FLAME readout ASIC

- FLAME design is in advanced stage
- Some modifications done compared to original project



Present status will be shown during the workshop (Jakub, Mirek). Submission as soon as the design is completed...

Design of LumiCal prototype
FPGA-based readout

- FLAME to FPGA GTP link almost ready
- 1Gbps link from FPGA to PC under development
- Clock domain synchronizer developed

Work on FPGA readout is progressing. Present status will be shown by Tomasz during the workshop...

Design of LumiCal prototype tungsten plates

- 10 new tungsten plates were produced by JINR
- Plates are slightly thicker than requested (~50-60um) and usually their flatness varies (on both sides) by ~30 um (for some ~100um)

The plates are of slightly worse quality than FCAL specs, but we decided to accept this 1st butch. The request is to improve it for the 2nd butch. Present status will be given by Mikhail...

Test-beams 2016 and New

- 2016 test-beam: progress on calibration and cleaning of the data taken with APV25 chip was shown by Sasha – the main issues are connected to small input range of this chip. Most of activities were shown at S&A meetings. We will see the present status during the workshop...
- New test-beam(s):
  - as discussed, the main test-beam should be done in ~mid 2019
    - AIDA2020 will be probably extended by 1 year
    - there are several months of delay in FLAME design
  - main test-beam most probably will be done with mixed readout: some planes read with APV25 and some with FLAME
  - simple (~1 layer) test-beam is proposed at ~end of 2018 to check the operation of the FLAME readout

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Thank You for Attention