BeamCal ASIC v3 Design

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Outline

- Specs – a reminder
- General readout concept
- Filter conceptual design
- Transistor-level design
- Future tasks

SPECS – A REMINDER

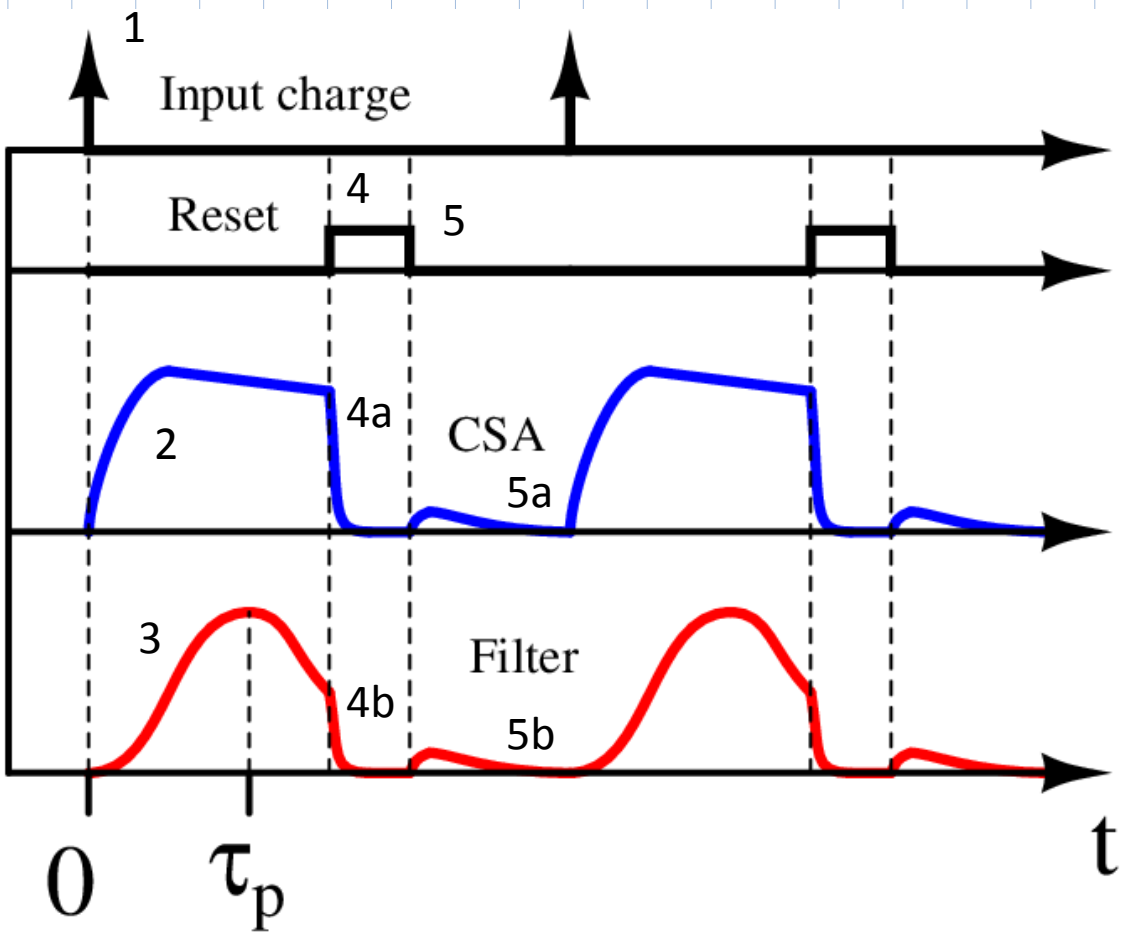
Specifications

Specification	Value
Q_{in}	> 2.8 fC
ENC	< 1000 - 1500 e^- rms
Number of channels	8
Maximum input rate	1 / 554ns
Baseline restoration	1%

- These specs are intended for **testbeam** purposes only
- Specs for **calibration** and **data taking** will be defined when the sensors are fixed
  - This ASIC will be a preliminary proof-of-concept

GENERAL READOUT CONCEPT

Timing diagram



1. CSA gets input charge
2. CSA integrates charge
3. Filter produces semi-gaussian shape
4. After peaking time, both filter and CSA are reset
   a. CSA returns to baseline instantaneously
   b. Filter returns to zero output instantaneously
5. Reset is released
   a. Noise charge is produced and decays due to CSA time constant
   b. Filtered noise charge decays before next input due to filter time constant

FILTER CONCEPTUAL DESIGN

Gm-C filters

- Suitable for VLSI
- Tunable
- Better than switched capacitors for higher bandwidth applications
- Continuous-time Gm-C filters are based on one building block: the integrator, which includes:
  - A tunable transconductor
  - A capacitor
- Direct circuit realization from block diagram

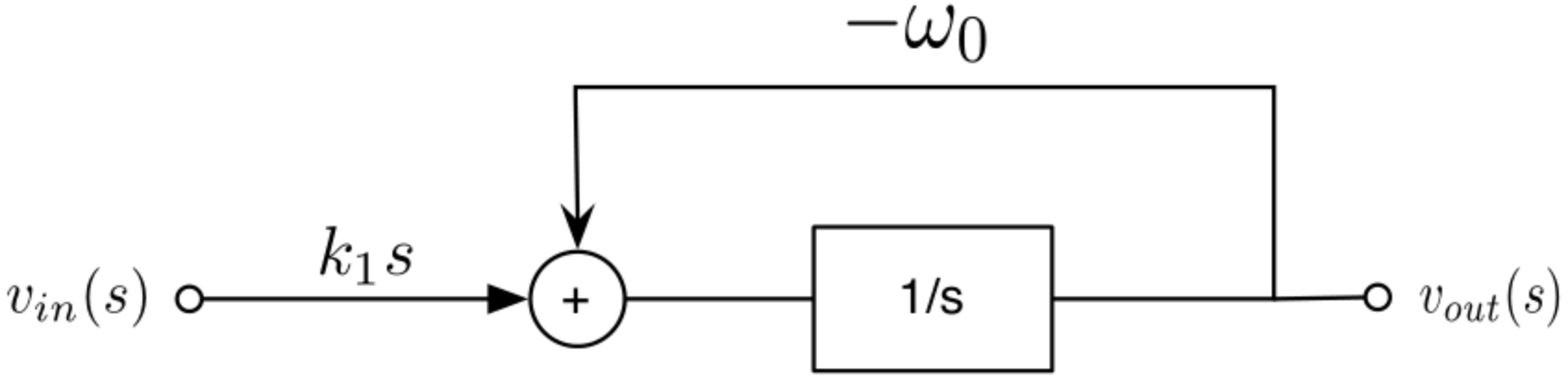
Filter implementation

- Cascade connection of:
  - Single-pole highpass filter
  - Two-pole lowpass filter
- Intended transfer function should look like this:

$$H(s) = K \cdot \frac{s\tau}{1+s\tau} \cdot \frac{1}{(1+s\tau)^2}$$

Single-pole highpass filter

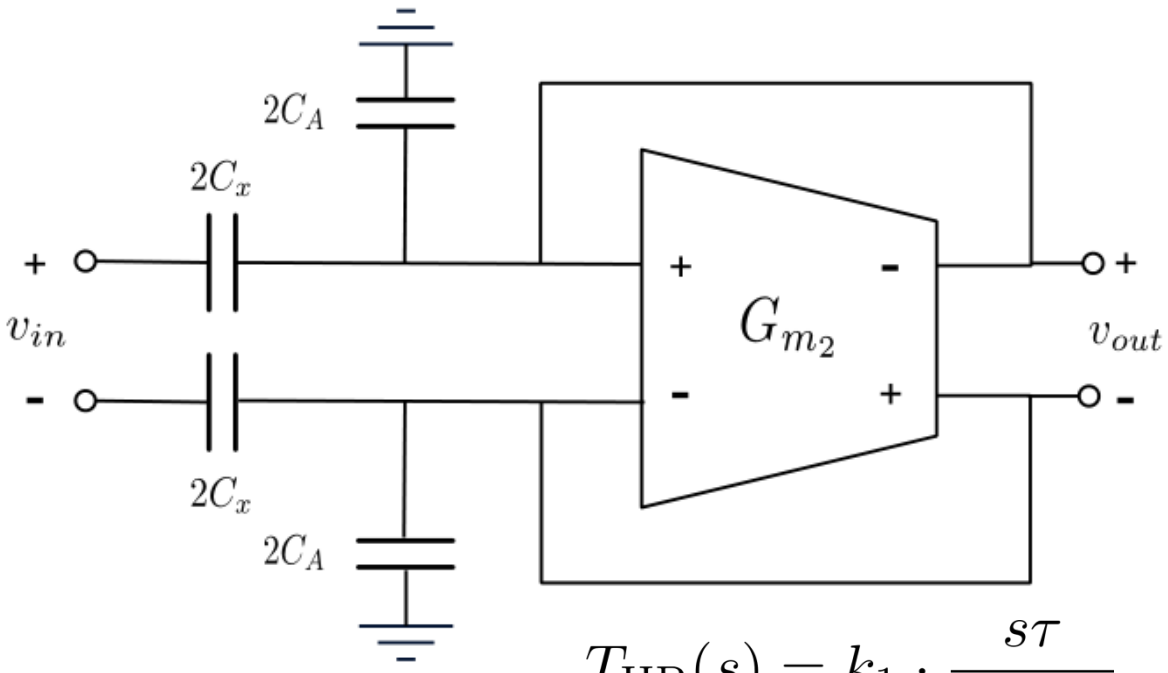
- Block diagram:



- Transfer function:

$$T_{\mathrm{HP}}(s) = k_1 \cdot \frac{s\tau}{1 + s\tau} \qquad \tau = \frac{1}{\omega_0}$$

Fully-differential Gm-C implementation of first-order bandpass filter



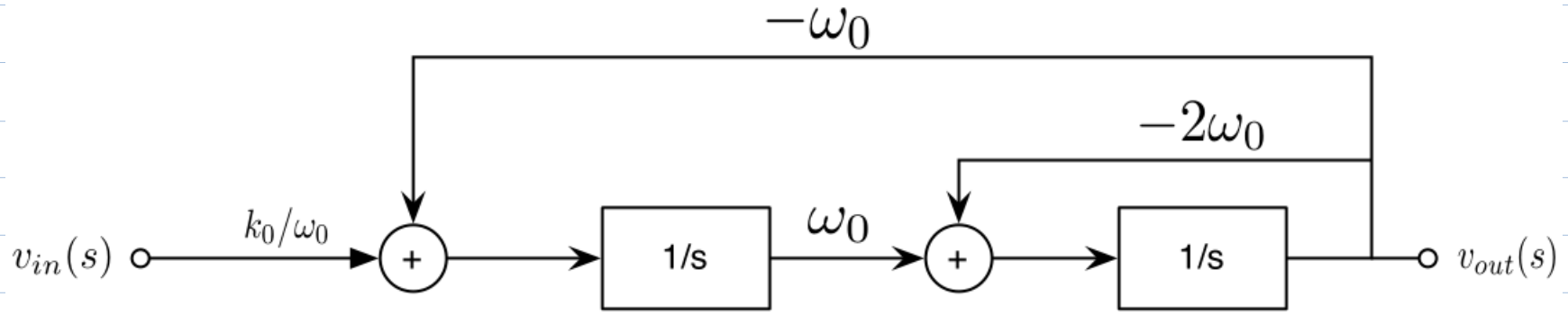
$$T_{\mathrm{HP}}(s) = k_1 \cdot \frac{s\tau}{1 + s\tau}$$

Design equations:

$$k_1 = \frac{C_x}{C_x + C_A} \qquad \tau = \frac{C_x + C_A}{G_{m2}}$$

Two-pole lowpass filter (KHN)

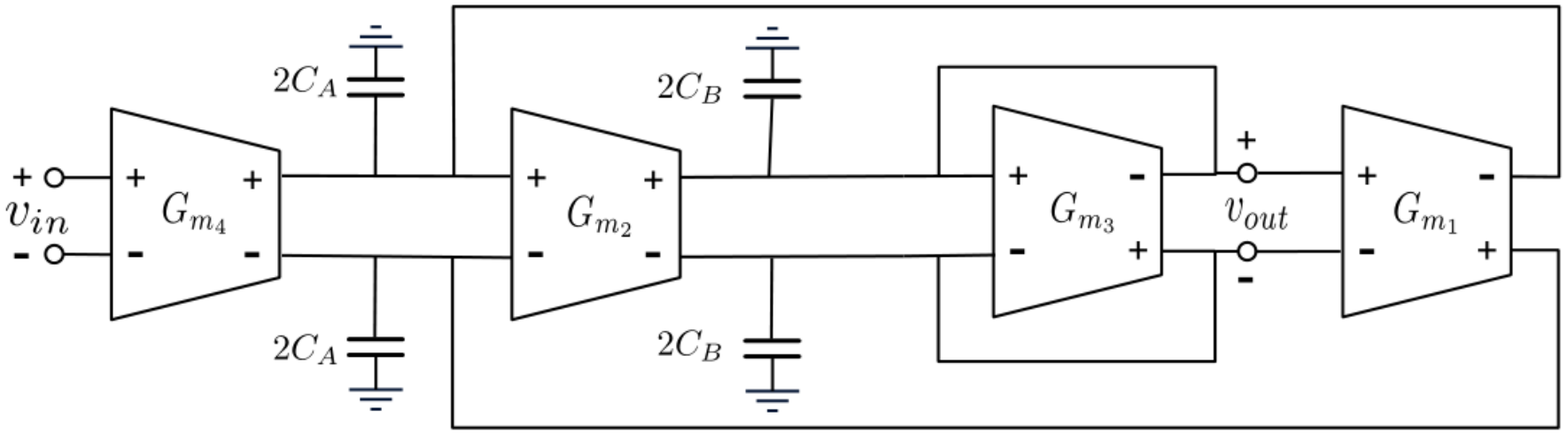
- Block diagram:



- Transfer function:

$$T_{\mathrm{LP}}(s) = \frac{k_0 \tau^2}{(1 + s\tau)^2} \qquad \tau = \frac{1}{\omega_0}$$

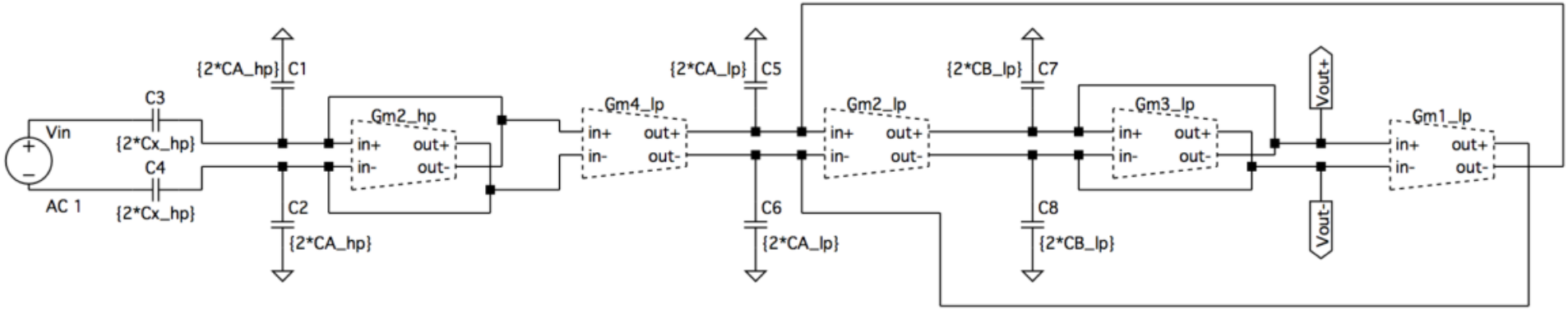
Fully-differential Gm-C implementation of second-order lowpass filter



$$T_{\mathrm{LP}}(s) = \frac{k_0 \tau^2}{(1 + s\tau)^2}$$

Design equations: $\tau^2 = \dfrac{C_A C_B}{G_{m1} G_{m2}}$ $\quad k_0 \tau^2 = \dfrac{G_{m4}}{G_{m1}}$ $\quad Q = \sqrt{\dfrac{G_{m1} G_{m2}}{G_{m3}^2} \dfrac{C_B}{C_A}} = 0.5$

Gm-C implementation of CR-RC^2 filter



$$H(s) = K \cdot \frac{s\tau}{1+s\tau} \cdot \frac{1}{(1+s\tau)^2}$$

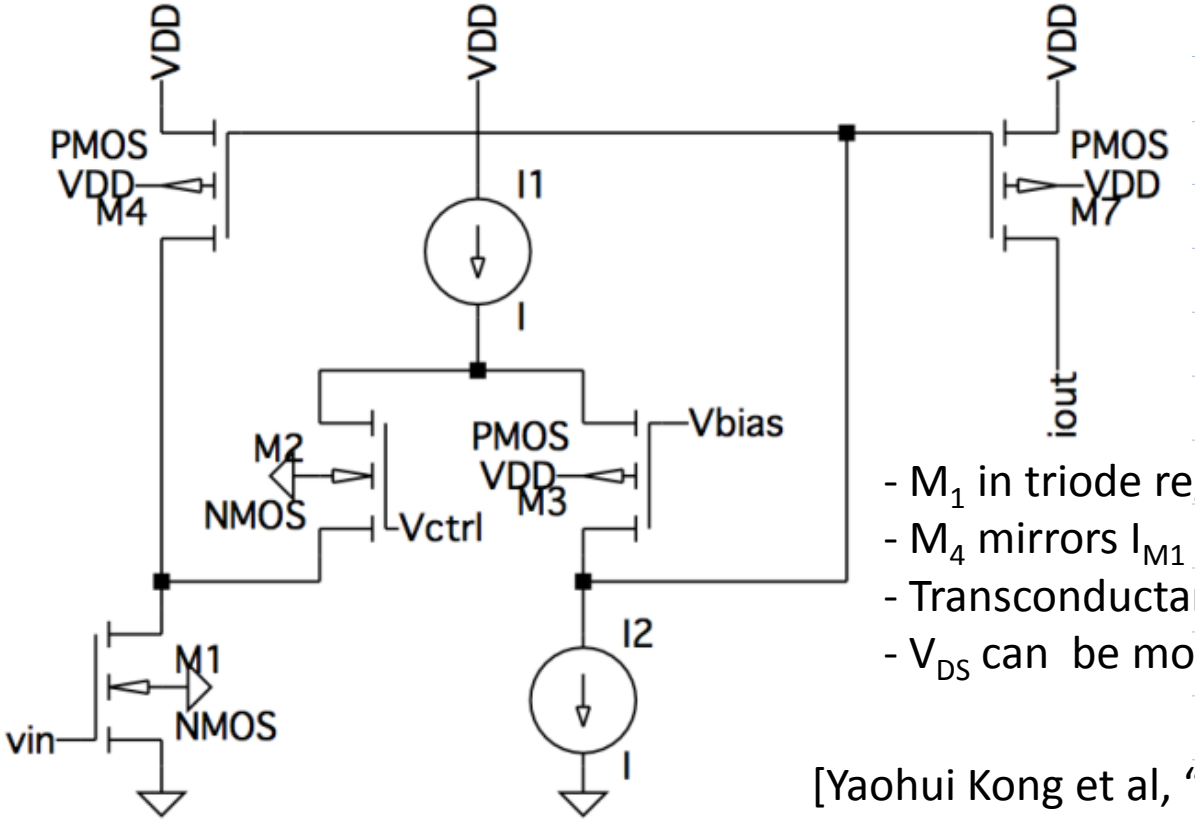
TRANSISTOR-LEVEL DESIGN

Challenges

- Constant value of G_m over the entire input range
  - Linearity
- High input range
- High output swing
- Wide tuning capabilities

Transconductor design

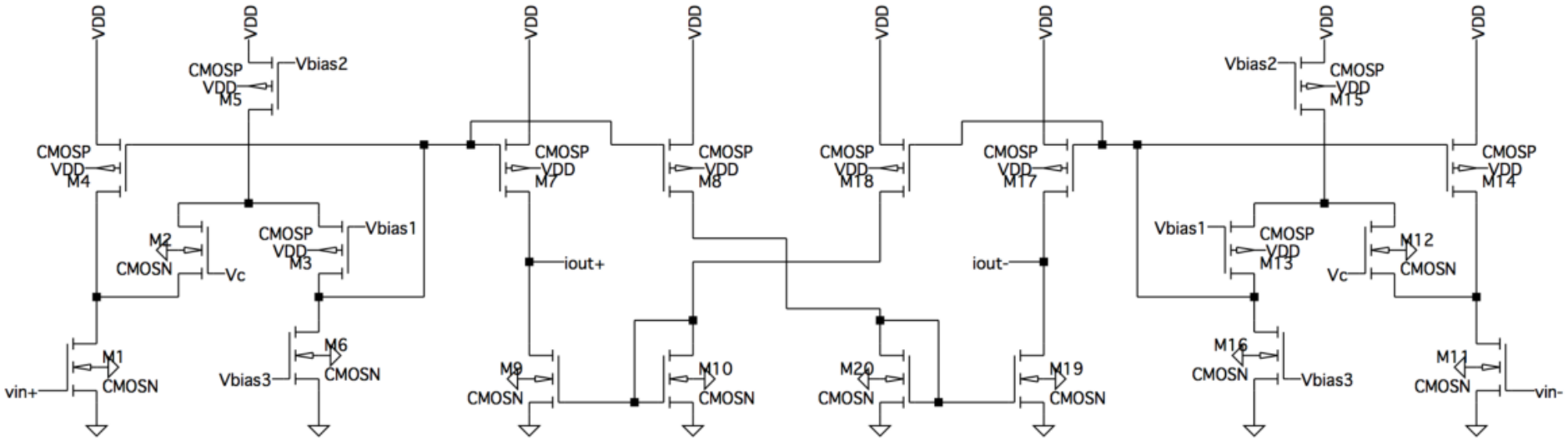
Highly linear transconductor with a wide tuning capability for low voltage and low power applications



- M_1 in triode region
- M_4 mirrors I_{M1} excess in M_7
- Transconductance is proportional to its V_{DS}
- V_{DS} can be modified by V_{ctrl}

[Yaohui Kong et al, "A highly linear low voltage CMOS triode transconductor", 2007]

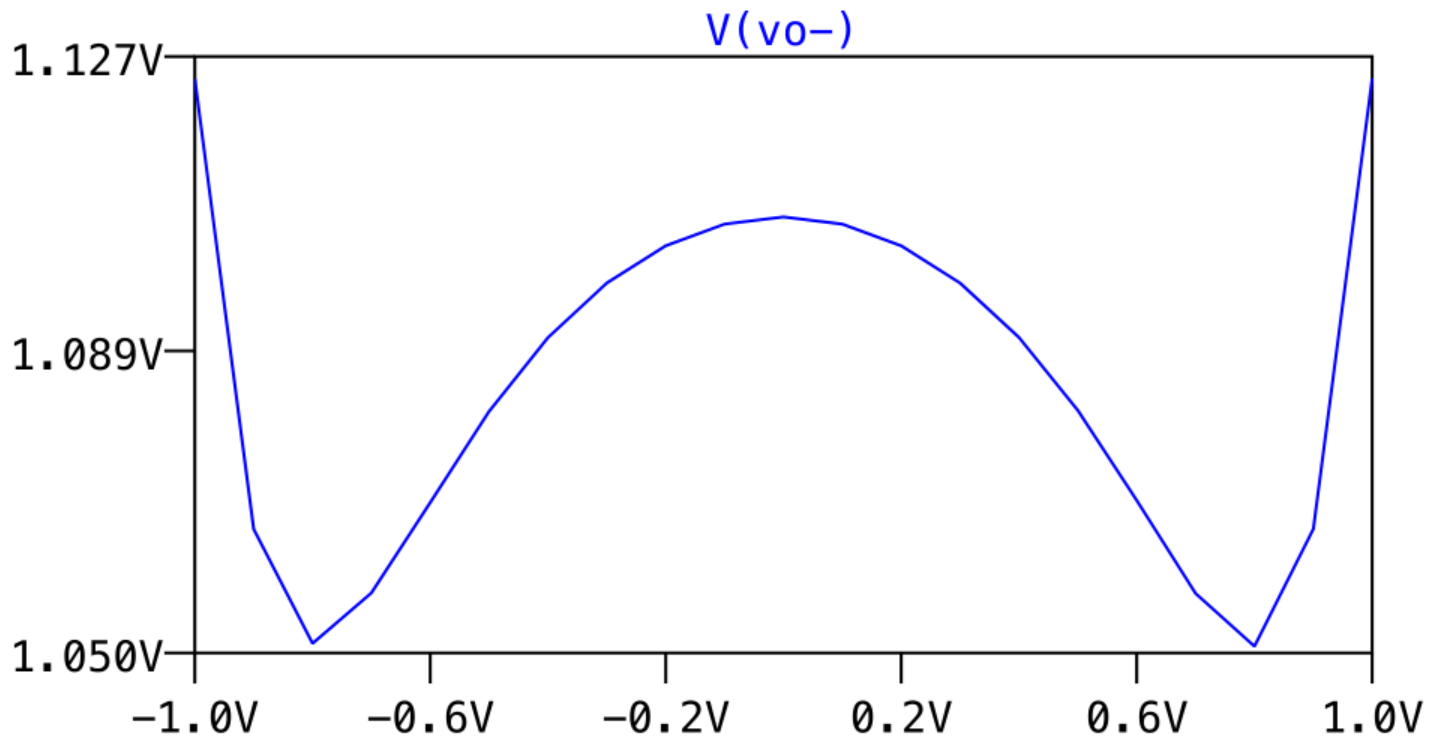
Transconductor fully-differential implementation (CMFB not shown)



The transconductance is

$$G_m = g_{m1} \cdot \frac{g_{m7}}{g_{m4}}$$

Output common-mode voltage simulation (CMFB included)



FUTURE TASKS

What's next?

- Verify filter through SPICE simulations
- Edit CSA from The Bean V1
- Edit auxiliary blocks from The Bean V1
- Complete layout
- Tape-out in September 12 2018, TSMC 180nm
- Design and test board: Sept - Nov 2018
- Get chips by mid Dec
- Test for electrical stimuli between Dec 2018 - Feb 2019

Thanks for your attention