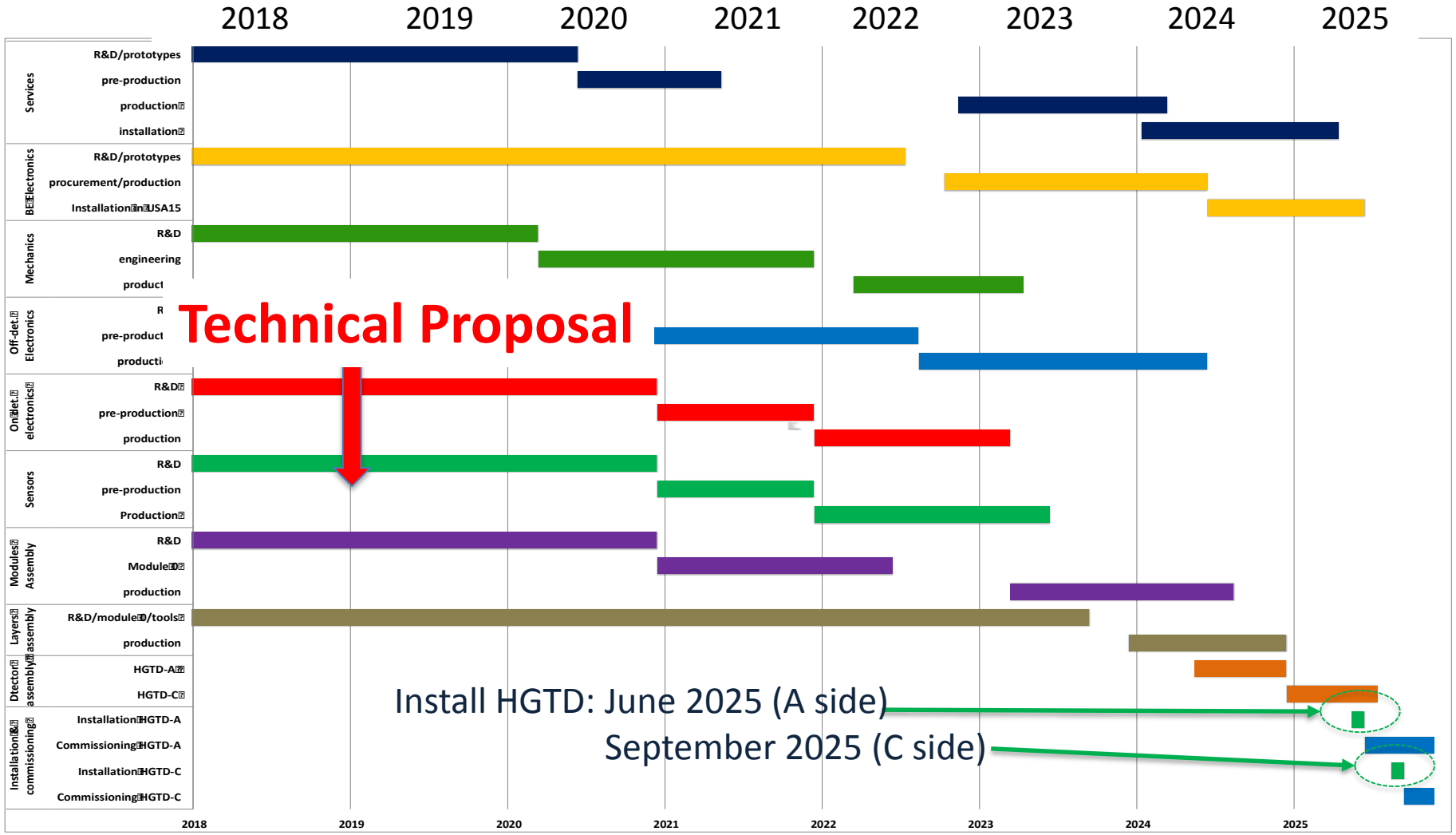
HGTD schedule (done for 4 layers/side)



- **2018-2020:** R&D
- **2021-2024:** Construction
- **2025-2027:** Integration/Installation/commissioning

More Robust schedule for optimised “2L+1” layout (~ ½ modules than in IDR)

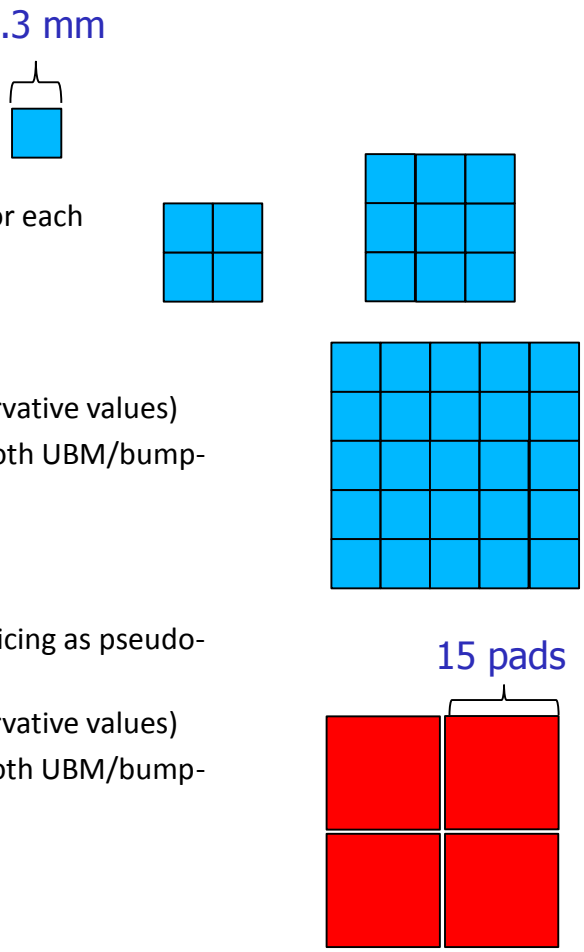
HGTD Sensor Test Overview

HGTD Sensor Development			Q1/18	Q2/18	Q3/18	Q4/18	Q1/19	Q2/19	Q3/19	Q4/19
Issue										
Geometry	Detector size	4 cm x 4 cm 25 pads (Altiroc)	HPK ATLAS/CMS CNM 6"?	HPK ATLAS/CMS CNM 6"?	HPK ATLAS/CMS CNM 6"?	HPK ATLAS/CMS CNM 6"?	ATLAS HGTD Proto	ATLAS HGTD Proto	ATLAS HGTD Proto	ATLAS HGTD Proto
	Edge region		HPK Tech 1	HPK Tech 1	HPK Tech 2	HPK Tech 2				
	Inter-pad distance	50-100um	CNM Ga 4"	CNM Ga 4"	CNM AIDA 2020	CNM AIDA 2020				ATLAS HGTD Proto
	Thickness		FBK tech	FBK	FBK	FBK				
Radiatio Hardness										
	Voltage Reach		HPK Tech 1	HPK Tech 1	HPK Tech 2	HPK Tech 2	HPK Tech 2	HPK Tech 2	HPK Tech 2	
	Shallow Implant		CNM Ga 4"	CNM Ga 4"	CNM Ga 4"	CNM Ga 4"	CNM Ga 4"	CNM Ga 4"	CNM Ga 4"	ATLAS HGTD Proto
	Accptor Removal		CNM AIDA 2020	CNM AIDA 2020	CNM AIDA 2020	CNM AIDA 2020	CNM AIDA 2020	CNM AIDA 2020	CNM AIDA 2020	
	B & Ga & C		FBK tech	FBK tech	FBK tech	FBK tech	FBK tech	FBK tech	FBK tech	
Bias Voltage										
	Long-term HV operation			HPK Tech 1	HPK Tech 1	HPK Tech 2	HPK Tech 2	HPK Tech 2	HPK Tech 2	ATLAS HGTD Proto
	Power Cycling			CNM Ga 4"	CNM Ga 4"	CNM AIDA 2020	CNM AIDA 2020	CNM AIDA 2020	CNM AIDA 2020	
Q/A										
	Yield									
	Uniformity: Gain, Break-down,					HPK ATLAS/CMS	HPK ATLAS/CMS	HPK ATLAS/CMS	HPK ATLAS/CMS	ATLAS HGTD Proto
	Rad hardness					CNM 6"?	CNM 6"?	CNM 6"?	CNM 6"?	

Legend		Fabrication				**Funding**				
		Testing								
	HPK ATLAS/CMS	ATLAS/CMS Common run at HPK				50-50 ATLAS-CMS				
	CNM 6"	6" run at CNM								
	ATLAS HGTD Proto	ATLAS pre-production Proto-type		Final size sensors						
	HPK Tech 1	HPK technology run #1				HPK				
	HPK Tech 2	HPK technology run #2 if needed				HPK ?				
	FBK Tech	Technology run at FBK: Ga, C, etc								
	CNM Ga 4"	Technology Run at CNM (RD50)		50um, like #10478						
	CNM AIDA 2020	Technology Run at CNM		35&50um, 5x5 arrays AltiRoC						

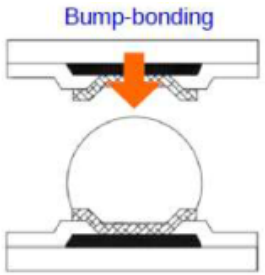
HGTD Sensor Wishlist

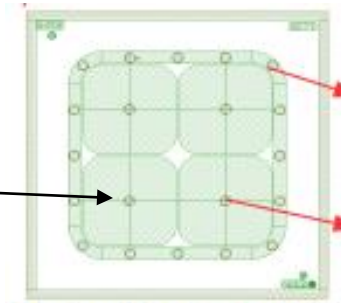
- Wafer active thickness: 50 µm (baseline) and 35 µm (option)
- Pad size always 1.3x1.3 mm²
- Structures (LGAD if not noted otherwise)
  - LGAD single pad, PIN single pad
  - Arrays of 2x2 and 3x3 pads
    - Inter-pad gap variations: 30, 50, 70 µm? (CNM standard 64 µm physical)
    - Slim edge variations: 100, 200, 300 µm? -> optimized edge design (GR etc.) for each
    - Large passivation openings for wire-bonding/probe needles
  - Arrays of 5x5 pads
    - Compatible to next version of HGTD readout chip (ALTIROC1, mid 2018)
    - Standard inter-pad gap (50-100 µm) and standard edge (300-500 µm) (conservative values)
    - 2 different passivation openings or alternatively biasing structures to allow both UBM/bump-bonding and probing/wirebonding
  - Large arrays of 15x15 pads (single-chips) and 30x15 pads (double-chips)
    - Compatible to final HGTD readout chip (~2019)
    - Designed as single-chip sensors, but arranged to allow yield-evaluation and dicing as pseudo-doubles and quads for module proto-typing
    - Standard inter-pad gap (50-100 µm) and standard edge (300-500 µm) (conservative values)
    - 2 different passivation openings or alternatively biasing structures to allow both UBM/bump-bonding and probing/wirebonding

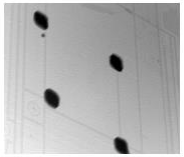


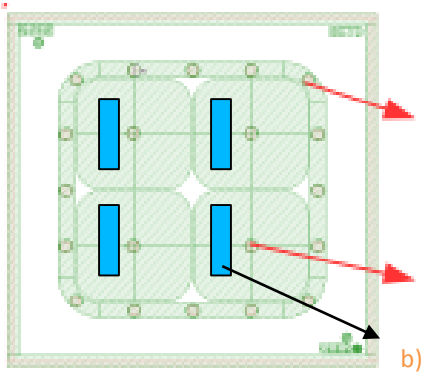
Bump-Bonding

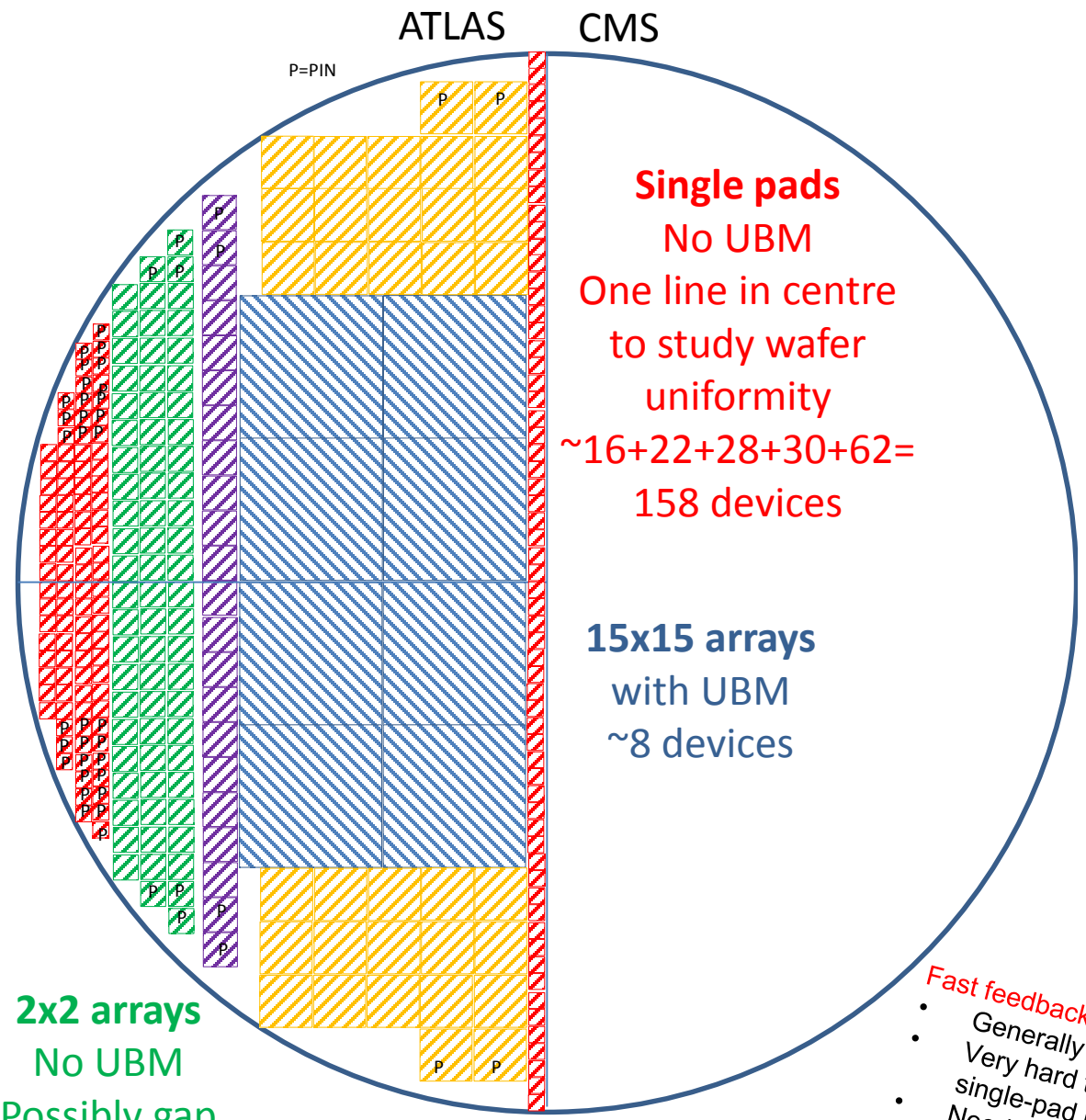
- Need to bump-bond sensor to readout chip
- Need Under-Bump-Metalisation (UBM)
  - Provided by vendor?
  - Which process? Is a mask used to protect other metal not foreseen for UBM?
    - Do structures for UBM need to be on one part of the wafer?
- HGTD bump-bonding tests so far
  - On CNM HGTD run (2x2 arrays for first version of readout chip: ALTIROC0)
  - Passivation opening of 90 µm diameters
  - Electro-less UBM in house by CNM
  - Bump-deposition of 80 µm diameter bumps and flip-chipping
  - Good results: hybrid works and delivers signal; good mechanical stability
- How do we assure probing (IV) and sensor selection on wafer?
  - Several options possible
    1. Implement 2 passivation openings on same pad: both small opening for UBM and large opening for probing/wire-bonding
       -> allows to probe IV of large sensors with probe card
    2. Temporary metal to shorten all pads
    3. Biasing structures like for pixels (e.g. punch-through or poly-Si)











6 inch LGAD wafer layout proposal (sketch)

- Shared between ATLAS/CMS (half-half)
- ATLAS pad: 1.3x1.3 mm² active area
- Some PINs for each structure
- Here not completely closely packed/well aligned (just a sketch) and each sensor has conservative 500 µm inactive width at each edge (incl. GR, margin, cut line) -> slightly higher density possible
- Typically arrays have safe standard inter-pad gap of ~50-100 µm (tbd)
- 2x2 arrays can have variations
  - Gap of e.g. 30, 50, 70 µm to optimise fill factor
  - Slim edge (100, 200, 300 µm)
- Large sensors (5x5, 15x15)
  - UBM (90 µm passivation hole in centre)
  - Additional structures for probing (larger openings for needles/wire bonds, maybe biasing structure)
  - 8 15x15 single-chip sensors
    - Designed as single-chip sensors, but arranged to allow yield-evaluation and dicing as pseudo-doubles and quads for module proto-typing

Fast feedback by CNM

- Generally no showstopper
- Very hard to dice (e.g. central single-pad line "impossible")
- Need space for test structures/alignment marks
- Need ALTIROC top-layer for UBM