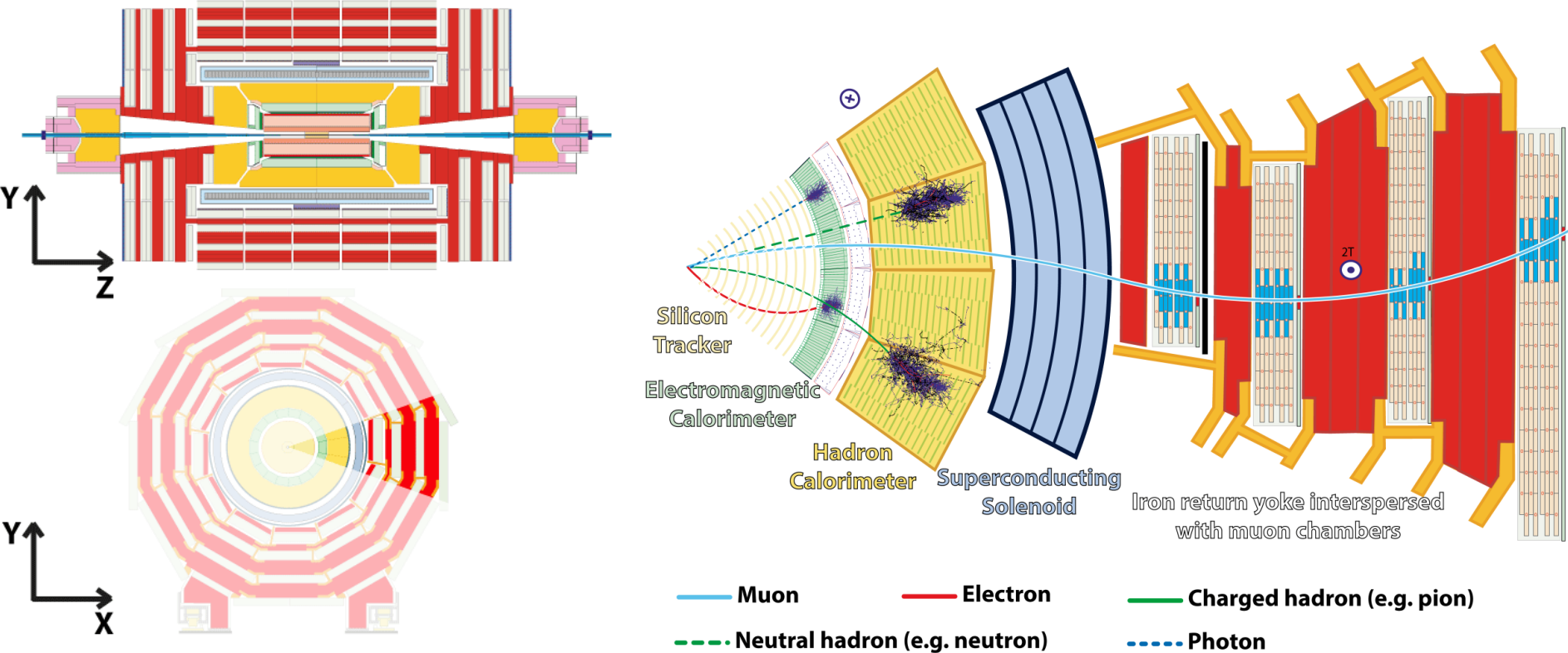


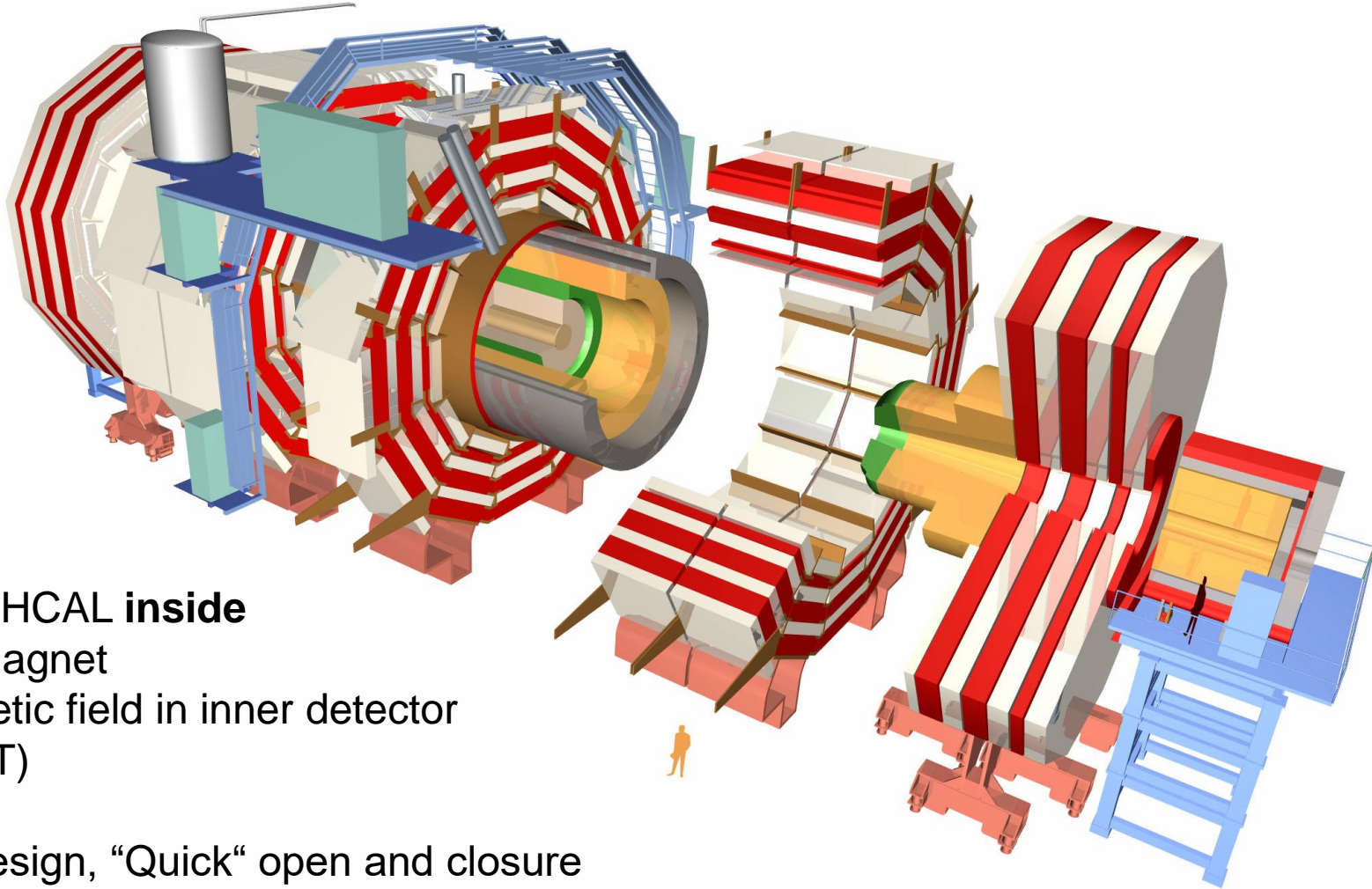
Design, construction, and performance of the new CMS pixel detector:
conceptual differences to ATLAS pixels on micro- and macroscopic level

Malte Backhaus

CMS Experiment

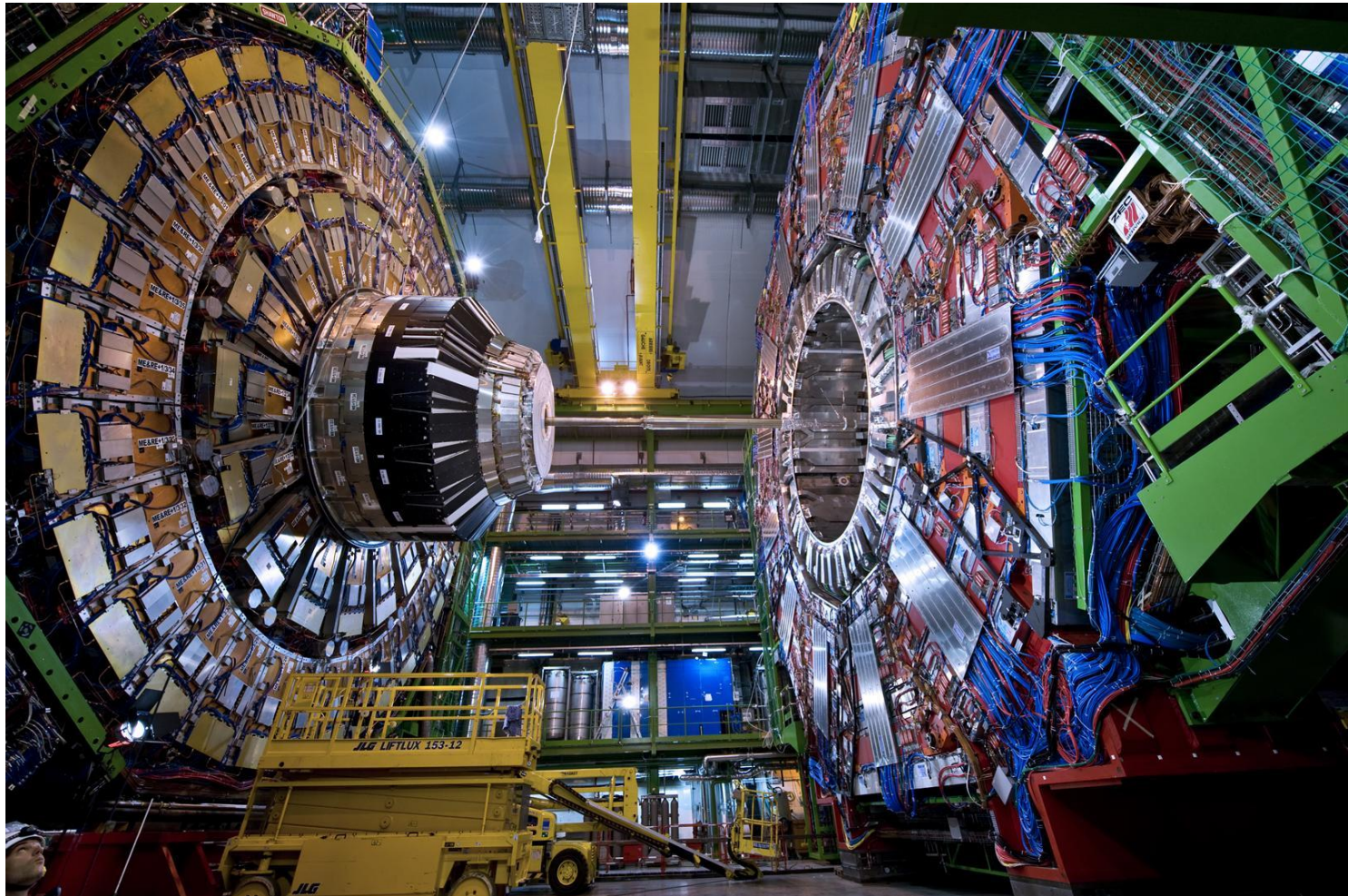


CMS Experiment

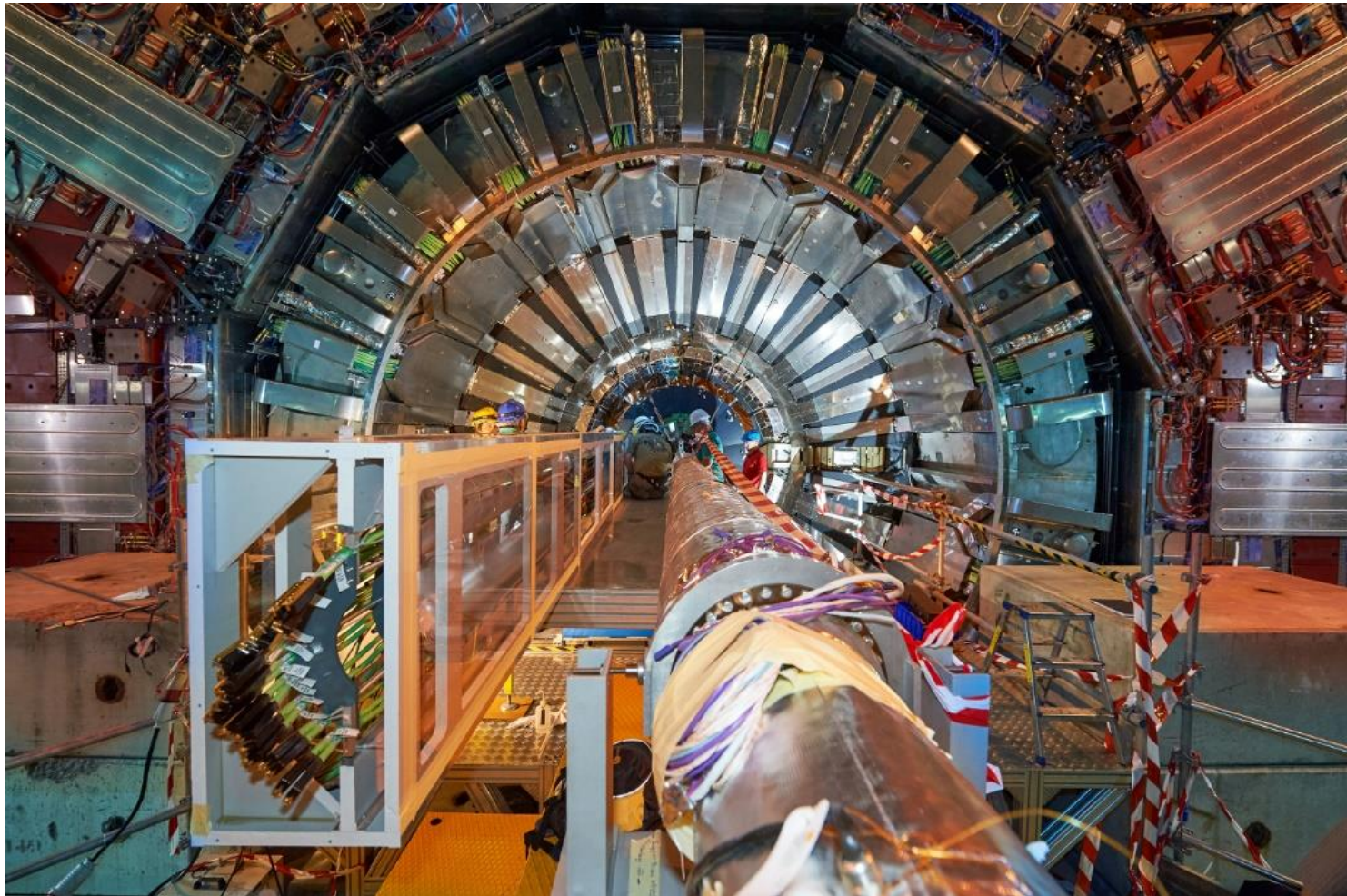


- ECAL and HCAL **inside** solenoid magnet
- ~4T magnetic field in inner detector (ATLAS: 2T)
- Modular design, “Quick” open and closure
- Access to components within ~14 days (ATLAS: ~6 months)

CMS Experiment



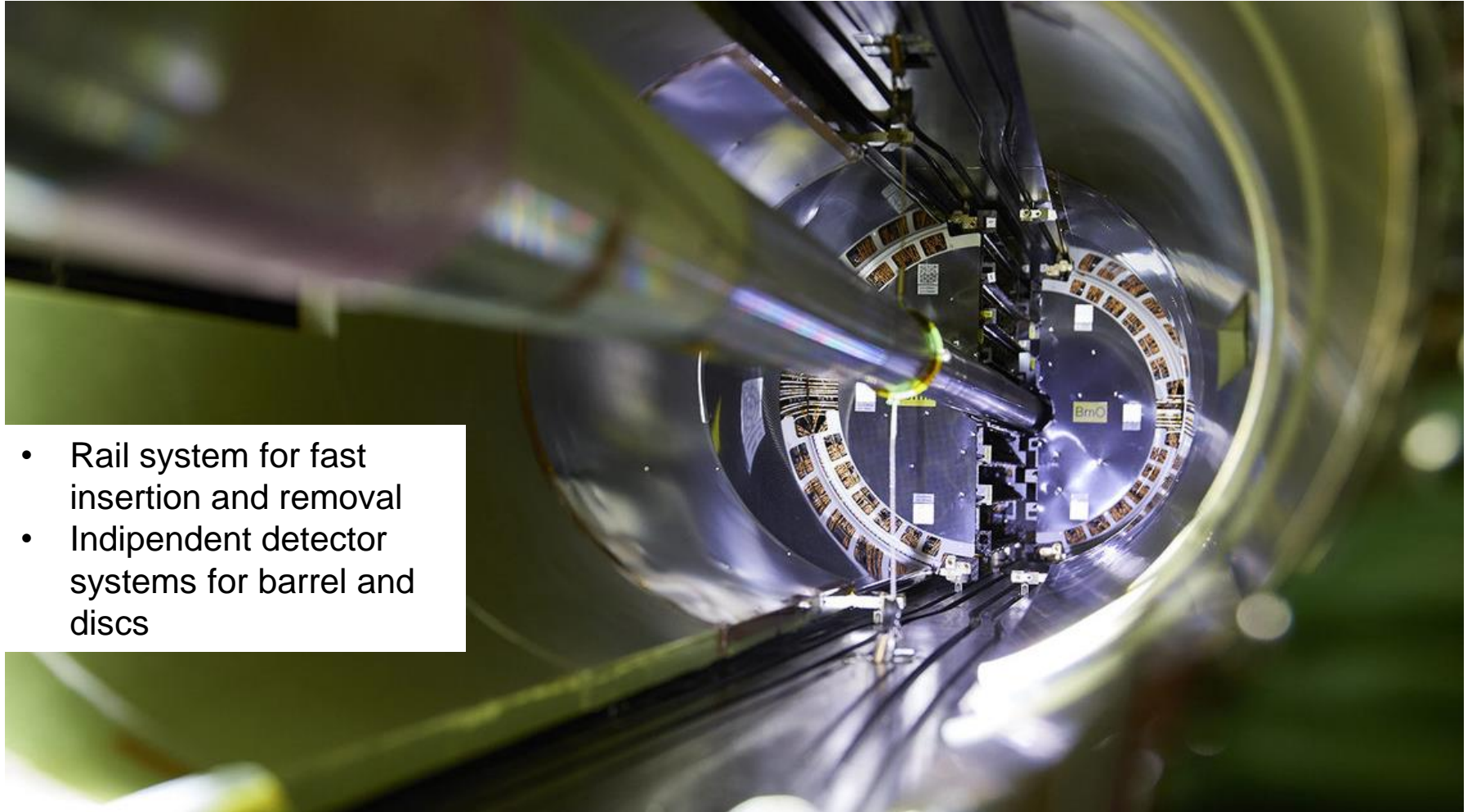
Insertion of CMS Pixel Detector: 2008



Insertion of new CMS Pixel Detector: 2017



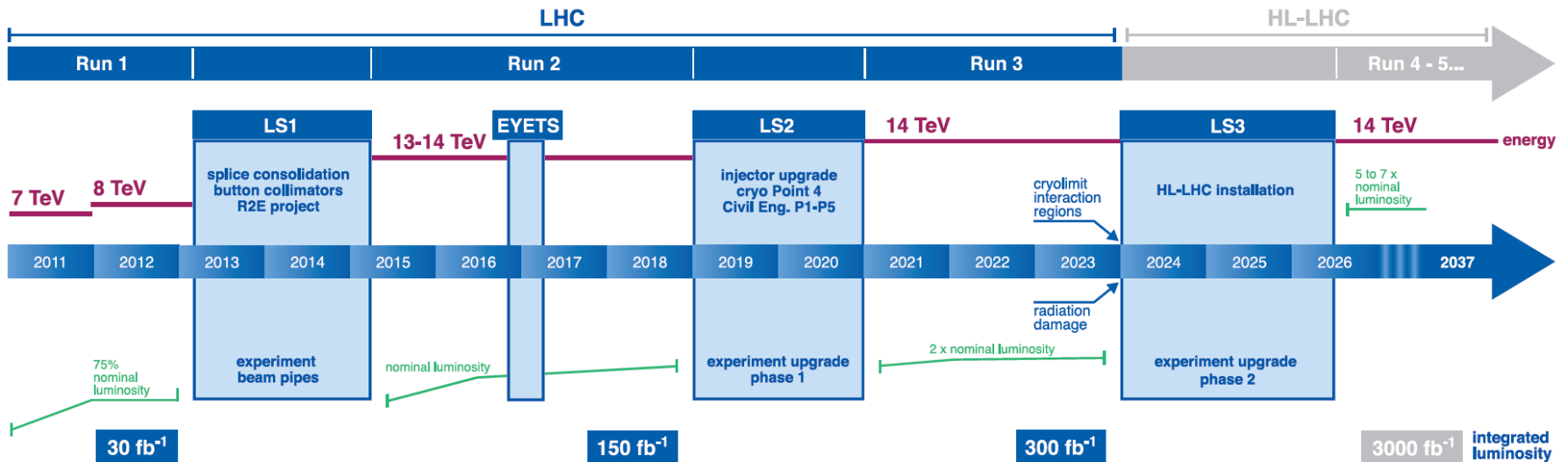
Insertion of new CMS Pixel Detector: 2017



- Rail system for fast insertion and removal
- Independent detector systems for barrel and discs

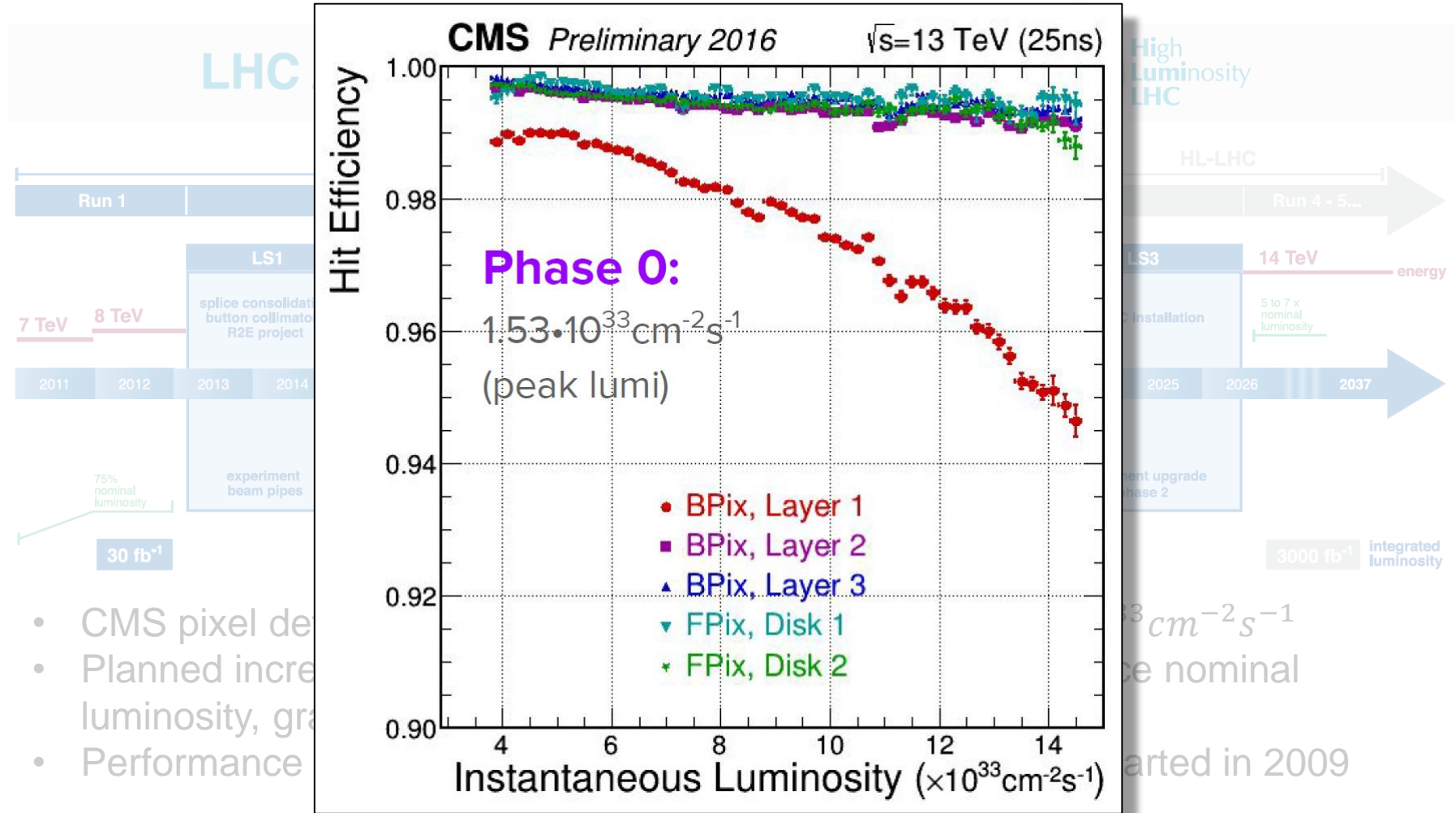
Motivation for CMS Phase-I Pixels

LHC / HL-LHC Plan



- CMS pixel detector designed for peak luminosity of $10 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$
- Planned increase of luminosity after Long Shutdown 2 to twice nominal luminosity, gradual increase before LS2.
- Performance degradation anticipated, replacement project started in 2009

Motivation for CMS Phase-I Pixels

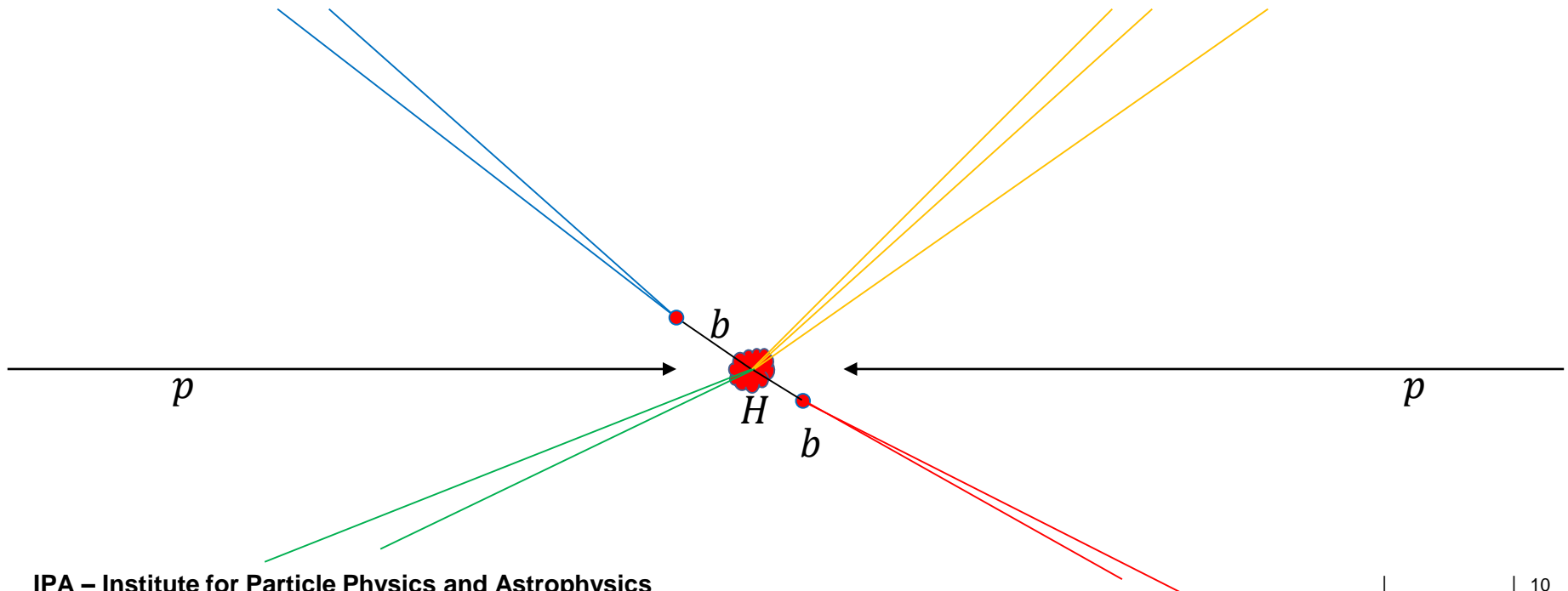


- CMS pixel de
- Planned incre
- luminosity, gra
- Performance

3 cm⁻²s⁻¹
 ce nominal
 arted in 2009

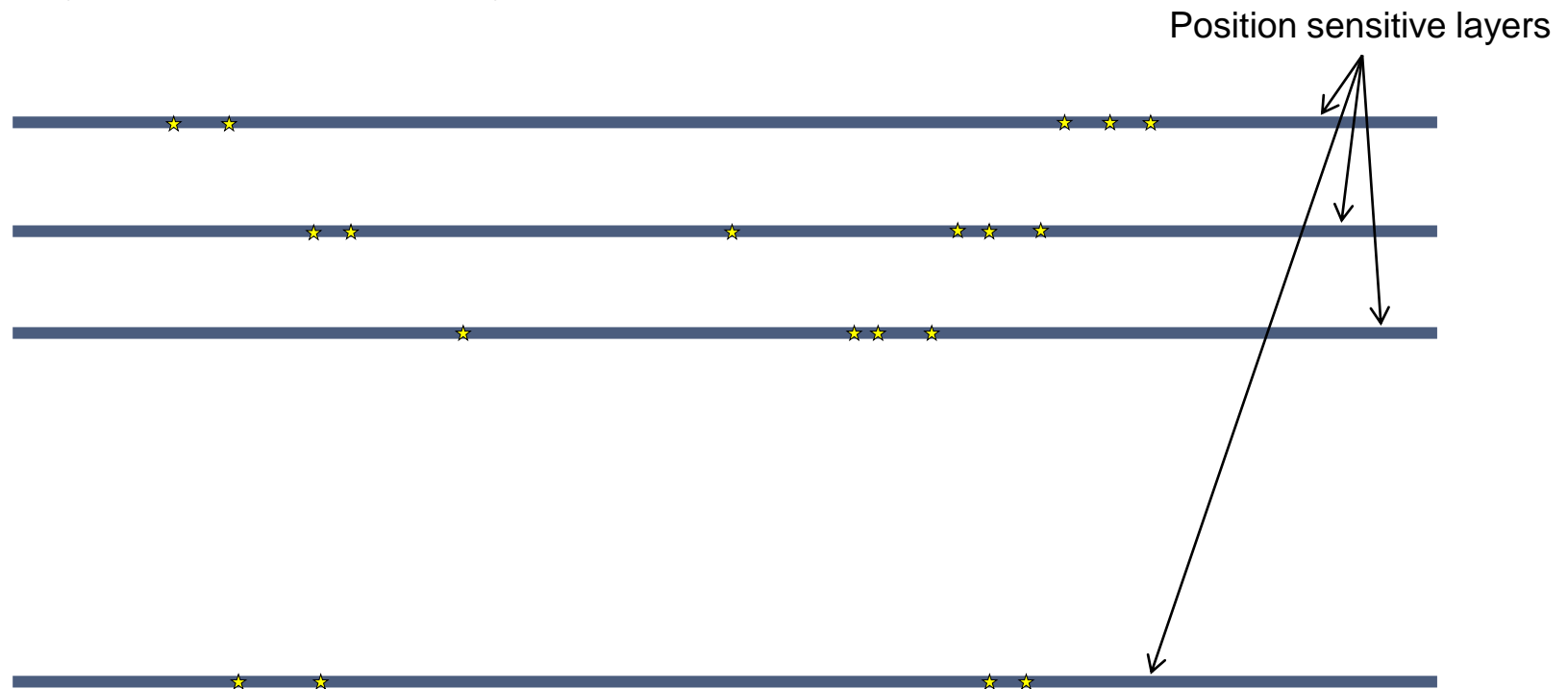
Secondary Vertex Identification

- Events with long lived hadrons (containing b -quarks and c -quarks) and τ -leptons are particularly interesting ($H \rightarrow b\bar{b}$, $H \rightarrow \tau\tau$, $t \rightarrow bW^\pm$, ...)
- Decay in displaced *secondary vertices*



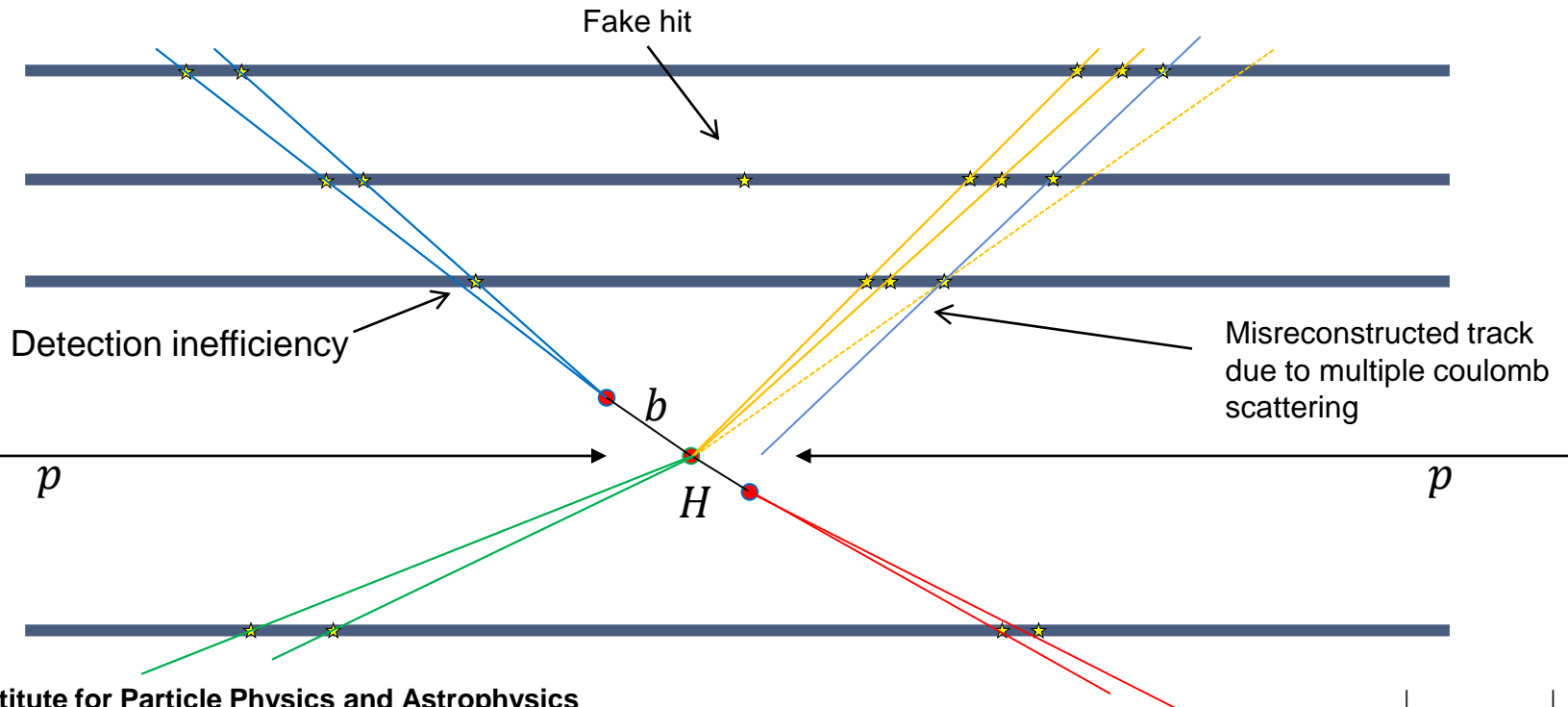
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Secondary Vertex Identification

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Requirements

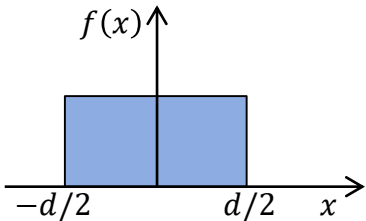
- High detection efficiency
+ additional layer for tracking robustness
- Low fake-hit rate
- Low material
- High vertex resolution...

Simplified Vertex Resolution

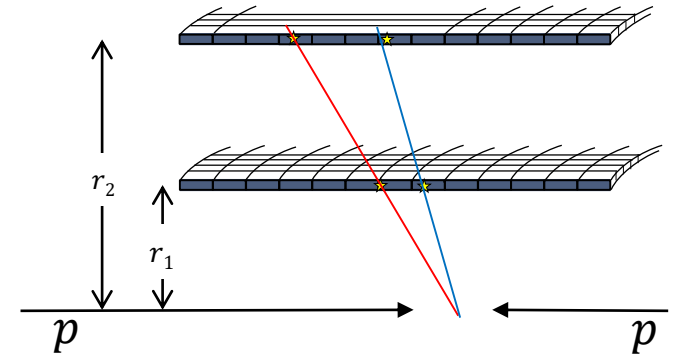
Major vertex resolution dependencies \rightarrow Simplified model:

- Two layers of 2D segmented detectors at r_1 and r_2
- Similar segmentation width d
- Full efficiency, no detection threshold

Spatial resolution:



$$\Rightarrow \sigma = \frac{d}{\sqrt{12}}$$

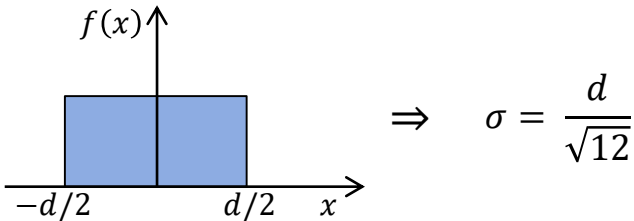


Simplified Vertex Resolution

Major vertex resolution dependencies → Simplified model:

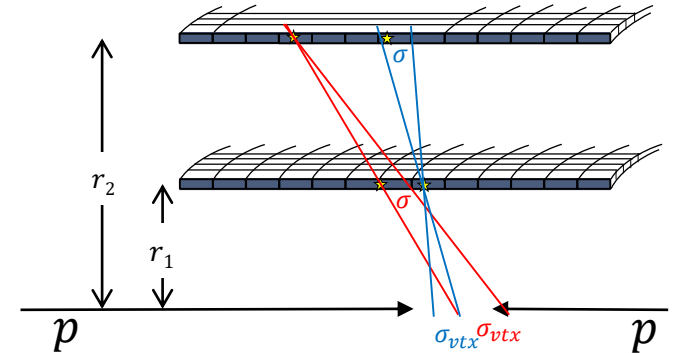
- Two layers of 2D segmented detectors at r_1 and r_2
- Similar segmentation width d
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Spatial resolution:



Vertex Extrapolation:

$$\sigma_{vtx} = \sigma_{vtx} \oplus \sigma_{vtx} \cong \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 \cdot \left(1 + \frac{r_1^2}{(r_2 - r_1)^2}\right)}$$



$$\sigma_{vtx} = \frac{r_2}{r_2 - r_1} \sigma$$

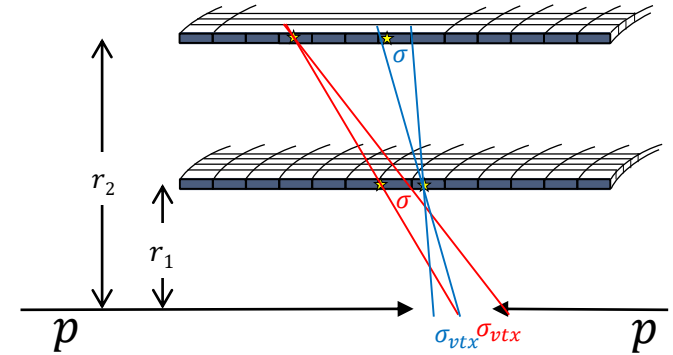
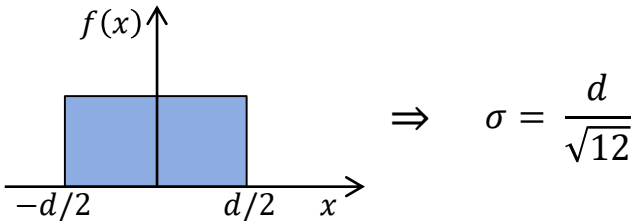
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Simplified Vertex Resolution

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- Two layers of 2D segmented detectors at r_1 and r_2
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Vertex Extrapolation:

add MS



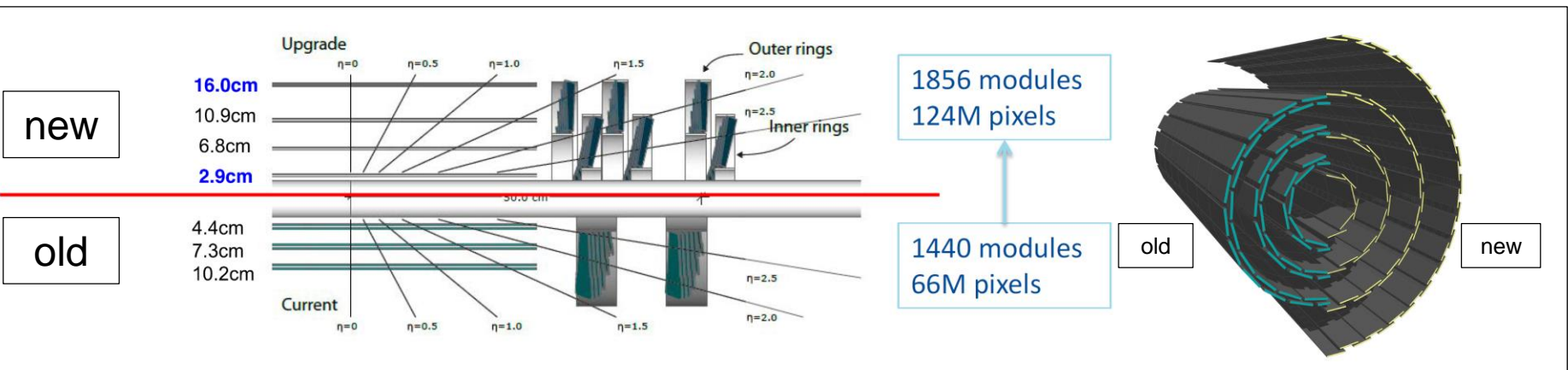
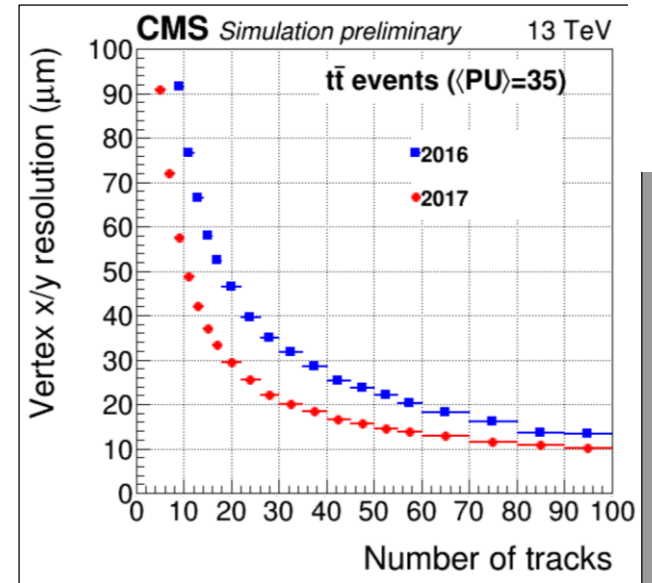
$$\sigma_{vtx} = \sigma_{vtx} \oplus \sigma_{vtx} \cong \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 \cdot \left(1 + \frac{r_1^2}{(r_2 - r_1)^2}\right)} \cong \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 \cdot \left(1 + \frac{r_1^2}{(r_2 - r_1)^2}\right) + (2r_1 - r_0)^2 \cdot \left(\frac{13.6 \text{ MeV}}{pv}\right)^2 \frac{l}{X_0}}$$

Requirements

- High detection efficiency
+ additional layer for tracking robustness
- Low fake-hit rate
- Low material
- High vertex resolution...
 - High spatial resolution
 - Small distance to interaction point
 - Large lever arm

Requirements

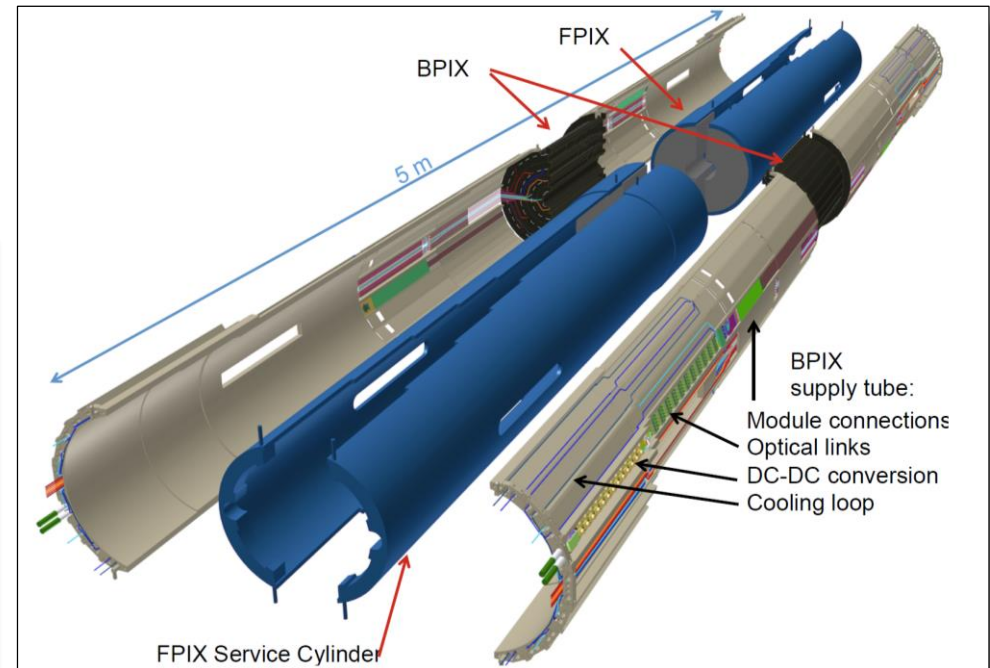
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Requirements

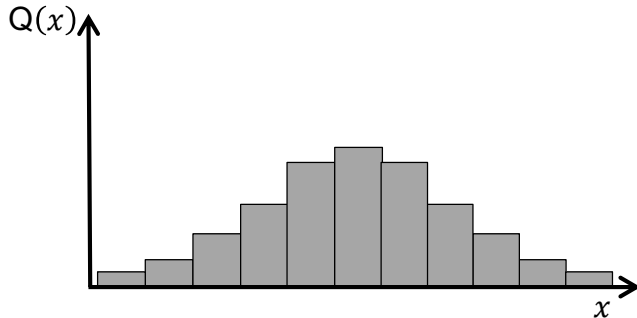
- High detection efficiency
+ additional layer for tracking robustness
- Low fake-hit rate
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- High vertex resolution...
 - High spatial resolution
 - Small distance to interaction point
 - Large lever arm

- DC-DC power system
→ four layers without service material increase
- CO₂ bi-phase cooling
- Lightweight carbon support ladders / rings
- Service components placement at larger z



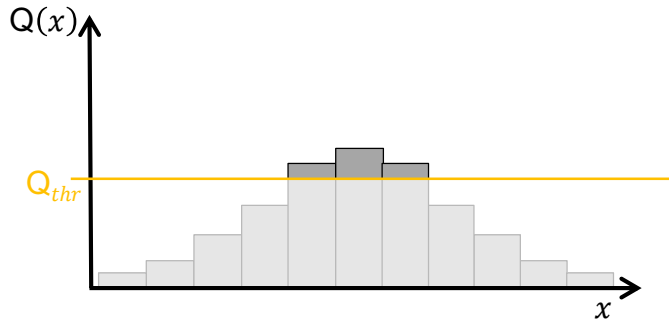
Towards high spatial resolution – ATLAS IBL

- Small segmentation pitch improves resolution: $\sigma = \frac{d}{\sqrt{12}}$
- ATLAS IBL: $50 \mu m$ $r\phi$ resolution $\rightarrow \sigma = 15 \mu m$
- Analog charge information \rightarrow charge weighting \rightarrow improved resolution



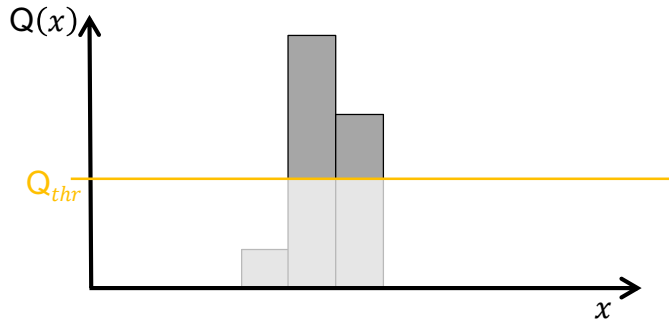
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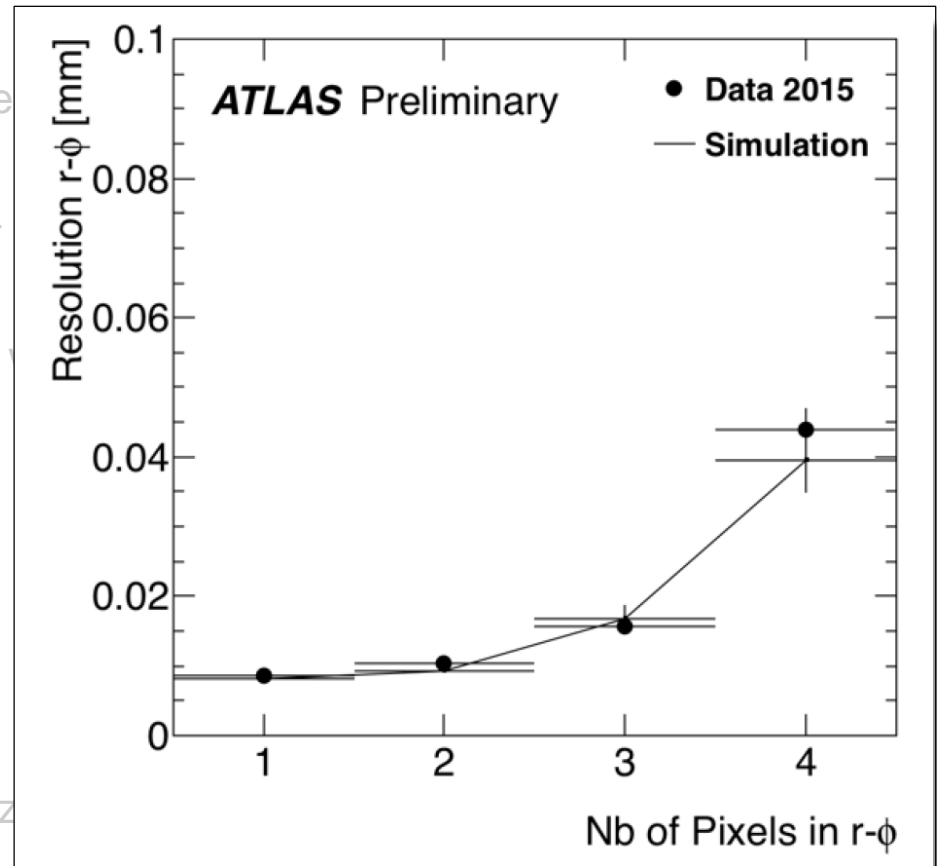
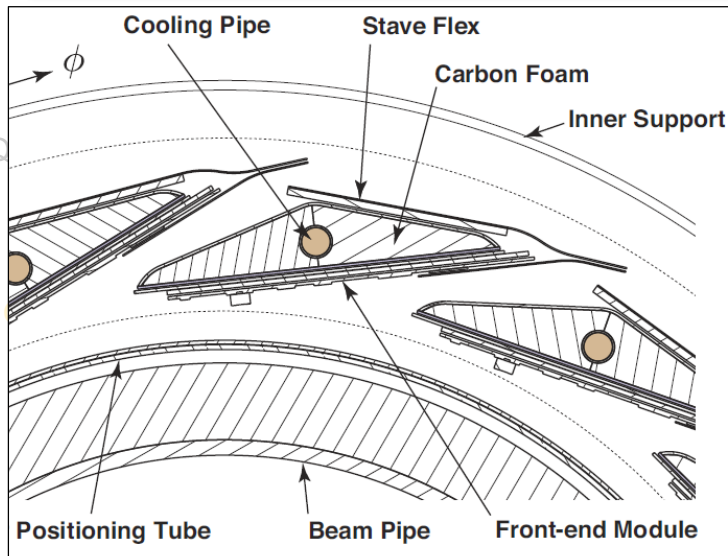
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- Design system for 2-3 pixel cluster size

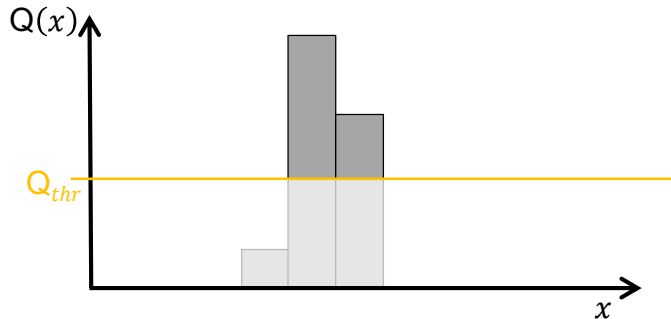
Towards high spatial resolution – ATLAS IBL

- Tilt of staves by 14°
→ 2-3 hit cluster size due to incident angle
- Resolution improvement:
 $15\ \mu\text{m} \rightarrow \sim 9\ \mu\text{m}$



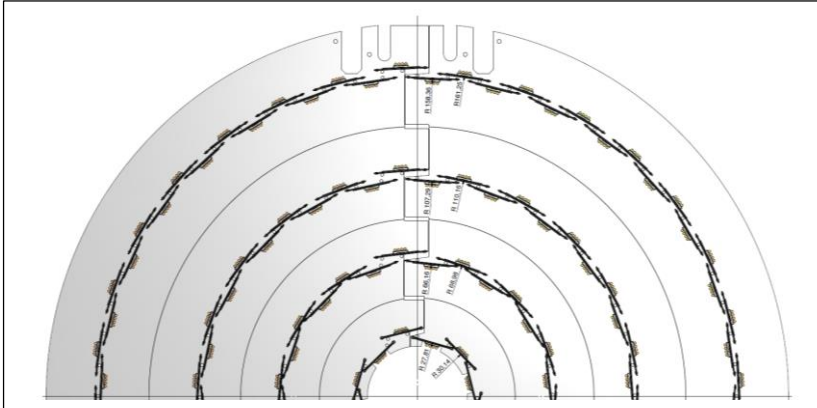
Towards high spatial resolution – CMS Pixel

- Small segmentation pitch improves resolution: $\sigma = \frac{d}{\sqrt{12}}$
- CMS pixel: **100 μm** $r\phi$ resolution \rightarrow **$\sigma = 30 \mu\text{m}$**
- Analog charge information \rightarrow charge weighting \rightarrow improved resolution



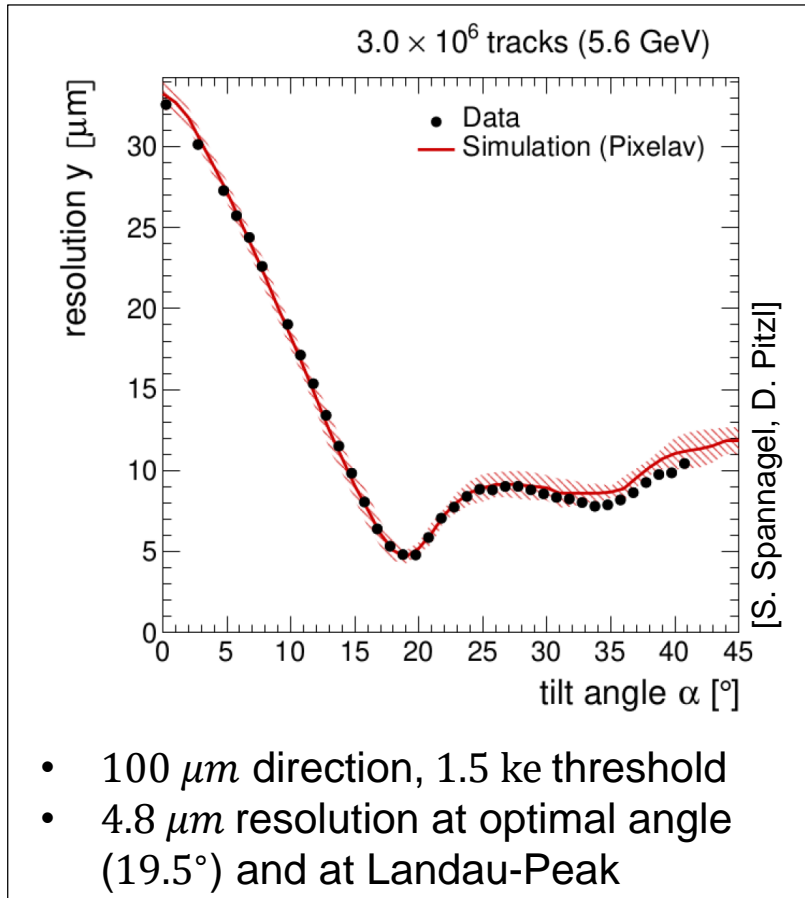
- Design system for 2-3 pixel cluster size

Towards high spatial resolution – CMS Pixel



- No tilt of ladders
→ orthogonal incident angle
- Use strong magnetic field in CMS
→ Charge drift in Lorentz angle (21°)
→ 2-3 hit cluster size
- Massive resolution improvement if charge resolution is good ($100 \mu\text{m}$ pixel pitch)
→ Analog pixel cell readout
→ 8bit ADC
- Sensor thickness chosen for optimal cluster size
→ $285 \mu\text{m}$ active thickness
→ Expected performance decrease after type inversion / partial depletion

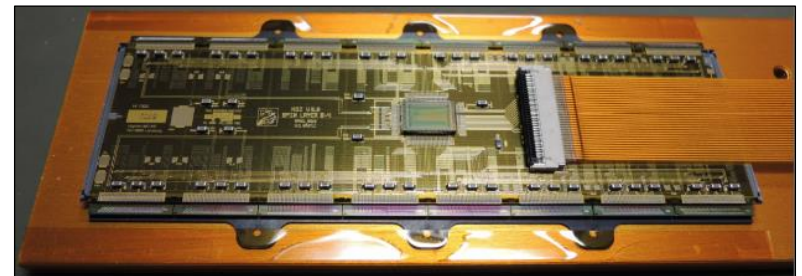
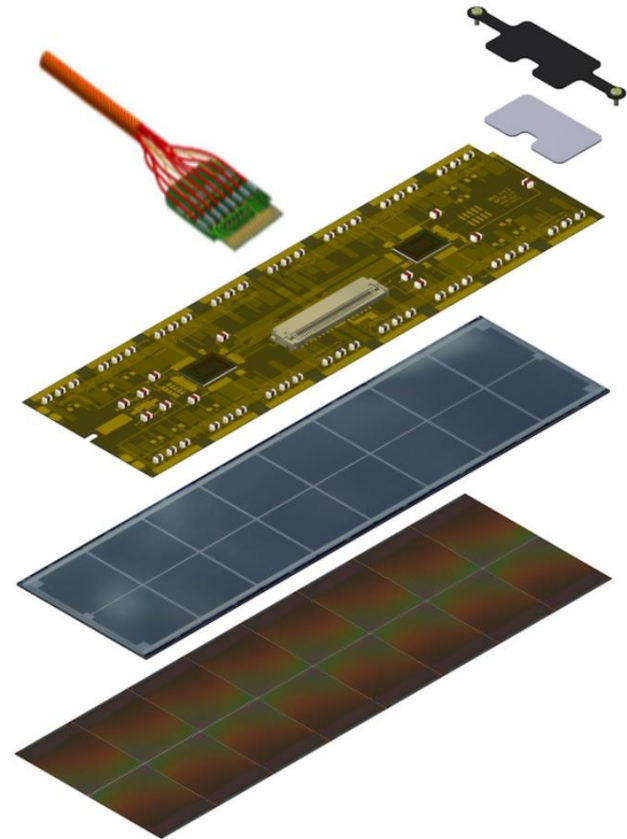
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→ 285 μm active thickness
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Modules for CMS phase 1 pixels

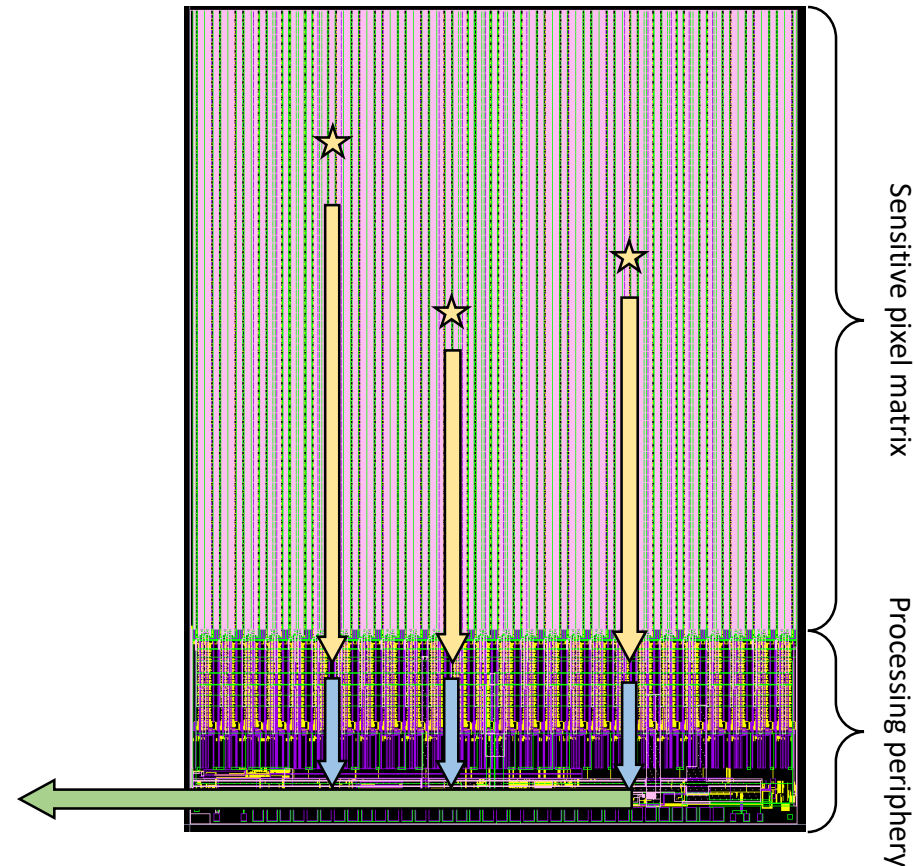
- **Sensor:**
 - Same as phase 0, 16 ROCs per sensor
 - n-in-n silicon design, 4160 pixels / ROC
 - pixel size: $100\ \mu\text{m} \times 150\ \mu\text{m}$
 - Edge pixel size increased, no ganged pixels
 - $285\ \mu\text{m}$ active thickness
- **ROC (ReadOut Chip):**
 - $250\ \text{nm}$ CMOS technology
 - $160\ \text{Mbit/s}$ readout
 - All transistors enclosed layout, manual layout and routing
 - Column-drain architecture with analog readout, single on-chip ADC for digital data transmission
- **TBM (Token Bit Manager):**
 - Interface to ROCs + readout control of ROCs, $400\ \text{Mbit/s}$ readout
 - Different number of TBM cores for variable bandwidth:
L3 + L4: 1 core, L2: 2 cores, L1: 4 cores



Readout chip overview

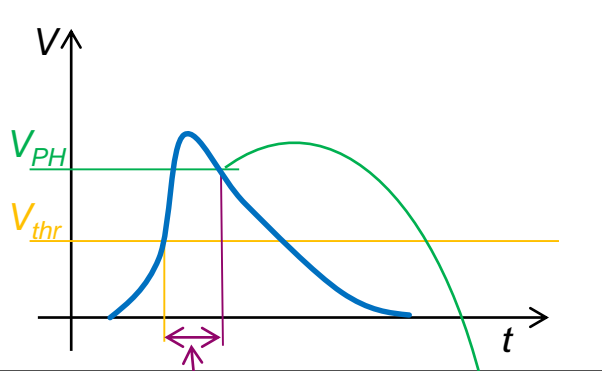
- Column drain architecture:
 1. Copy all hits from matrix into buffers
 2. Wait for trigger
 3. Digitize hit and send data (or delete hit)
 - Very similar architecture in ATLAS FE-I3, digitization using ToT mechanism
→ clock in matrix, increased current consumption
 - Fully analog matrix readout in CMS pixels
→ no clock in matrix, low current consumption

Designed by PSI

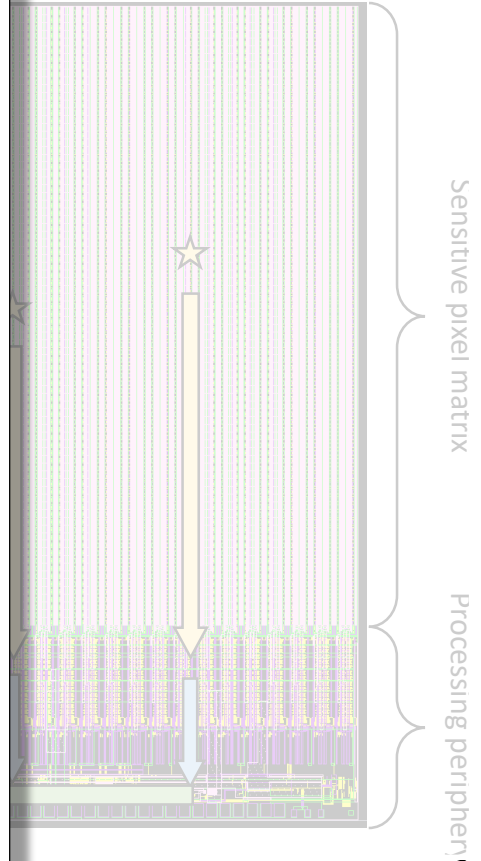
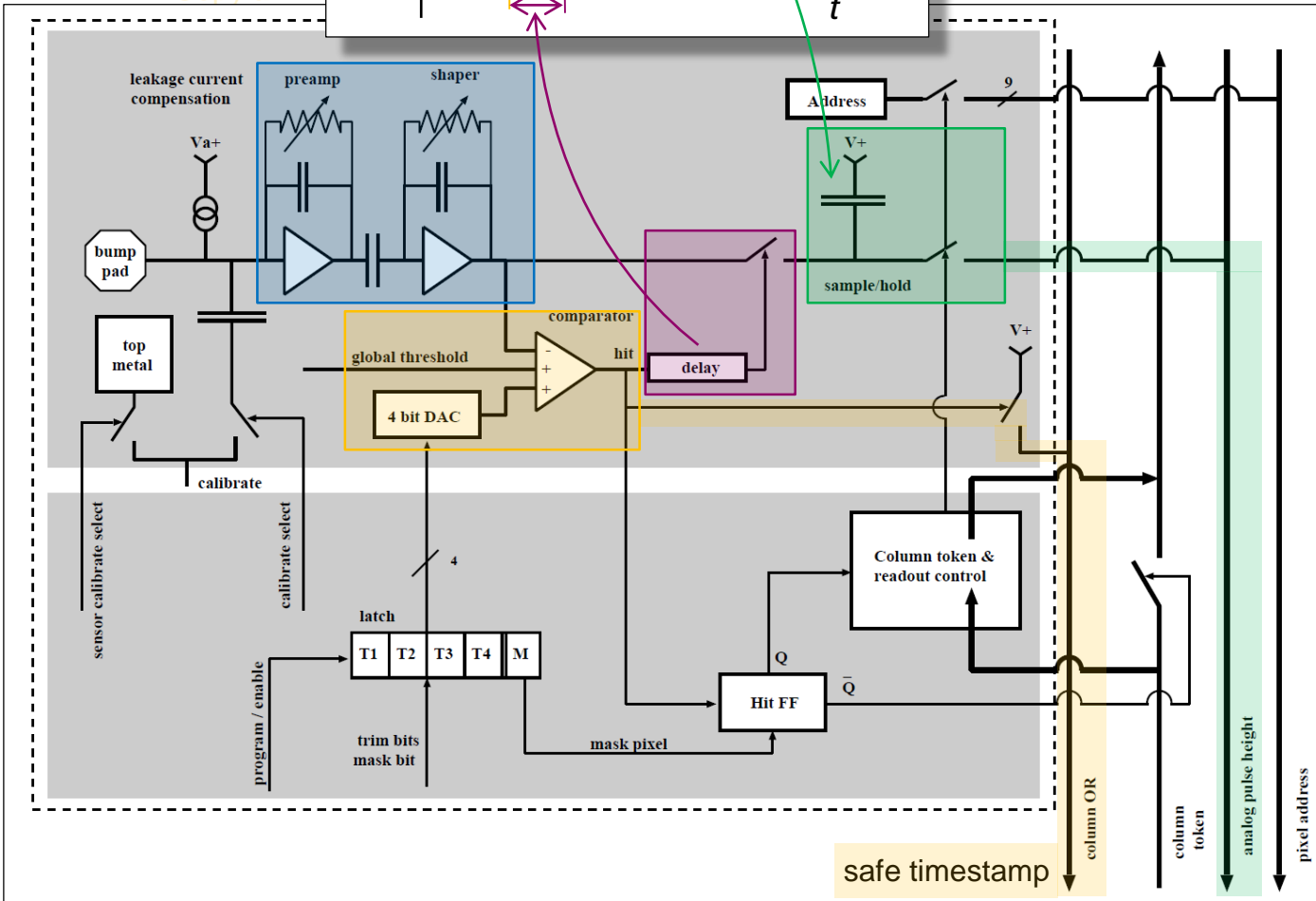


Readout

- Column driver
- 1. Copy all hit



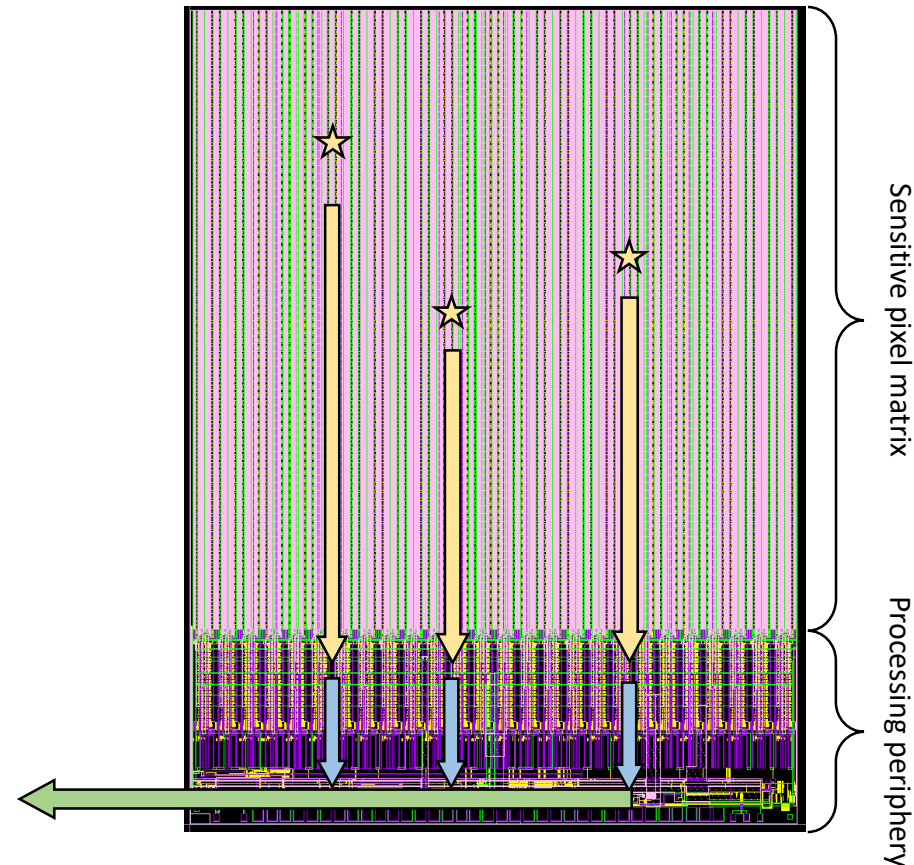
Designed by PSI



Readout chip overview

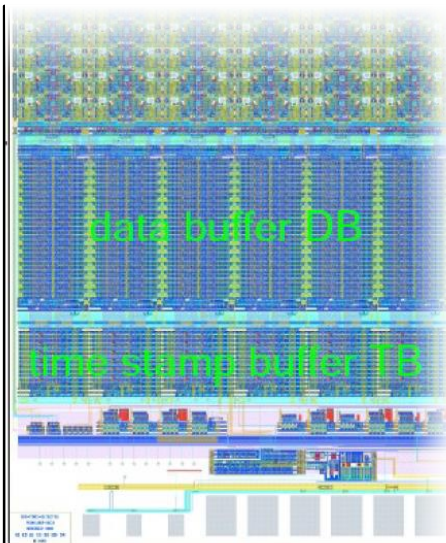
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→ clock in matrix, increased current consumption
 - Fully analog matrix readout in CMS pixels
→ no clock in matrix, low current consumption
- 0.1 W/cm^2 power consumption (FE-I4: 0.2 W/cm^2)
- Size: $7.9 \text{ mm} \times 10.2 \text{ mm}$
- 160 Mbit/s readout
- $< 2000 e$ threshold
- 8 bit pulse height charge information
- Data loss: 1.6% at 150 MHz/cm^2
 - Buffer depth increase wrt. phase 0
 - Inefficiency due to copy time

Designed by PSI



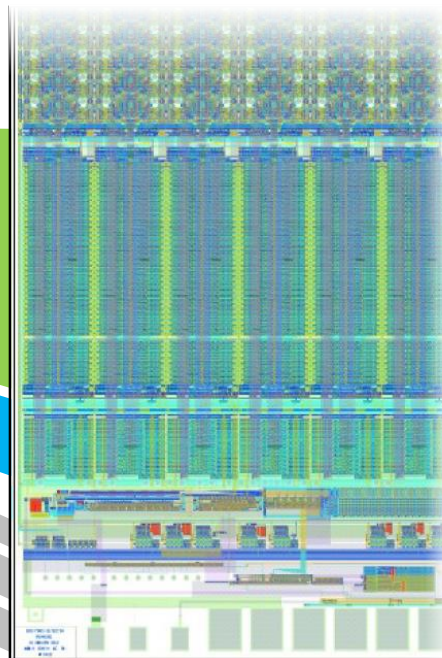
From CMS phase 0 to phase 1 ROCs

PSI46 – phase 0 all layers



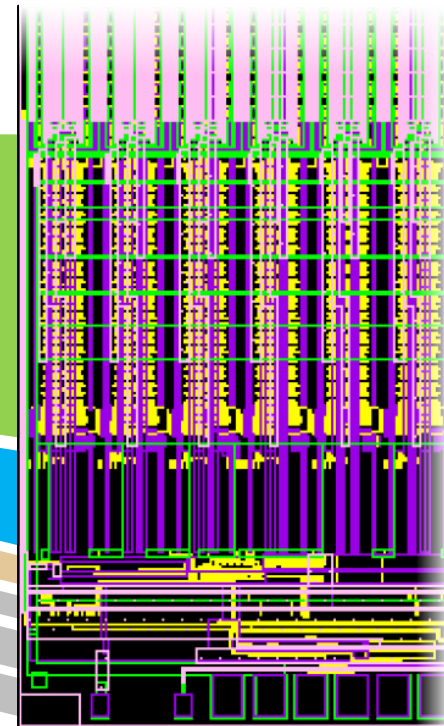
- DB: 32, TB: 12
- RO: 40 MHz analog
- Analog Column Drain architecture

psi46dig – phase 1 L2-L4



- DB: 80, TB: 24
- RO: 160 MHz (digitized)
- Analog Column Drain architecture
- ADC + 64 ReadOut Buffers

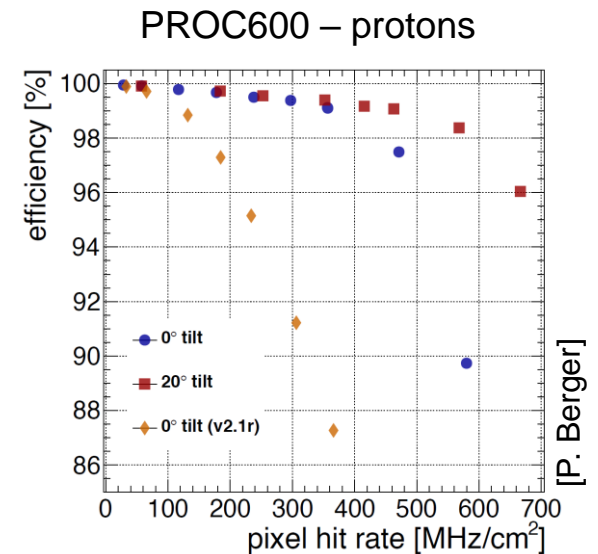
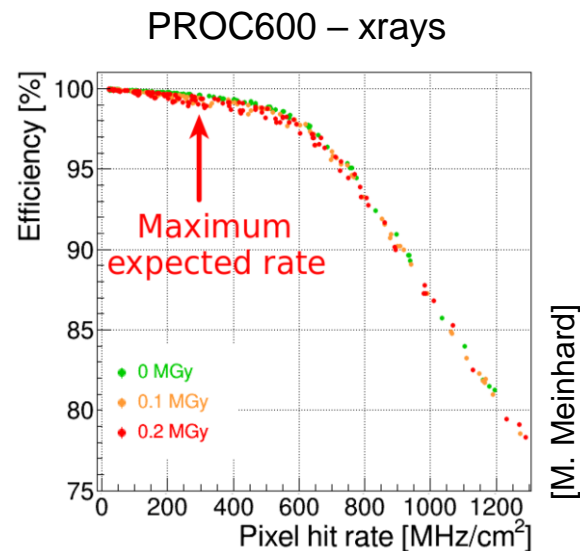
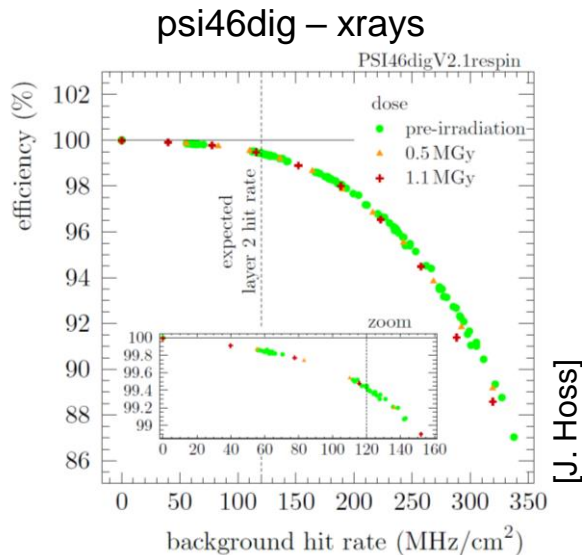
PROC600 – phase 1 L1



- DB: 4x56, TB: 40
- RO: 160 MHz (digitized)
- Analog *dynamic cluster* Column Drain architecture
- ADC + 64 ReadOut Buffers

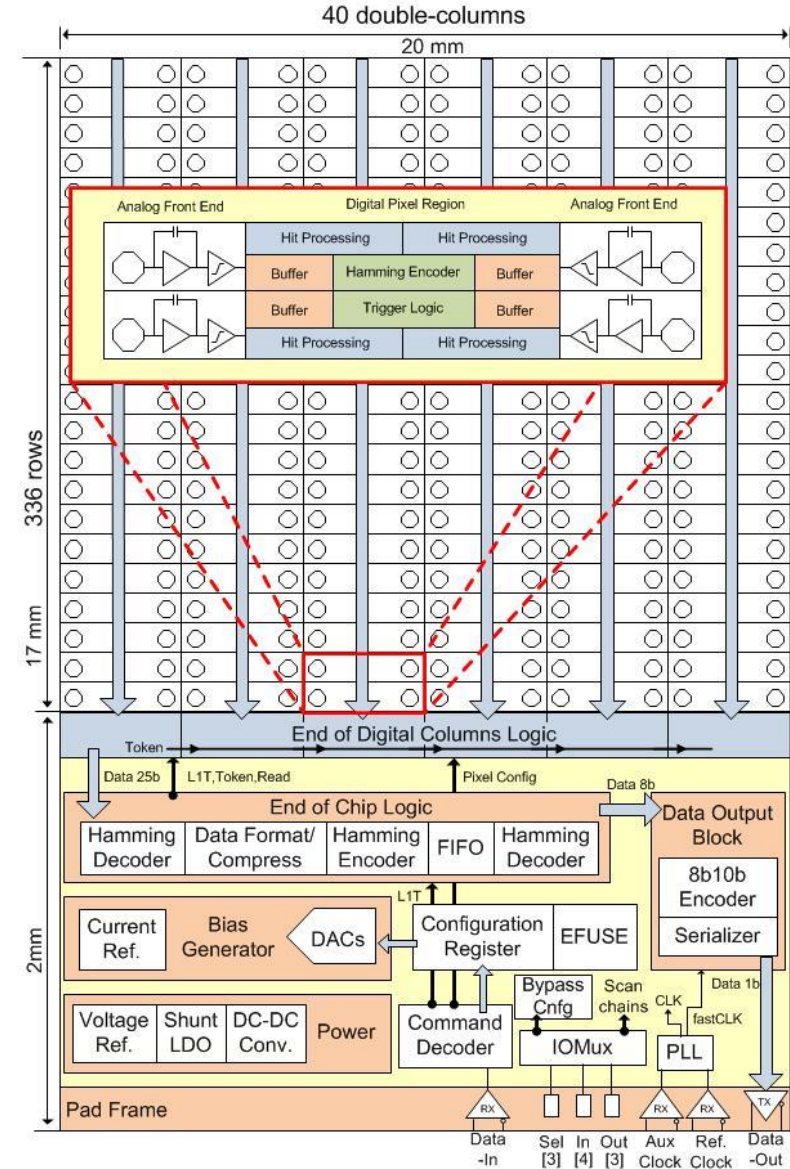
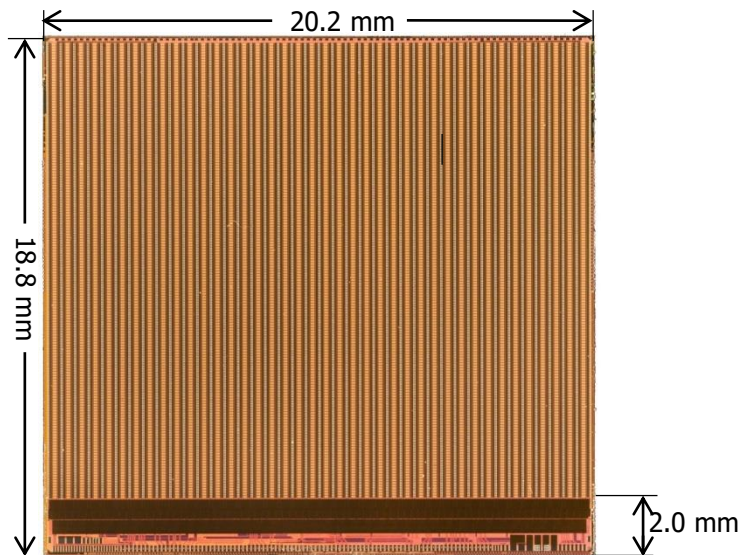
Phase 1 ROCs efficiency

- Generate flux with xrays or protons → measure pixel hit rate
- Test charge injection in single pixel → measure detection efficiency
- Significant efficiency increase wrt. phase 0 ROCs
→ increase of buffer depth (+*cluster copying* in PROC600)
- Performed on all modules during QC tests for efficiency validation



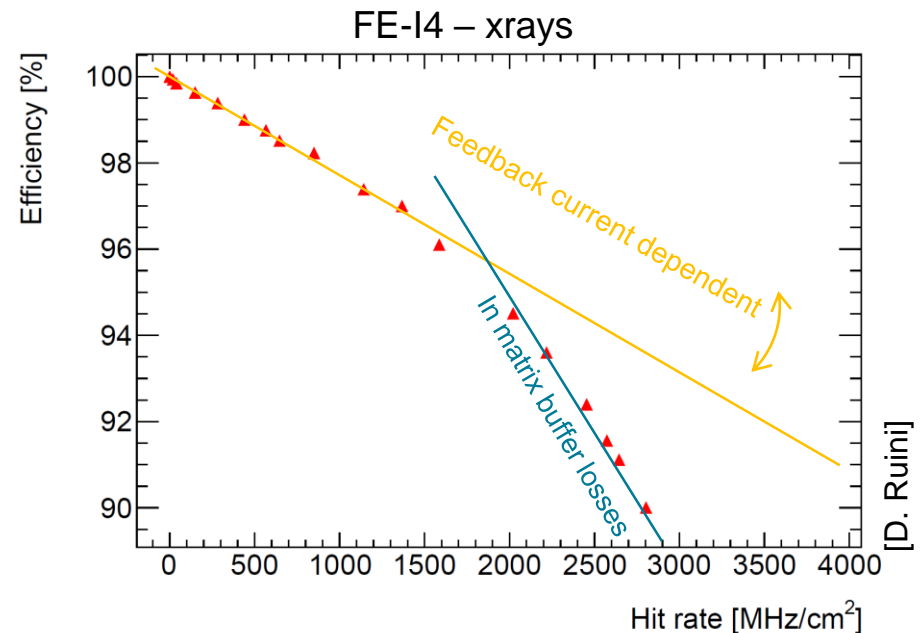
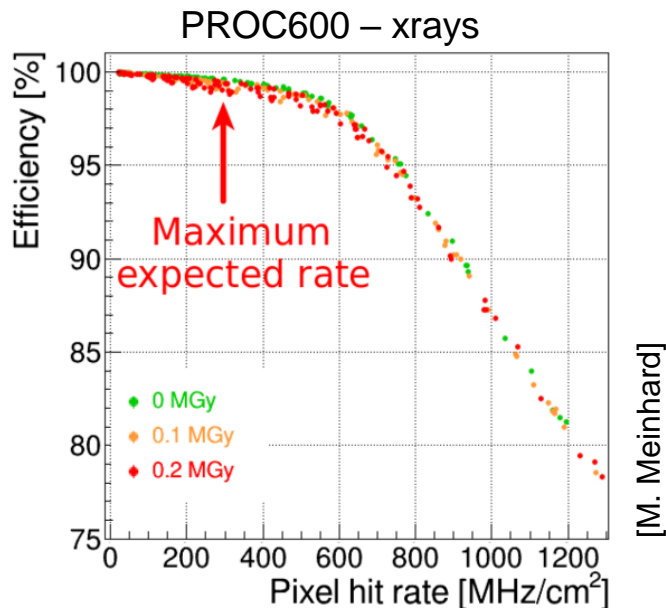
FE-I4 Overview

- Largest chip in high energy physics:
19 x 20 mm² → ~6 times size of FE-I3 or CMS ROCs.
- No column-drain architecture:
avoid copying of untriggered data
→ buffer and trigger logic in pixel cell
→ increase of digital logic
→ power consumption: 0.2 W/cm²
- Readout structured in four pixel regions,
→ efficient cluster readout



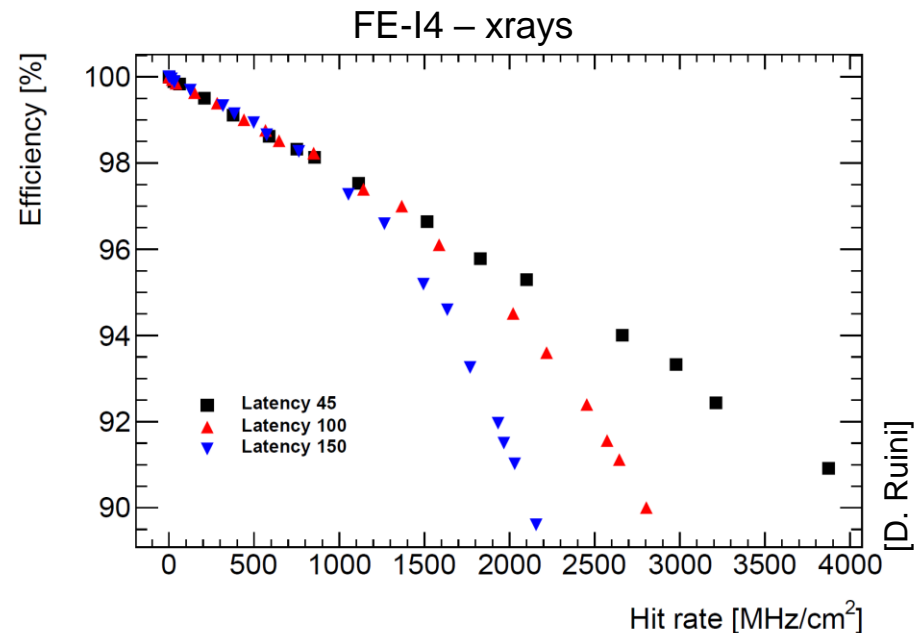
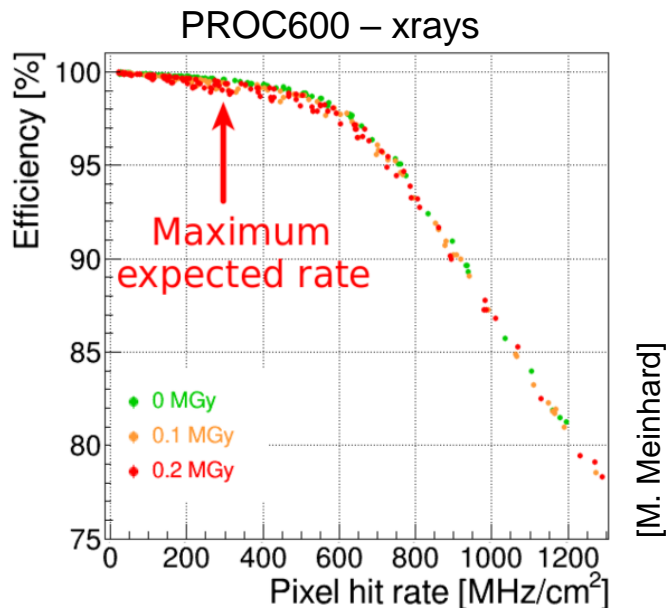
ATLAS FE-I4 efficiency

- Efficiency validation in FE-I4 can be done with internal injection (done during QC tests)
- Performed comparison measurement using xrays and similar settings
- Pulse Height measurement allows faster amplifier return than ToT
→ higher efficiency
- Significantly less copy/buffer inefficiency in FE-I4

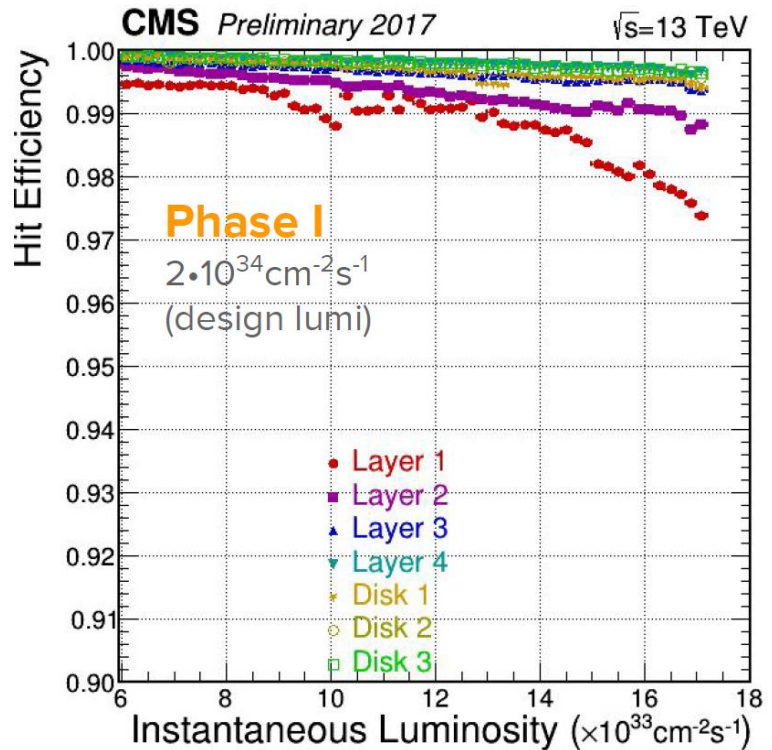
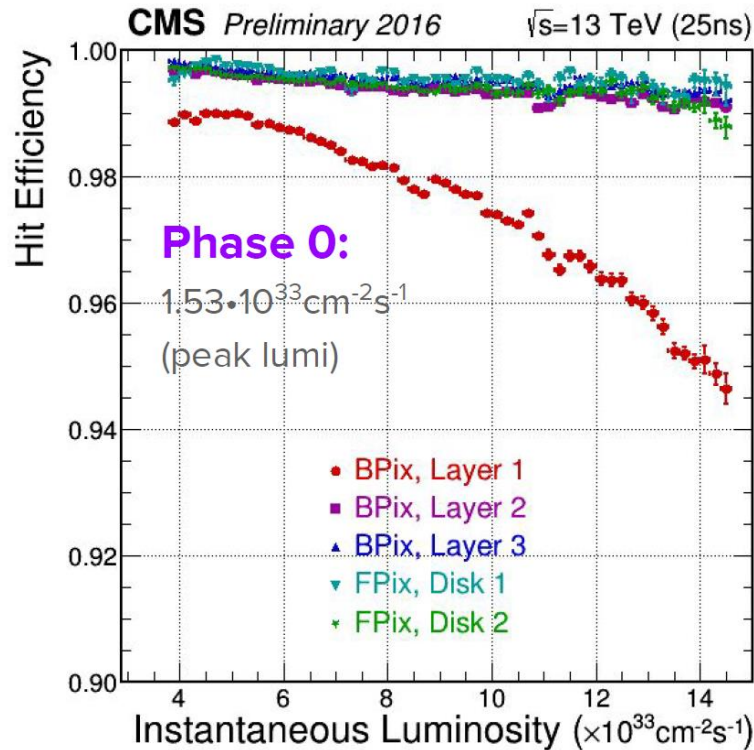


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Efficiency improvement in detector



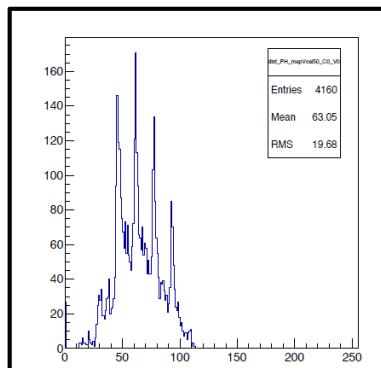
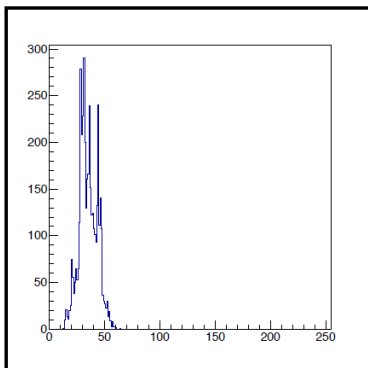
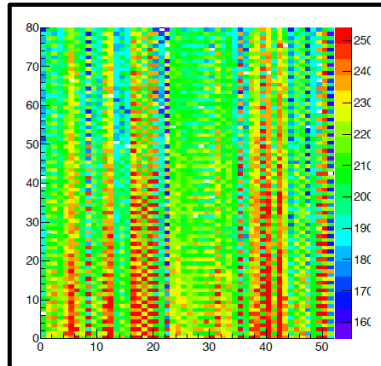
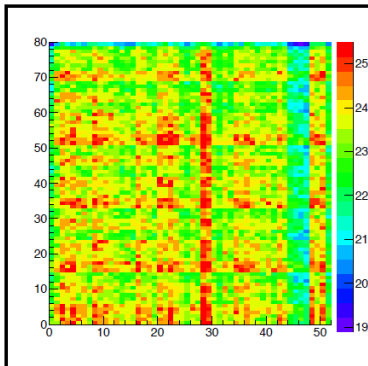
- CMS phase 1 pixel detector with very good hit finding efficiency
- Even the new Layer 1 at smaller radius exceeds phase 0 performance, at $12 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$: 96% \rightarrow 99% (radius: 4.4 cm \rightarrow 2.9 cm)

Phase 1 ROCs charge resolution

- No pixel by pixel PH adjustment

digv21respin

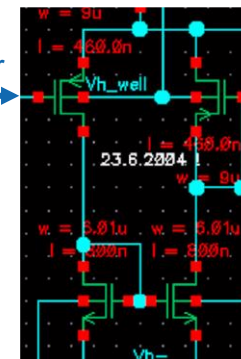
PROC600



[D. Zhu]

- Good uniformity in psi46dig
- Parallel copying of four hits in PROC600
 → four current mirrors per double column in same area
 → reduction of transistor size required
 → relative production variation increased

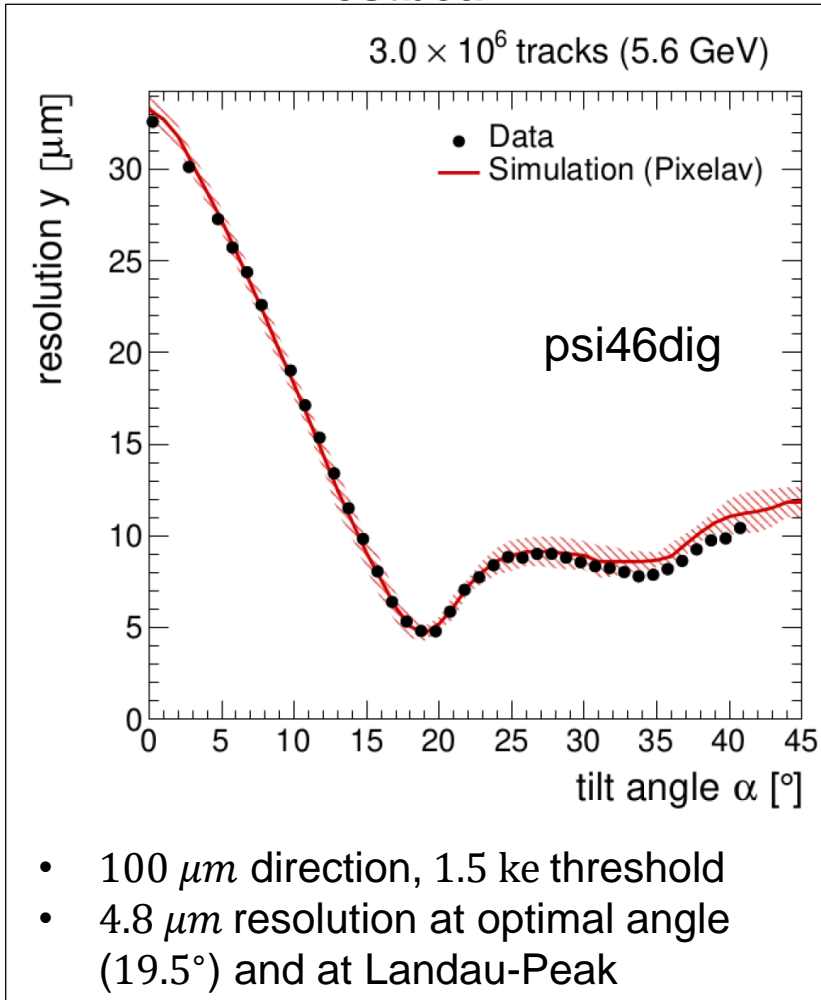
Voltage from sample and hold capacitor



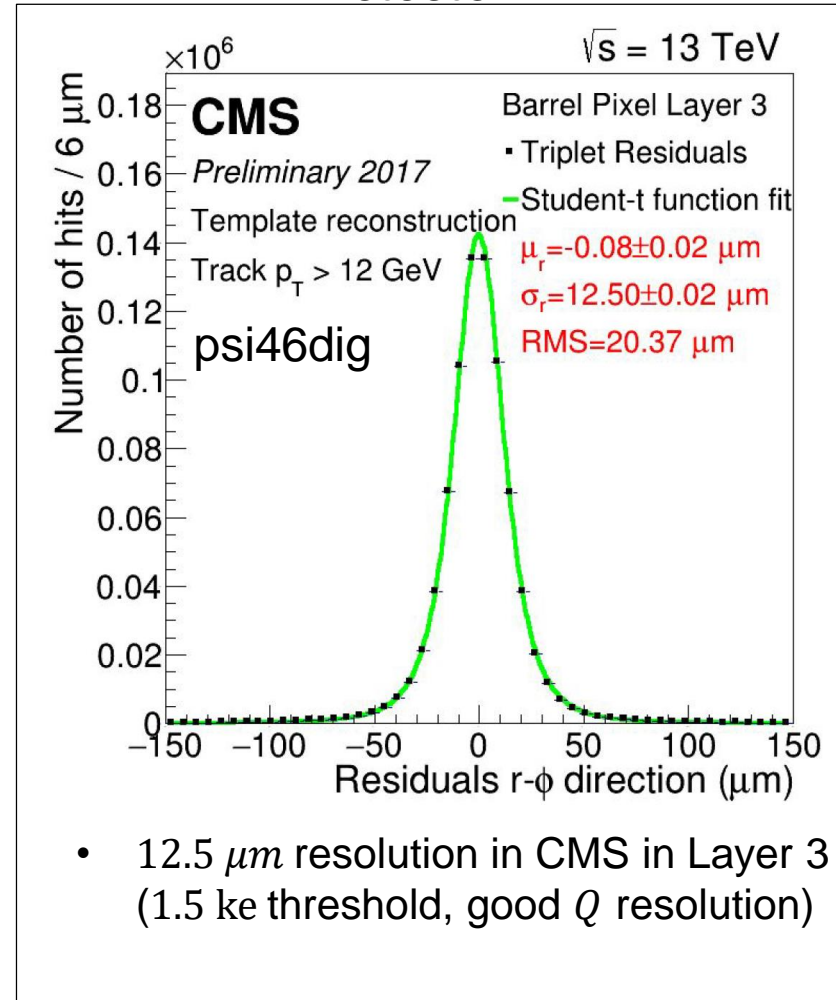
to PH buffer

Phase 1 detector performance: spatial resolution

Testbeam

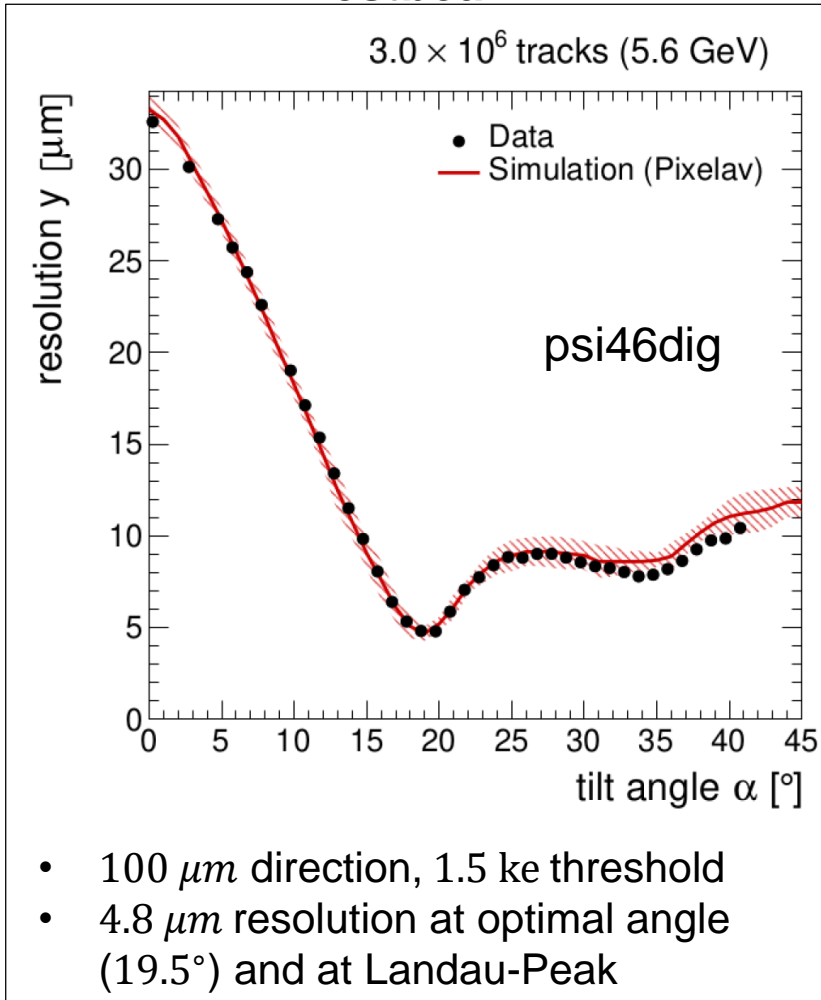


Detector

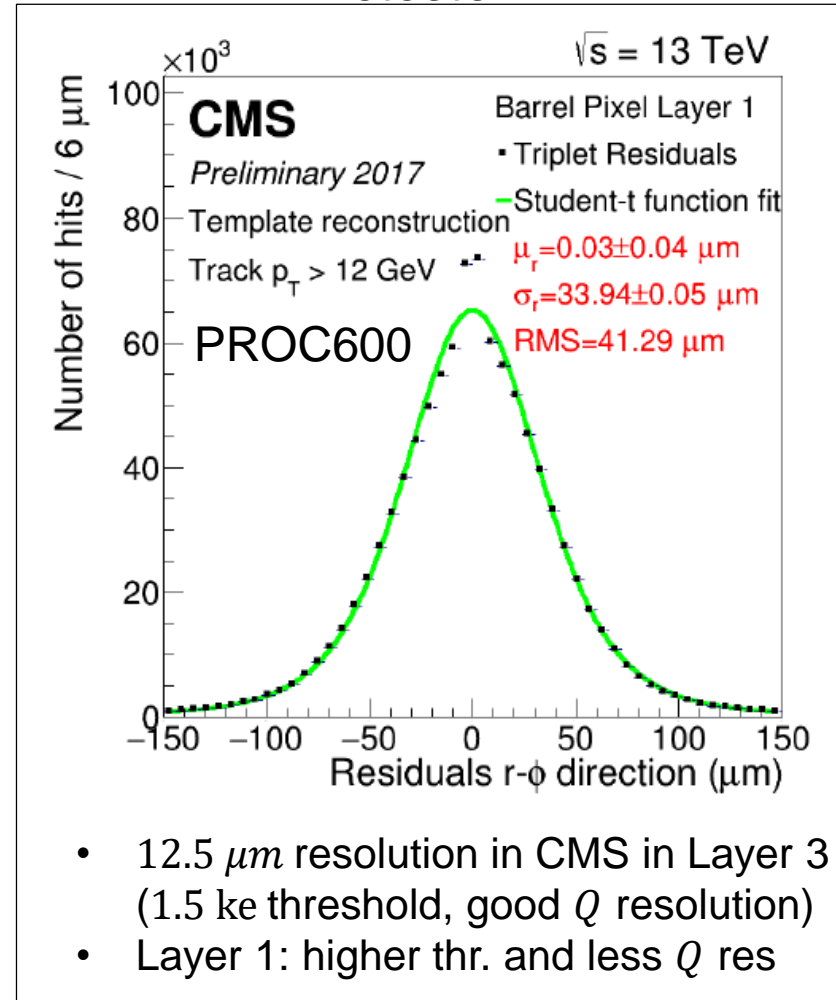


Phase 1 detector performance: spatial resolution

Testbeam

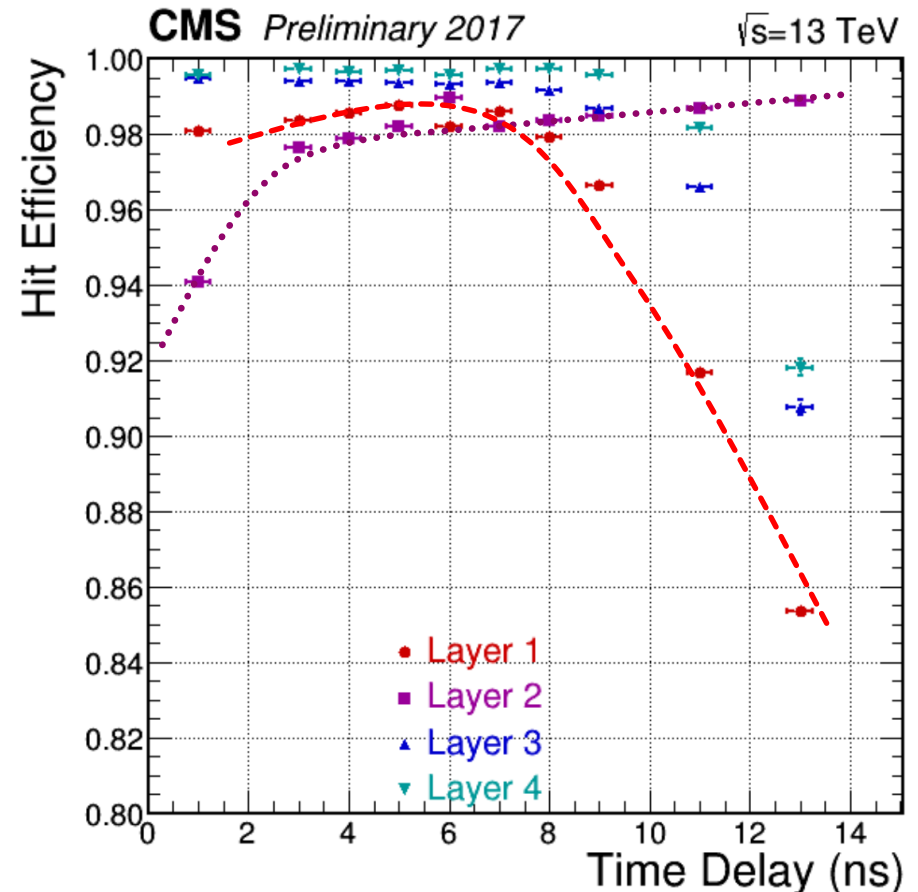


Detector

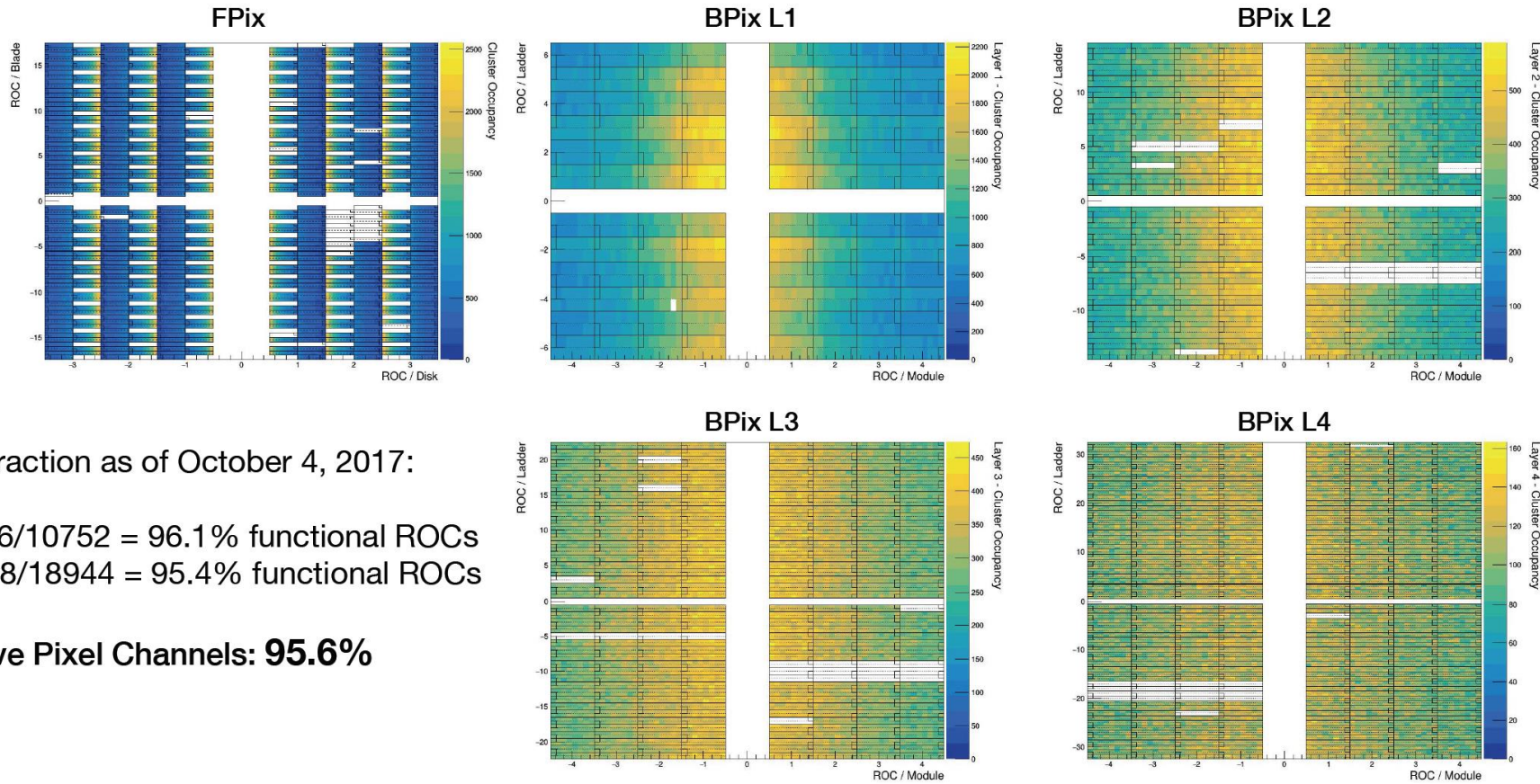


Phase 1 detector performance: timing

- Fine time adjustment in pp collisions
→ PROC600 faster than psi46dig
- Layer 1 and layer 2 on same clock link
- Timing optimized for layer 1 efficiency
→ slightly early for layer 2
- Improved situation by adjusting on-chip bias settings



Phase 1 detector performance: occupancy



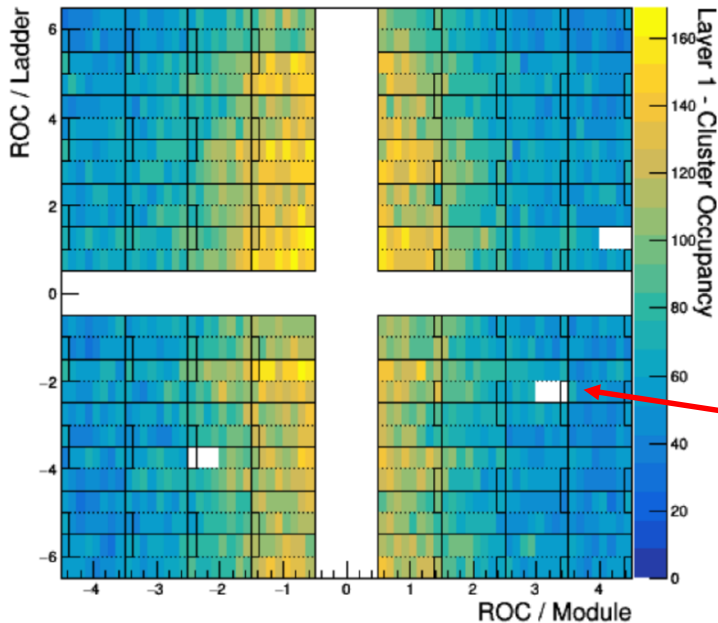
Detector fraction as of October 4, 2017:

FPix 10336/10752 = 96.1% functional ROCs

BPix 18068/18944 = 95.4% functional ROCs

Total Active Pixel Channels: **95.6%**

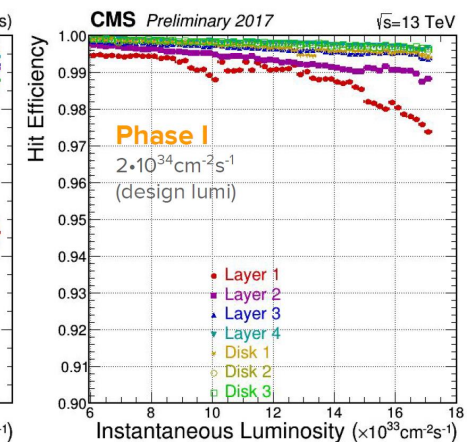
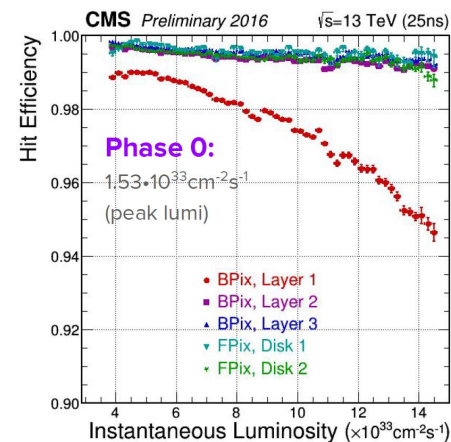
Phase 1 detector performance: TBM SEUs



- SEU problem in TBMs observed
- FlipFlop not connected to reset
→ recovery with power-cycle
- Effect depending on luminosity, position, module type (# TBM cores)
→ Layer 1 most effected,
→ holes with granularity of 4 ROCs
→ dynamic inefficiency maps

Summary

- CMS installed a completely new pixel detector in February/March 2017
- Construction as well as commissioning very challenging
 - many difficult issues solved or optimizations found
 - detector shows good or better performance than previous detector in 2017!
 - Congratulations to the commissioning and operation team!
- Performance of detector “dynamic”, commissioning still ongoing and new challenges appearing
 - action needed for 2018 run
- Hopefully efficient use of winter break
 - Rapid access to detector pays off!



backup

Readout chip overview

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- 3. Digitize h
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- clock i
- Fully ana
- no clo

