Institut "Jožef Stefan" Ljubljana, Slovenija
a
University of Glasgow
b
CERN
c
universitätbonn Rheinische Friedrich-Wilhelms-Universität Bonn
d
UNIVERSITY OF OXFORD
e
Univerza v Ljubljani
Fakulteta za matematiko in fiziko

Development of the monolithic "MALTA" CMOS sensor for the ATLAS ITK outer pixel layer

TWEPP 2018, Antwerp, Belgium, 21.09.2018

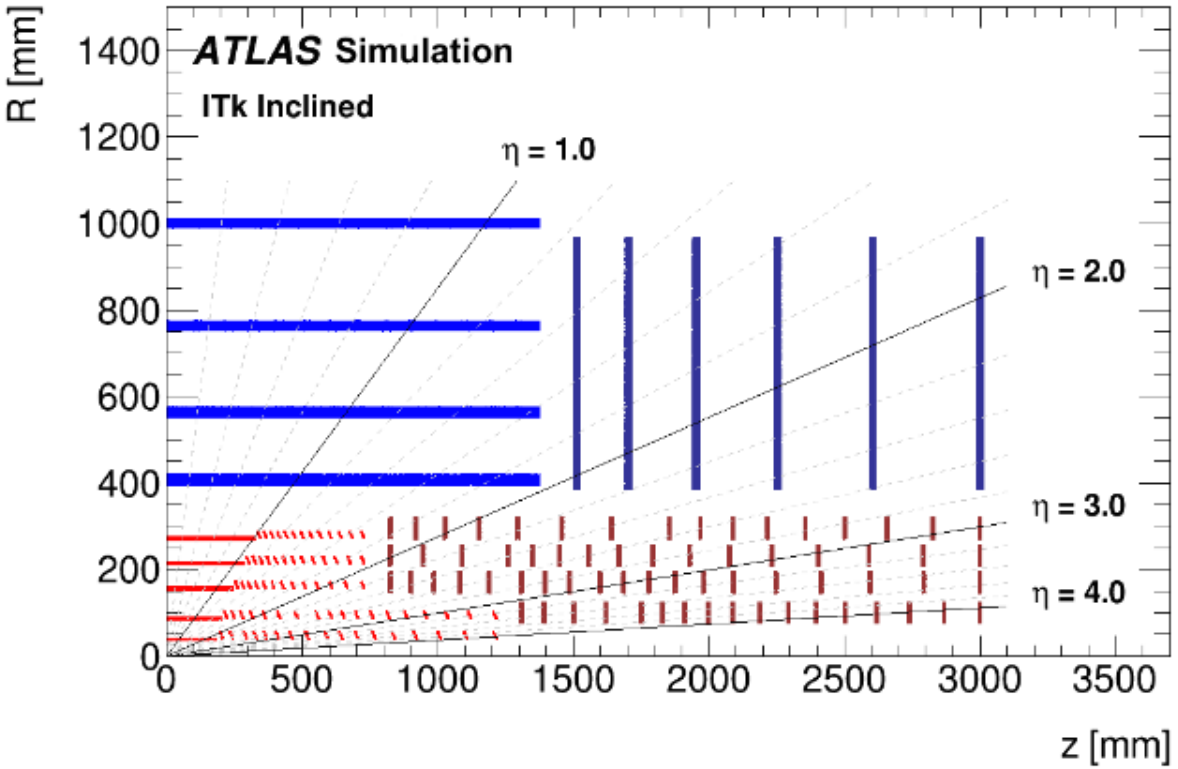
B. Hiti[a], L. Argemi[b], I. Asensi Tortajada[c], I. Berdalović[c], I. Caicedo Sierra[d], R. Cardella[c], F. Dachs[c], V. Dao[c], N. Egidos Plaja[c], A. Gorišek[a], T. Hemperek[d], H. Krüger[d], T. Kugathasan[c], I. Mandić[a], C. A. Marin Tobon[c], K. Moustakas[d], M. Münker[c], H. Pernegger[c], F. Piro[c], P. Riedler[c], P. Rymaszewski[d], C. Riegel[c], E. J. Schioppa[c], A. Sharma[c,e], W. Snoeys[c], C. Solans Sanchez[c], T. Wang[d], N. Wermes[d]

ATLAS Phase II ITk upgrade

See talk by Z. Chen, S. Terzo

- HL-LHC Pixel detector upgrade (2024-2026): 5 pixel layers, inclined layout
- Option for the outermost Layer 4: Depleted Monolithic Active CMOS sensors
- Requirements for Pixel Layer 4:
  - Radiation tolerance (without safety factors):
    - **NIEL 1e15 n_{eq}/cm^2**
    - **TID 80 Mrad**
  - Hit rate 100 – 200 MHz/cm^2
  - Timing resolution 25 ns

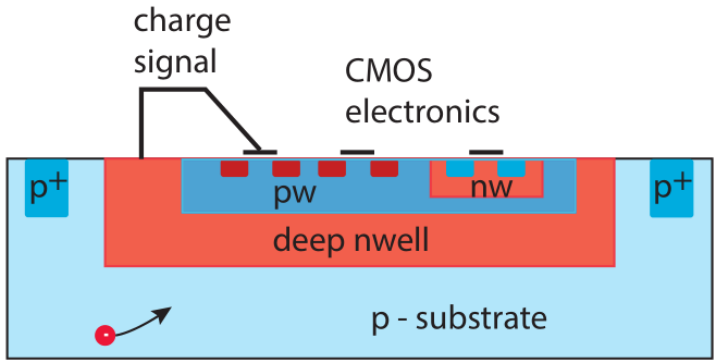
ATLAS ITk Pixel TDR



CMOS sensors: Large vs. Small collection electrode

See talks by W. Snoeys, Z. Chen, S. Terzo

Large collection electrode

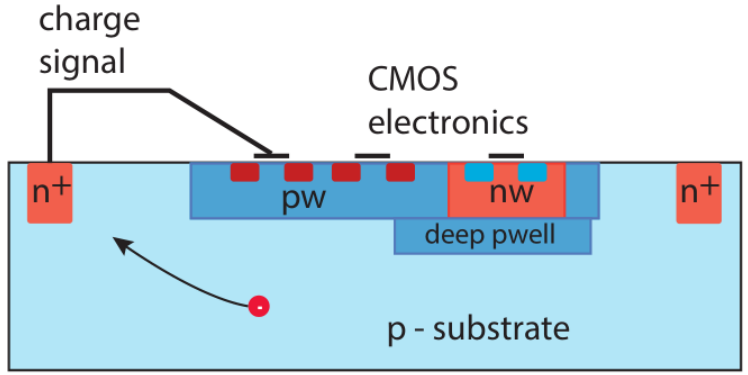


M. Garcia-Sciveres and N. Wermes, arXiv:1705.10150

- Larger capacitance: $C \approx 300 - 400$ fF
- Higher analog power, sensitive to crosstalk
- Uniform, strong drift field, high radiation tolerance and detection efficiency

$$\tau_{CSA} = \frac{1}{g_m}\frac{C}{C_f} \qquad ENC^2_{thermal} = \frac{4}{3}\frac{kT}{g_m}\frac{C^2}{\tau_f}$$

Small collection electrode (MALTA)



- Smaller capacitance: $C \approx 3$ fF → low power
- Less sensitive to crosstalk
- Longer drift paths
- Full depletion can be achieved by modifying the process → radiation tolerance increases

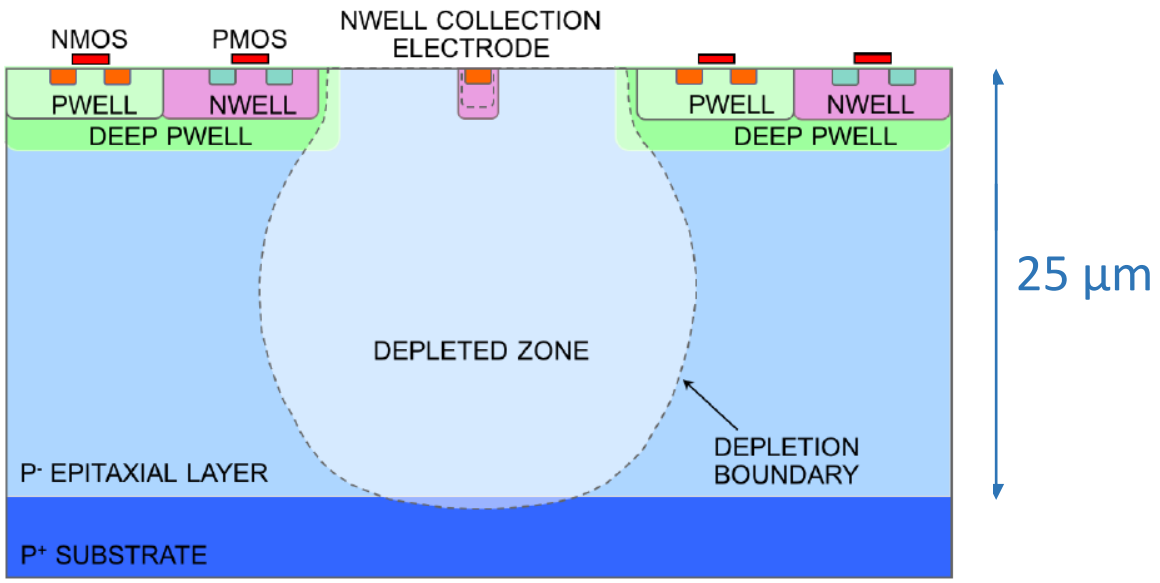
$$\frac{S}{N} \approx \frac{Q/C}{\sqrt{g_m}} \sim \frac{Q/C}{\sqrt[m]{P}} \Rightarrow P \sim \left(\frac{Q}{C}\right)^{-m}$$

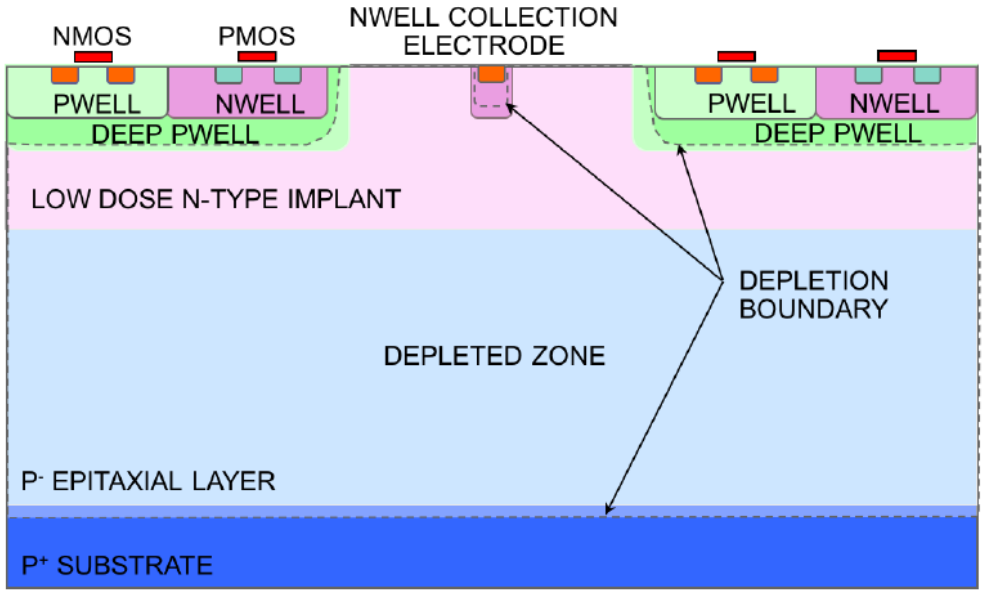
TowerJazz process: Small collection electrode

TowerJazz 180 nm CMOS imaging process, 4 nested wells, 25 µm p epitaxial layer

Typical bias voltages: -20 V (substrate), -6 V (deep PWELL)

See talk by W. Snoeys





Standard process

no full depletion on pixel edges

partially charge collection by diffusion, not radiation tolerant

Modified process

additional low doped n-layer

full depletion, maintains low capacitance, better radiation tolerance, faster charge collection

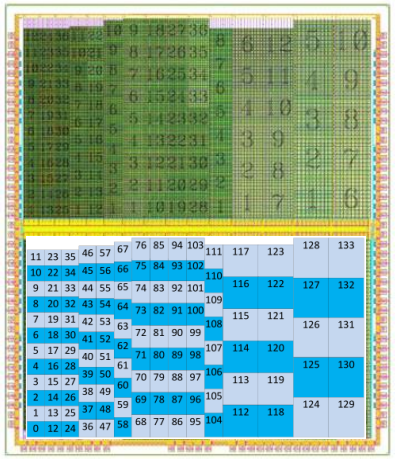
W. Snoeys et al.
DOI 10.1016/j.nima.2017.07.046

TowerJazz 180 nm development line

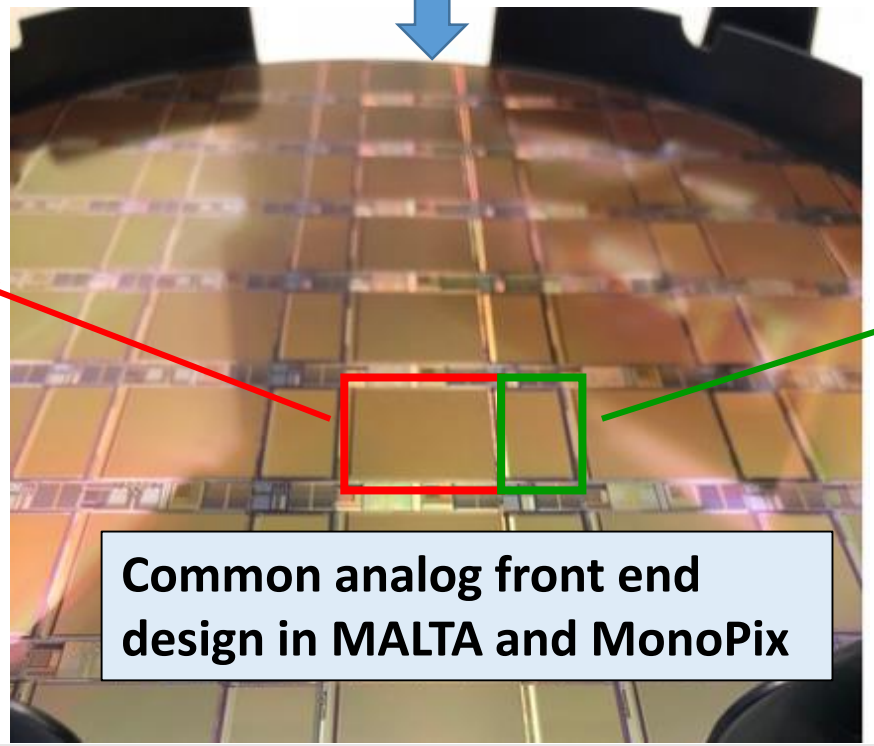
ALPIDE chip for ALICE ITS upgrade

https://doi.org/10.1016/j.nima.2016.05.016

radiation hardness,
timing, hit rate
x 100



TJ Investigator (2015)
> 250 different pixel flavors
Analog output after CSA



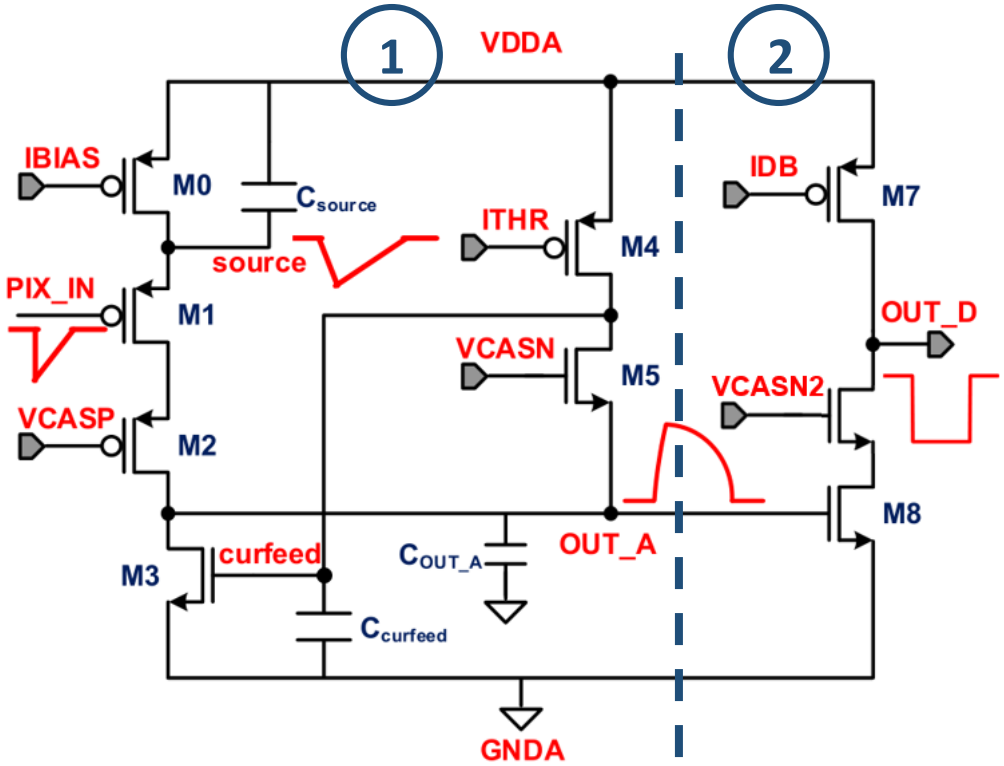
TJ MALTA (2018)
20 x 22 mm^2 full size
Asynchronous matrix readout

Design team (CERN)
W. Snoeys, T. Kugathasan,
C. Marin Tobon, I. Berdalović,
R. Cardella, N. Egidos Plaja

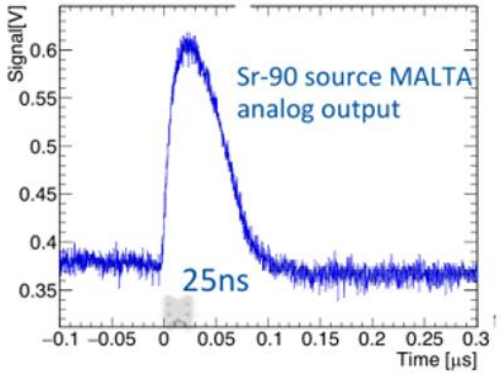
TJ MonoPix (2018)
20 x 10 mm^2 half size
Column drain readout

Digital readout designed
by **University of Bonn**
T. Wang et al 2018 JINST 13 C03039

Charge sensitive front end



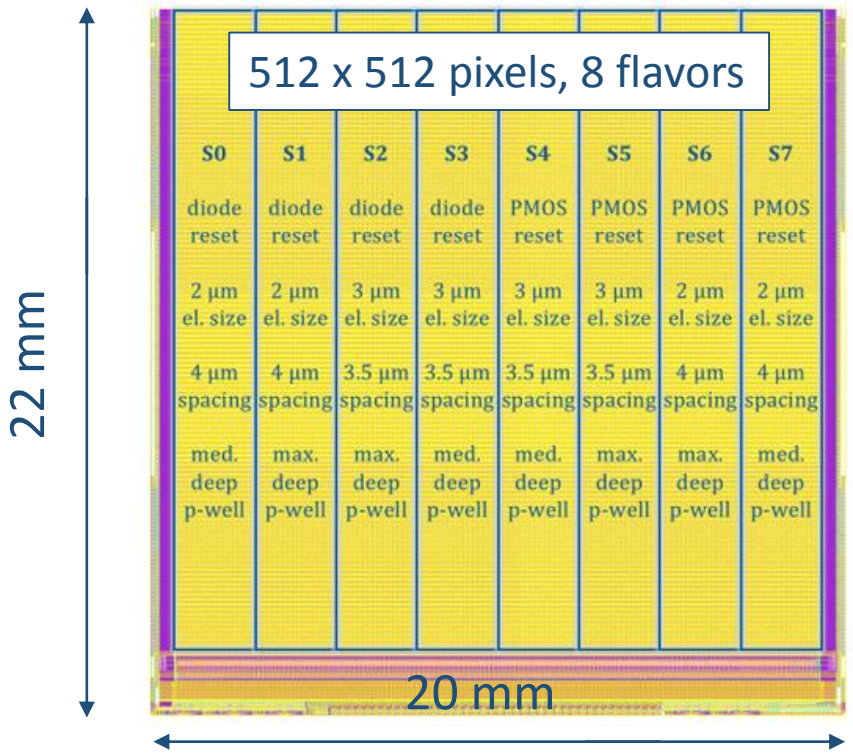
1 – amplification
2 – discrimination

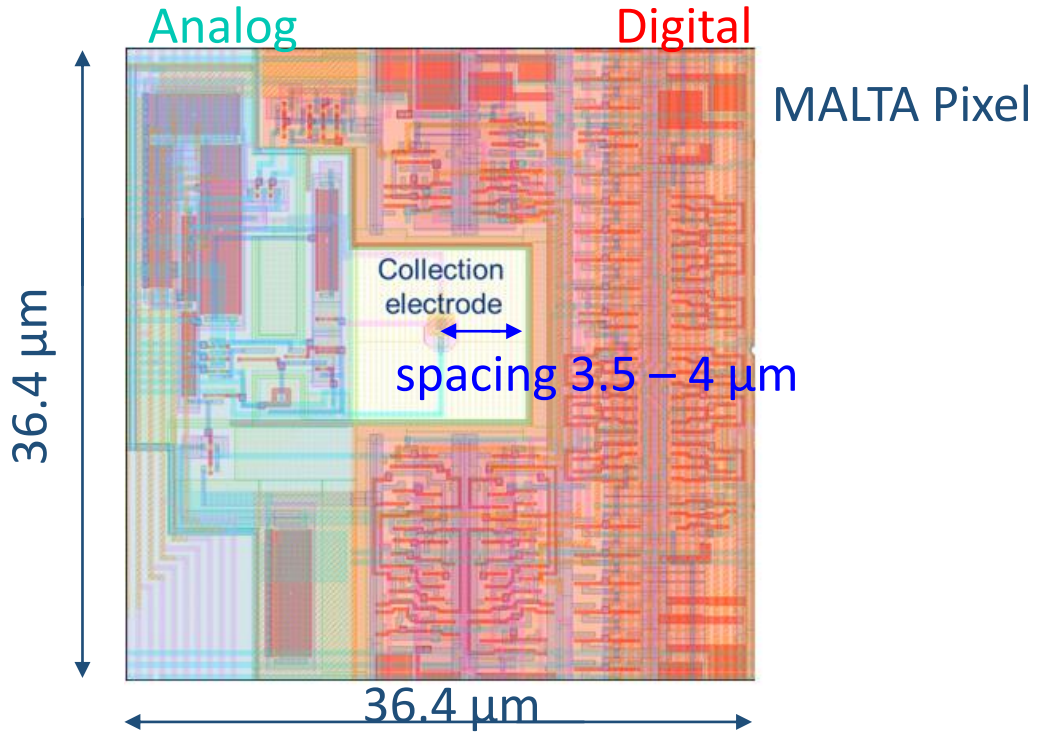


- Operating principle derived from ALPIDE front end
  D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042
- < 5 fF sensor capacitance → excursion at input of tens of mV
  - Voltage amplifier can take the place of a standard CSA
  - Optimization for minimal power consumption and fast timing response
- Power 0.9 µW, thr. ≈ 200 e^-, ENC ≈ 12 e^-, gain 0.4 mV/ e^-

- M1 acts as a source follower to avoid loading the input
- M2 is a cascode transistor to increase the gain on the output node and eliminate the Miller effect for the input node.
- The analog output node is stabilized at low frequencies by active feedback on the transistor M3
- Efficient current usage for the input (the same branch current powers the source follower and the amplification stage)
- MALTA: optional clipping of the analog pulse

TJ MALTA

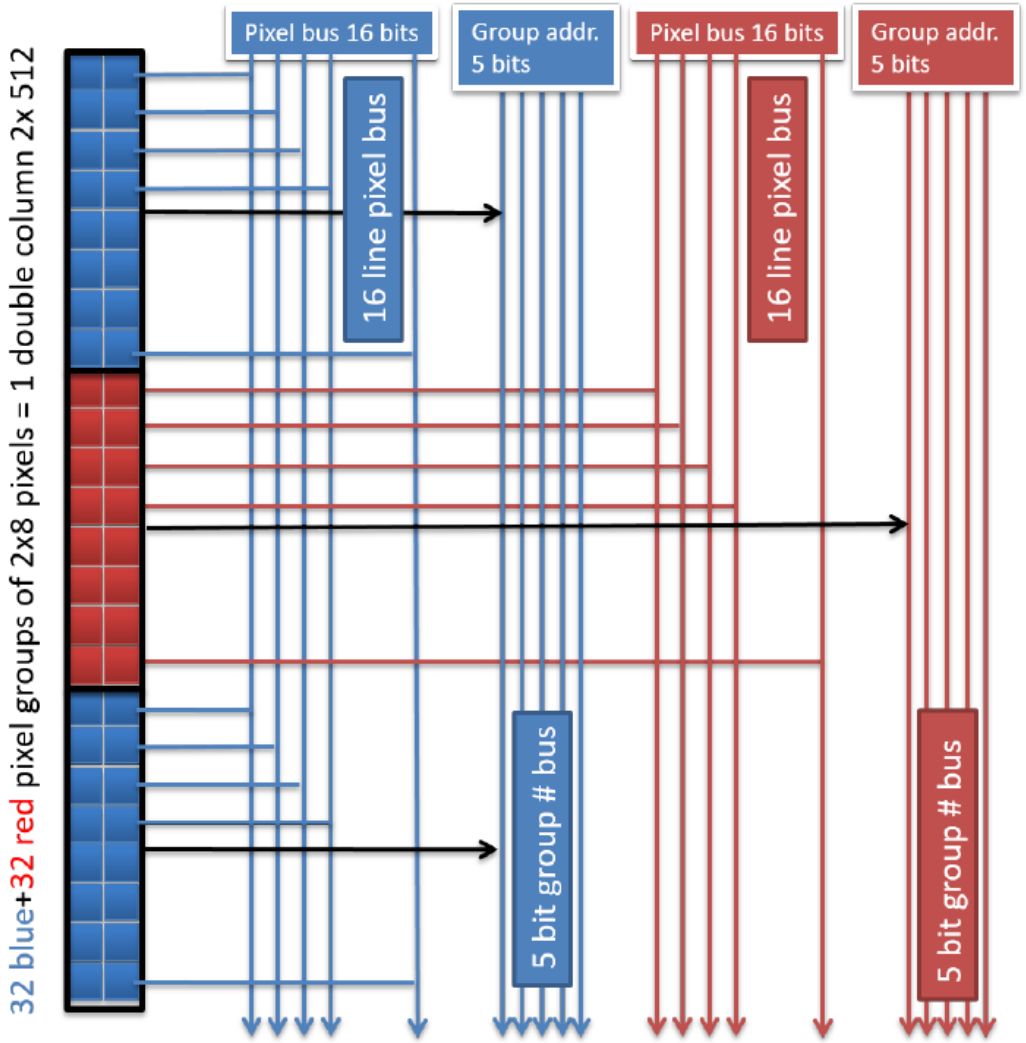




- Novel asynchronous readout, no clock distribution over pixel matrix → reduced power
- Low threshold spread, no in-pixel threshold tuning
- Analog power ≈ 1 µW per pixel (75 mW/cm^2)
- Digital power (Layer 4) ≈ 10 mW/cm^2
- Time-walk based charge information

Asynchronous column-drain architecture

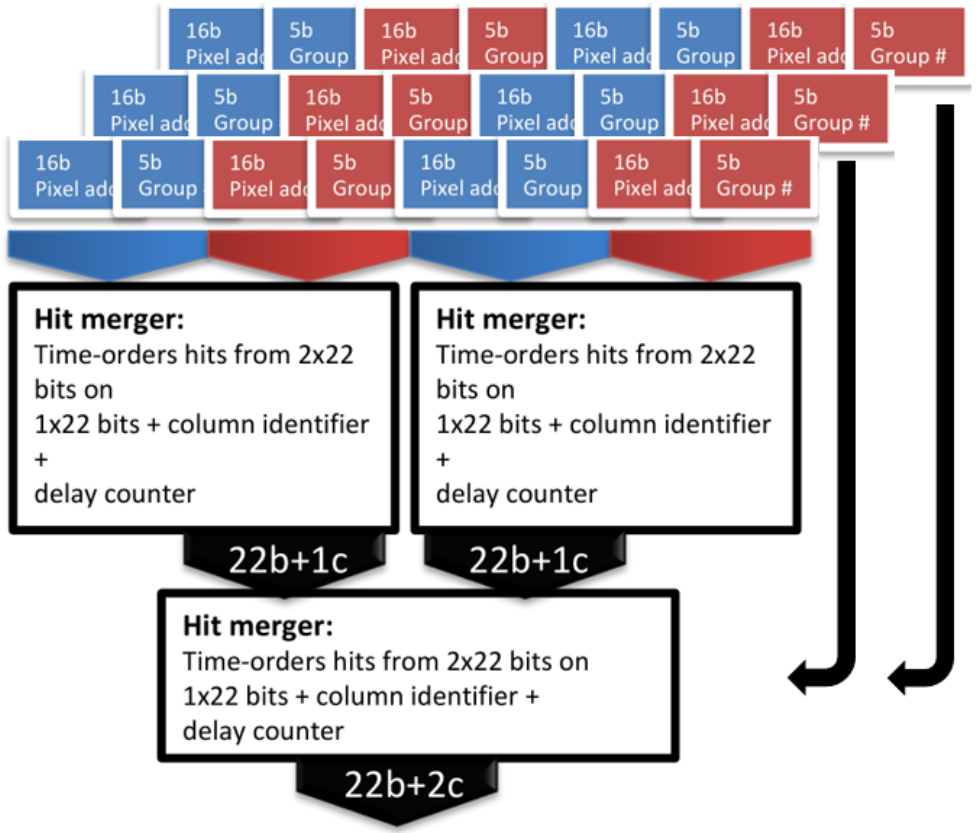
- Front end discriminator outputs are transmitted asynchronously over high speed bus to chip periphery
- 2 independent buses serve alternating 2 x 8 pixel groups (one bus for the red groups and another for the blue groups)
  - Significantly reduced number of lines per pixel
  - Important to minimize probability for data collisions
  - Adjustable pulse length 0.5 – 2 ns
- 22 bits per bus: pixel pattern (16b) + reference (1b) + group address (5b) → 22b



*I. Berdalovic et al 2018 JINST **13** C01023*

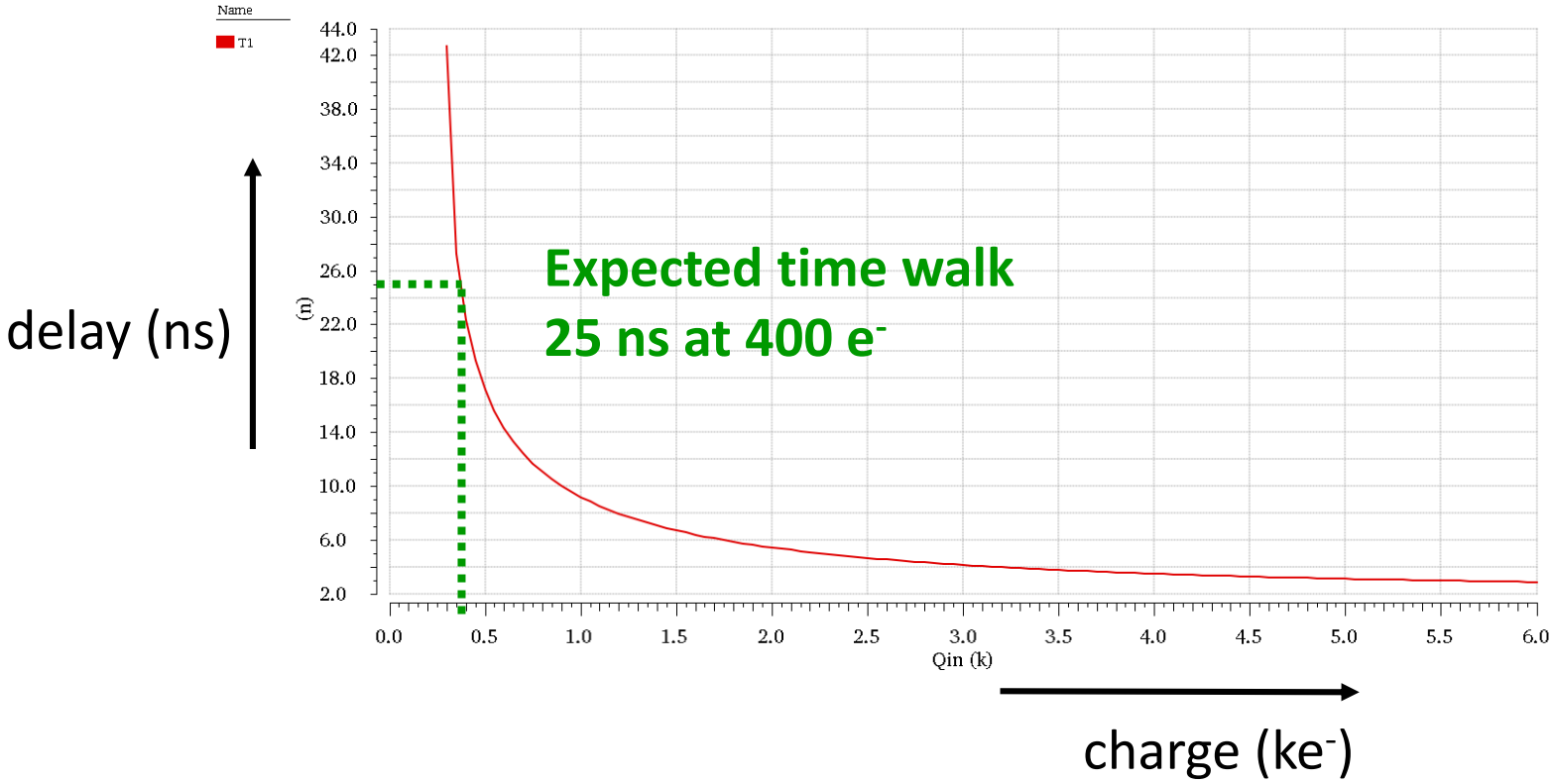
MALTA end of column logic

- Asynchronous signals are merged onto a common bus in the periphery
  - Adjustment for propagation delay in the parallel data bus
  - Column address, time stamp bits added
- Arbitration logic (*Hit merger*) to process simultaneous signals
  - One of the signals is delayed to avoid data collisions
  - Keeping track of the number of delays, additional delay bits
- 40 bit output word
- Asynchronous hit signals transmitted from the chip via LVDS up to 5 Gbps
- Asynchronous readout and slow control with custom readout firmware using Xilinx Virtex-7 VC707 FPGA kit



MALTA charge measurement

- Charge measurement from time difference between bunch crossing time and leading edge of hit signal
- Simulation: Time walk of 25 ns corresponds to 400 e^-



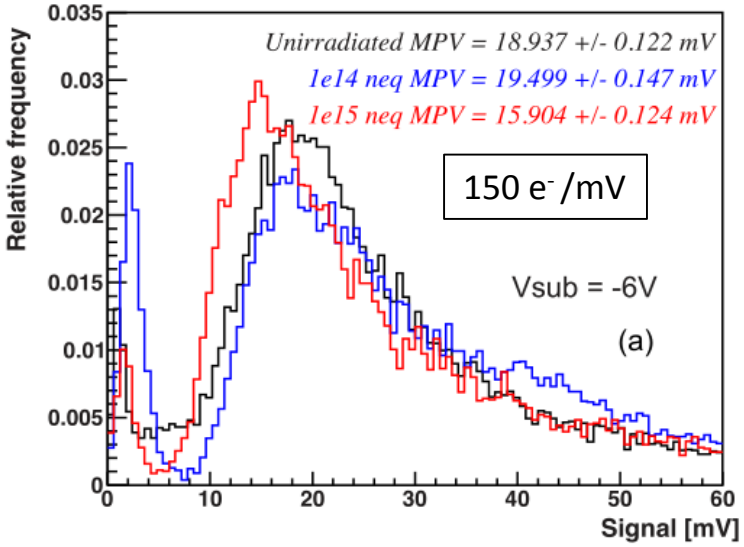
MALTA status

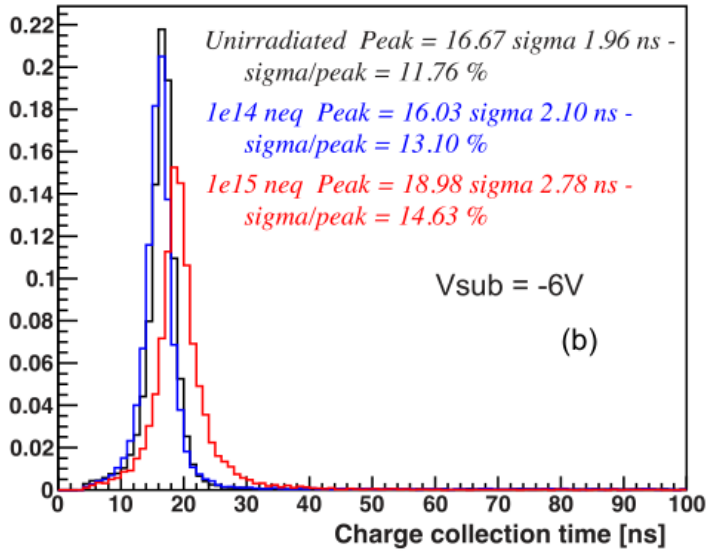
- First submission – chips received Jan 2018
  - Pixel readout and pixel pulsing functional
  - Slow control not fully functional – masking only on double column level, no individual pixels
  - Hit merger in the periphery disabled due to too high noise activity → can cause data collisions
- Second submission (MLVLC) – chips received Jul 2018
  - Modifications aimed at improving ohmic connections in slow control and powering with minimal number of masks
  - Chip behavior remained similar to first submission

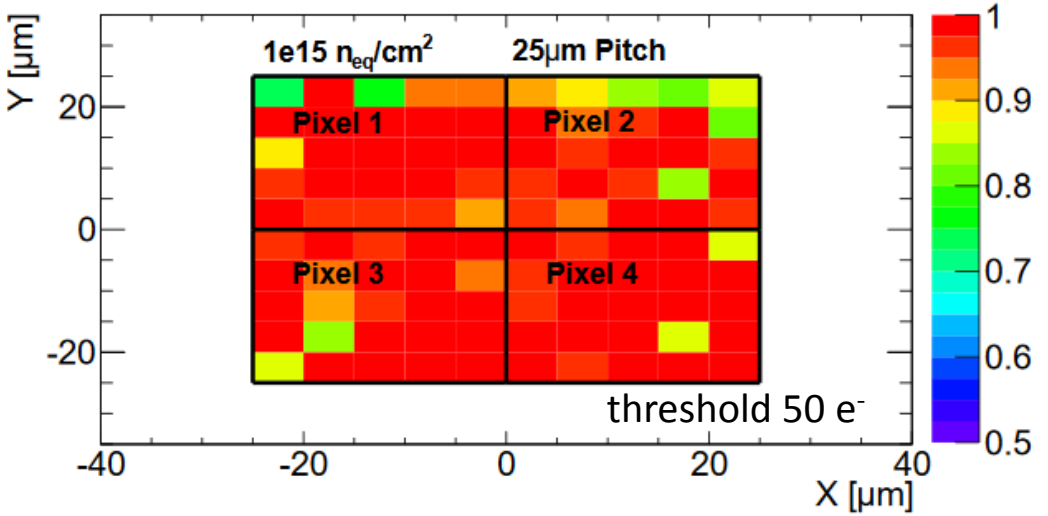
- Future submissions: Mini MALTA – submitted Aug 2018 (MPW)
  - Smaller 64 x 16 pixel chip with additional functional blocks
  - Slow control redesigned to achieve correct masking, pixel tuning
  - Additional synchronization circuit in the periphery to compensate pixel delays at the end of column

TESTING

TJ Investigator results summary





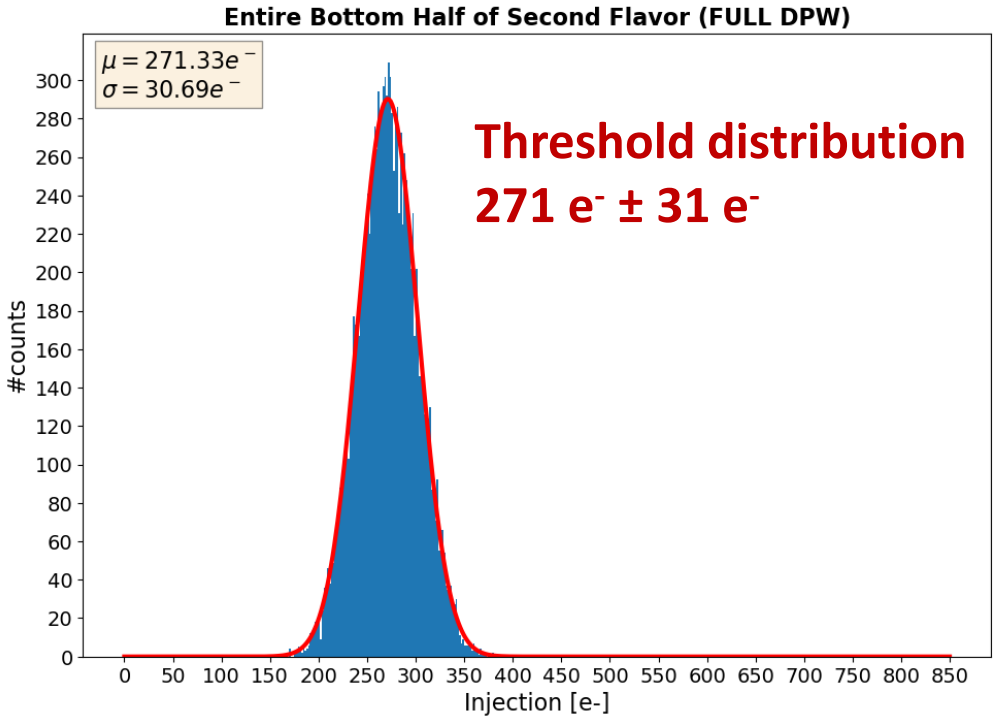


H. Pernegger et al 2017 JINST 12 P06008

- Analog output from the front end
- Good sensor and front end performance after 1e15 n_{eq}/cm^2 neutron irradiation*:
- ^{90}Sr measurements:
  - < 20 % drop in signal MPV: 18.9 mV → 15.9 mV
  - Charge collection time 19.0 ns ± 2.8 ns
- Test beam (SPS 180 GeV/c pions, FEI4 beam telescope, 9 µm pos. resolution):
  - Uniform 98.5 % efficiency within 25 µm pixel (smaller than MALTA)

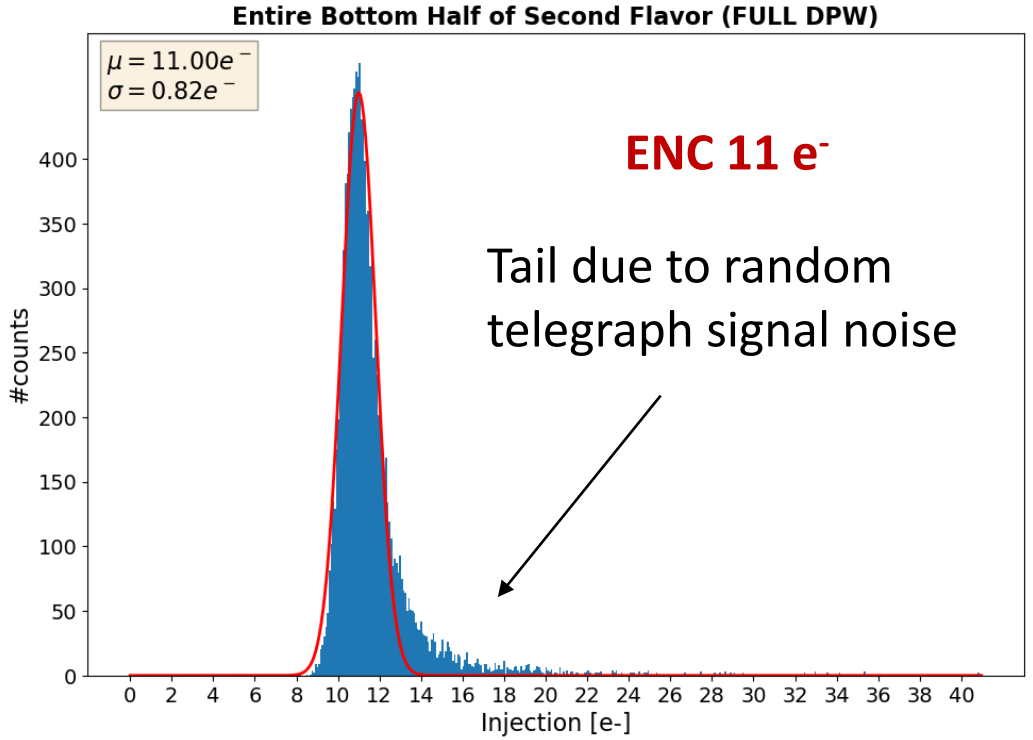
*All neutron irradiations made at Ljubljana TRIGA reactor

Threshold scan – TJ MonoPix



Threshold distribution
271 e⁻ ± 31 e⁻

TJ MonoPix
before irradiation



ENC 11 e⁻

Tail due to random
telegraph signal noise

- Threshold measurement in MALTA not trivial (no masking)

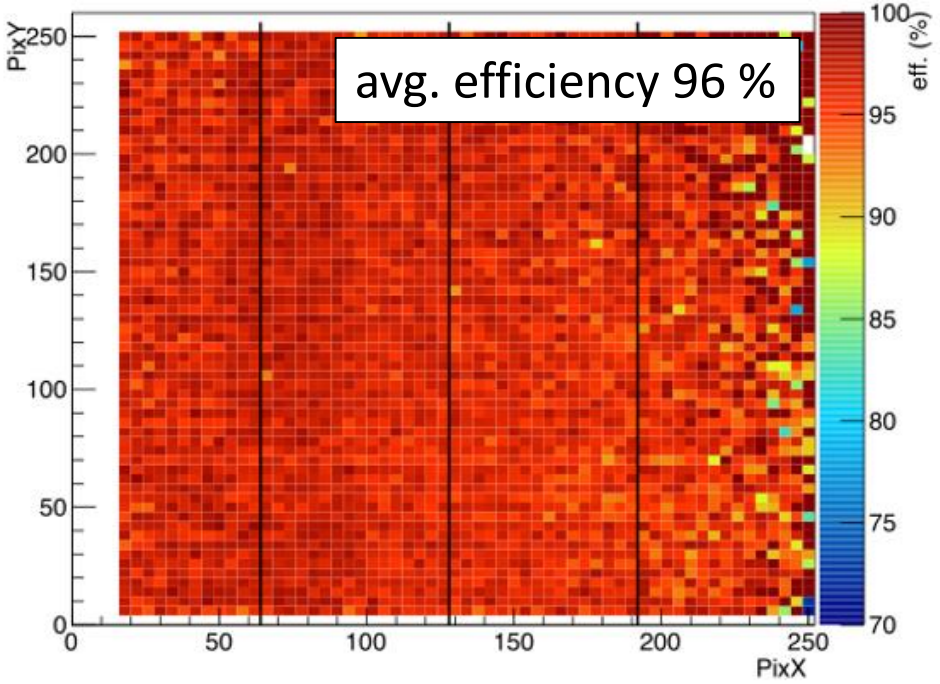
K. Moustakas et al, arXiv:1809.03434

- MonoPix: Measurement of S-curves by injecting test charge into front end
- Before irradiation: thr. 271 e⁻ ± 31 e⁻, ENC 11 e⁻
- After irradiation: thr. 470 e⁻ ± 50 e⁻, ENC 20 e⁻ (1.5e15 n_{eq}/cm^2 neutrons, 1 Mrad TID)
- Increase in noise may require in-pixel threshold adjustment
- Extracted values in MALTA compatible with MonoPix

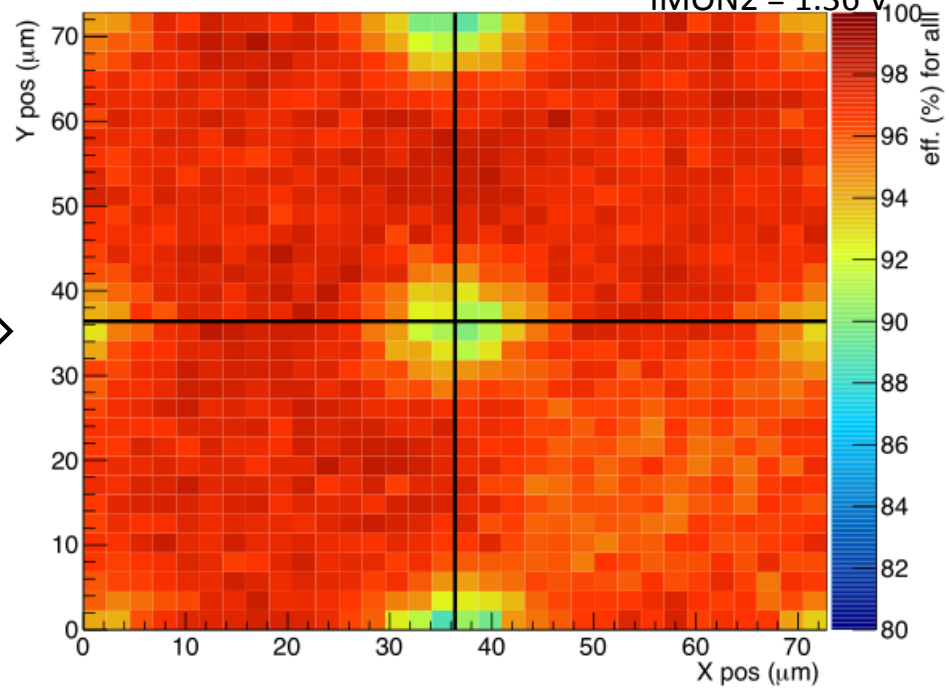
MALTA test beam

- SPS test beam, 180 GeV/c pions, Mimosa beam telescope, 5 µm position resolution https://doi.org/10.1016/j.nima.2014.05.033.
- Before irradiation: avg. efficiency 96 % (less in corners)
- Efficiency loss due to noise
  - Merger circuit and pixel masking not available
  - Track hit and a noise hit arrive simultaneously (within 1 ns)
  - Data is misinterpreted as a hit coming from another pixel → not matched with telescope track

Efficiency map (unirrad.)

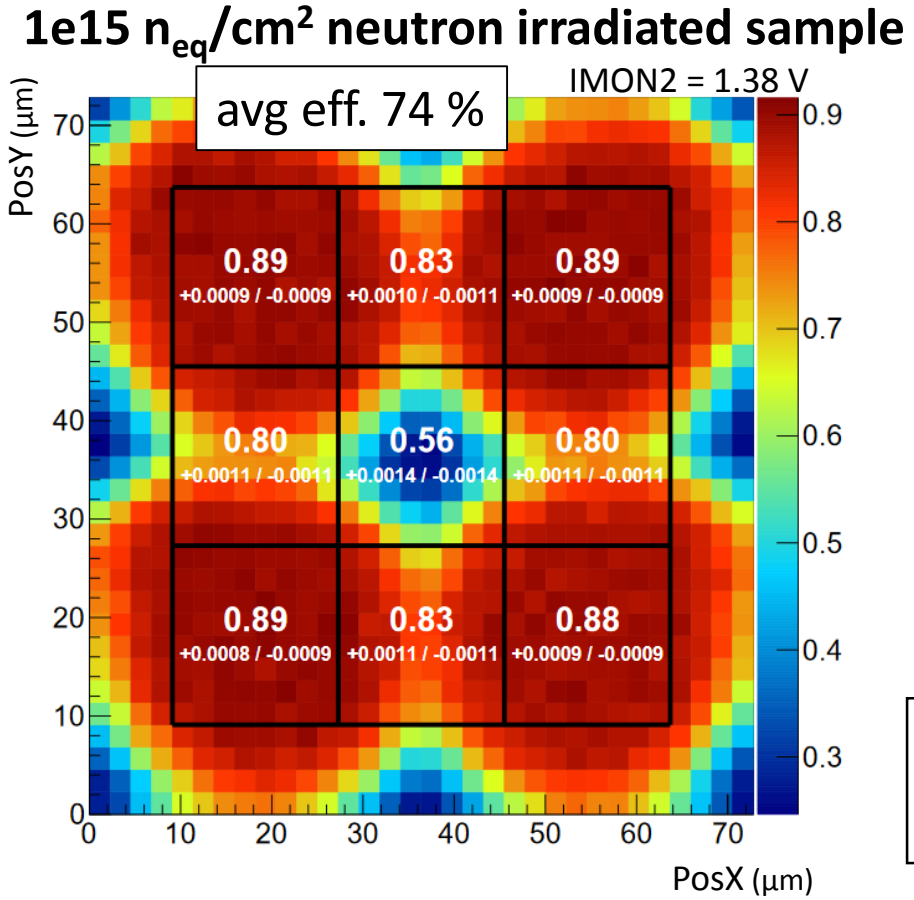


In-pixel efficiency (unirrad.)

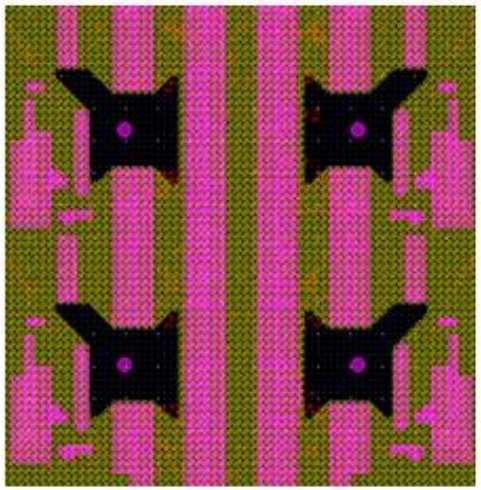


Optimal HV bias configuration
SUB -15 V, PWELL -6 V

MALTA test beam irradiated



Deep PWELL distribution



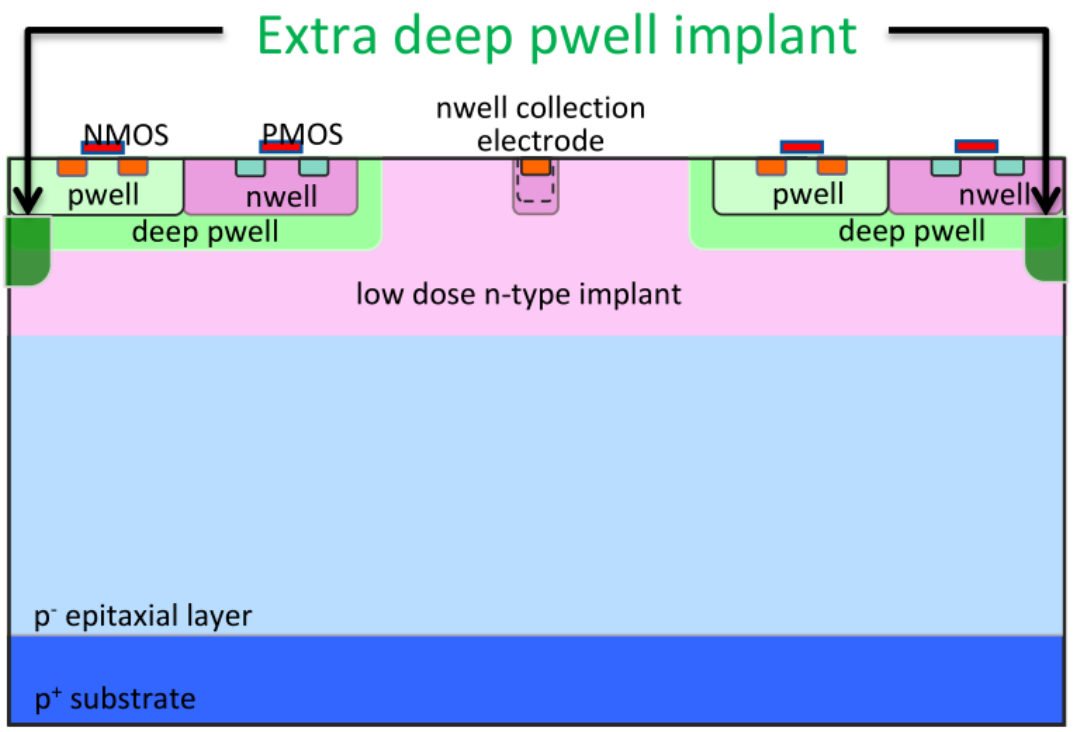
Low threshold
inefficiency due to noise

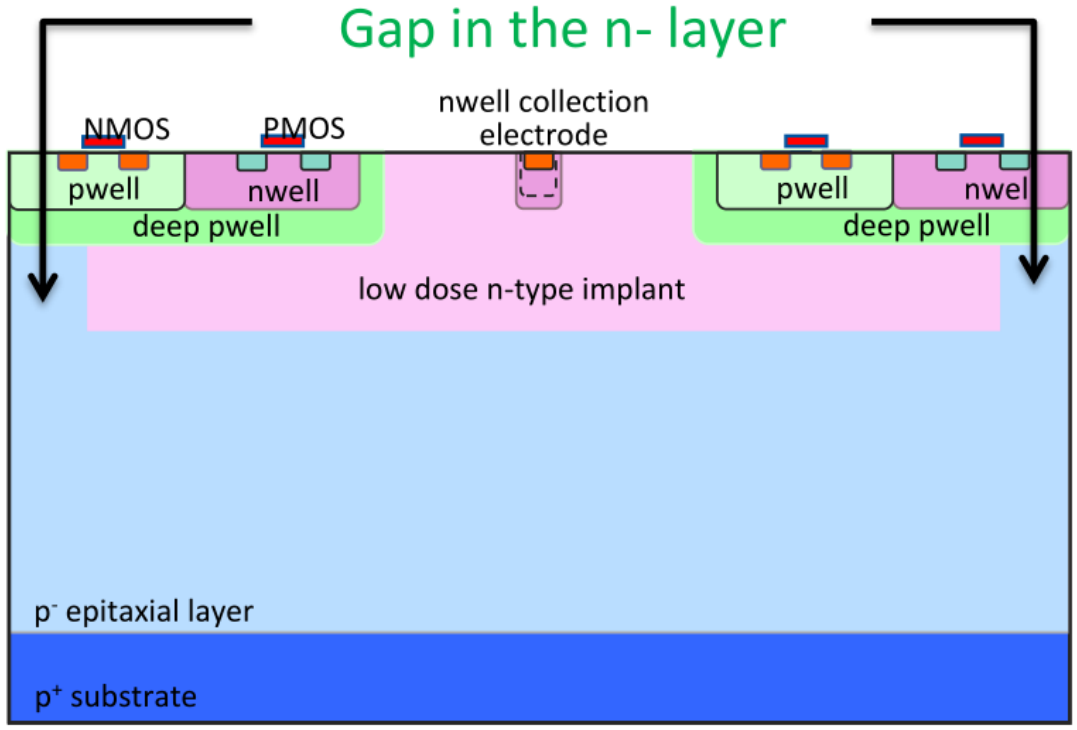
⟺

High threshold
inefficiency for low signals

- Critical efficiency loss in pixel corners after irradiation
  - Noise increases in irradiated samples → higher threshold required to suppress noisy pixels (no masking/merging !)
  - **Threshold too high** to detect hits on pixel edges (charge sharing)
- Inefficiency in the centers due to a high noise level (efficiency in centers increases at a higher threshold !)
- Efficiency correlated with deep PWELL distribution – inspired modifications discussed with the foundry

Fixes discussed/planned with the foundry





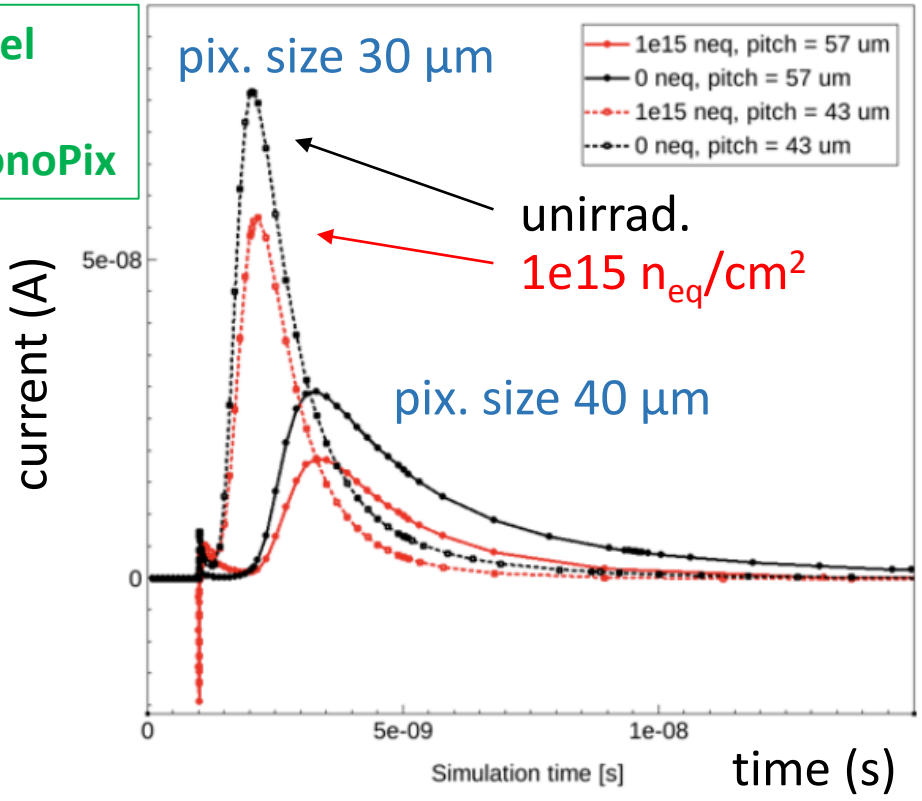
- Additional deep p-type implant
- Requires additional mask, but can use 'known' process step

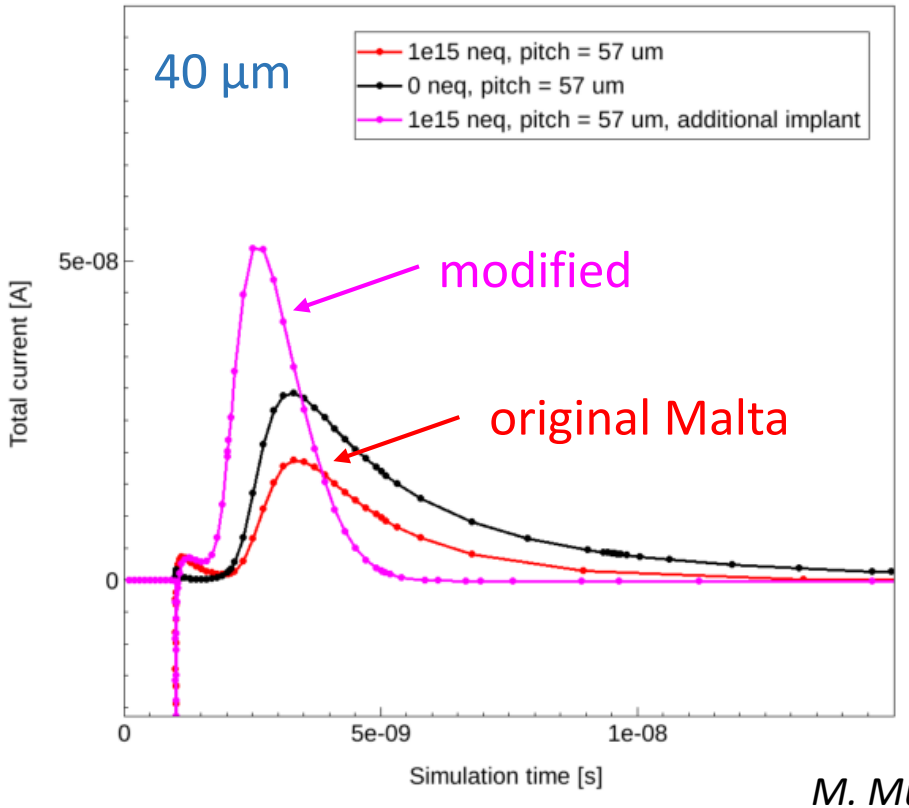
- Creating a gap in the deep n-type implant
- Mask change, no additional mask required

Both changes target modifying lateral electrical field to improve charge collection – TCAD simulation

2D Device simulation

original pixel layout MALTA/MonoPix





Extra deep PWELL implant

Gap in n-layer:
3d simulation required for fully understanding the effects

M. Münker, CLICdp, CERN

- Induced pulses in pixel corner
- Large penalty for increased pixel pitch (slower, smaller pulses)
- Modifications expected to significantly improve charge collection

Summary

- After encouraging results on first prototypes, designed two monolithic CMOS sensors for the ATLAS ITk upgrade with a small low capacitance collection electrode layout for low analog power consumption
  - **Monopix**: more conservative synchronous column-drain readout
  - **Malta**: novel asynchronous readout without clock distribution over the matrix to minimize power (< 100 mW/cm^2)

- Degraded detection efficiency, especially in the pixel corners, due to:
  - Higher threshold spread than expected from simulations,
    further degraded after irradiation
  - Non-gaussian tail in the noise due to random telegraph noise
  - The increased pixel pitch, effect confirmed also by TCAD simulations
  - Slow control issue on Malta
    (unability to correctly mask and therefore large number of noise hits and constraint to stay at higher threshold)

  Degraded efficiency correlated with deep PWELL layout

Malta efficiency

Test beam	Average eff.	Eff. in corners
unirradiated	96 %	90 %
1e15 n_{eq}/cm^2	75 %	< 40 %

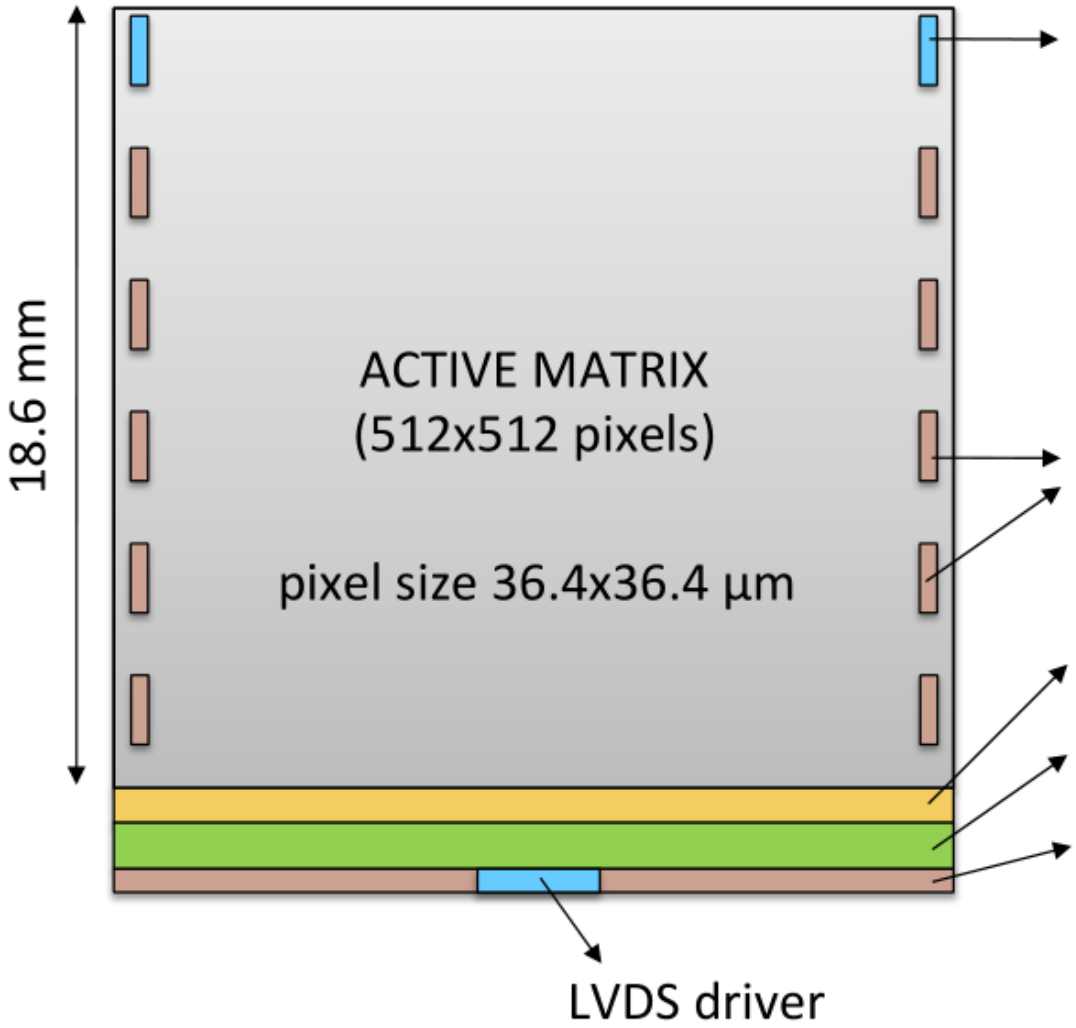
- This initiated:
  - Development of threshold tuning and front end study (not yet completed)
  - Collaboration with the foundry and extensive TCAD simulations to improve charge collection by mask or process modification and submission of a MiniMalta test chip in an MPW including a first version of these fixes in August

Acknowledgements

- We thank TowerJazz for their constructive collaboration
- This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.
- The authors acknowledge the financial support from the Slovenian Research Agency (research core funding No. P1-0135 and project ID PR-06802).

BACKUP

MALTA chip



CMOS input/output pads

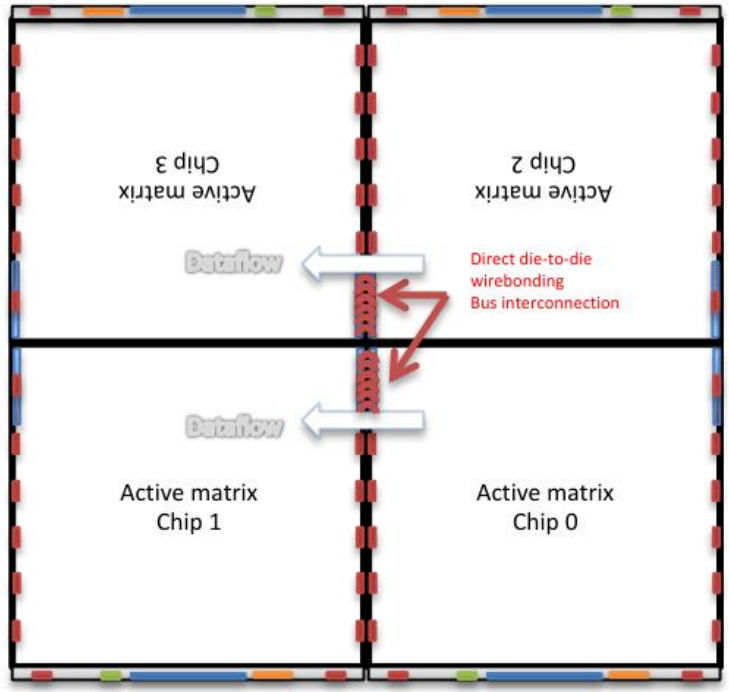
- 8 sectors (different collection electrode size and deep PWELL spacing)

power pads
allow chip-to-chip bonding

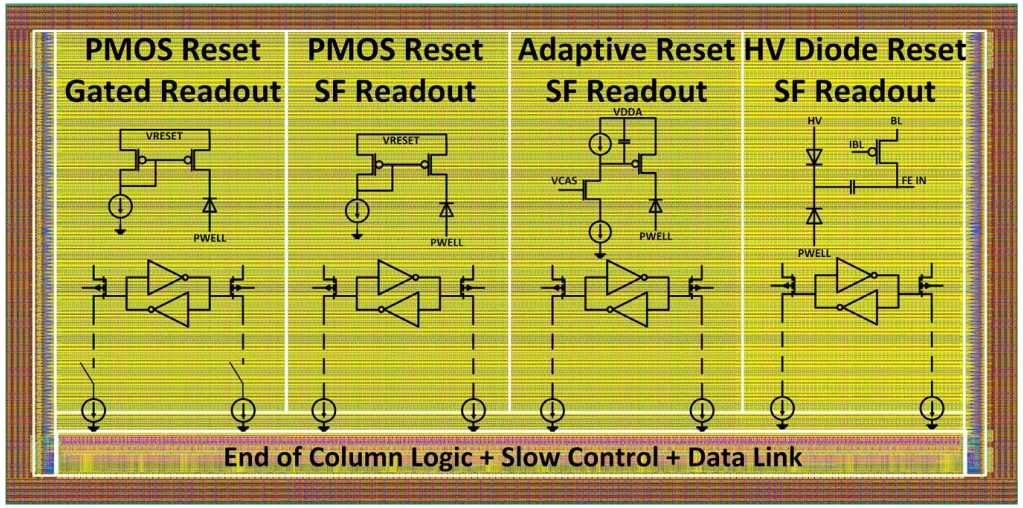
DACs for analog biases

digital periphery

regular pads



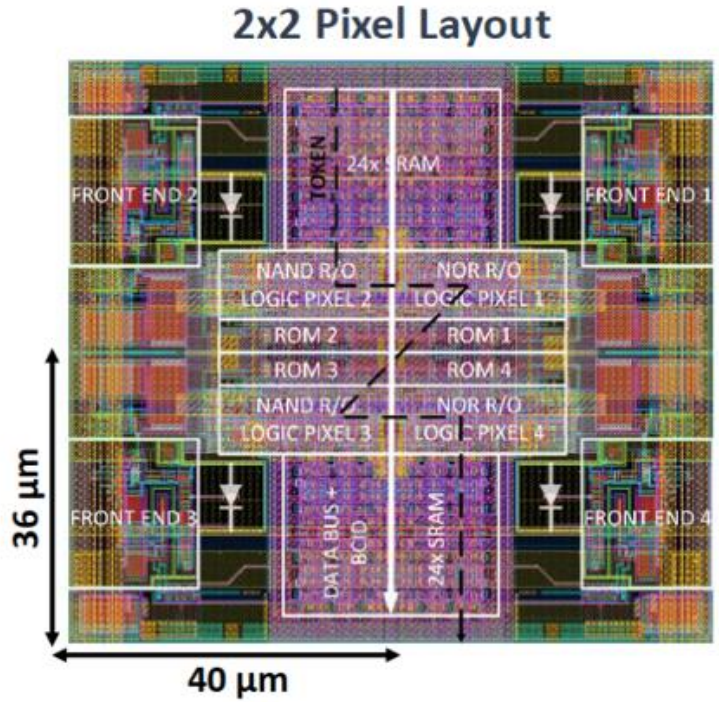
TJ MonoPix



- 1 x 2 cm^2 chip (224 x 224 pixels)

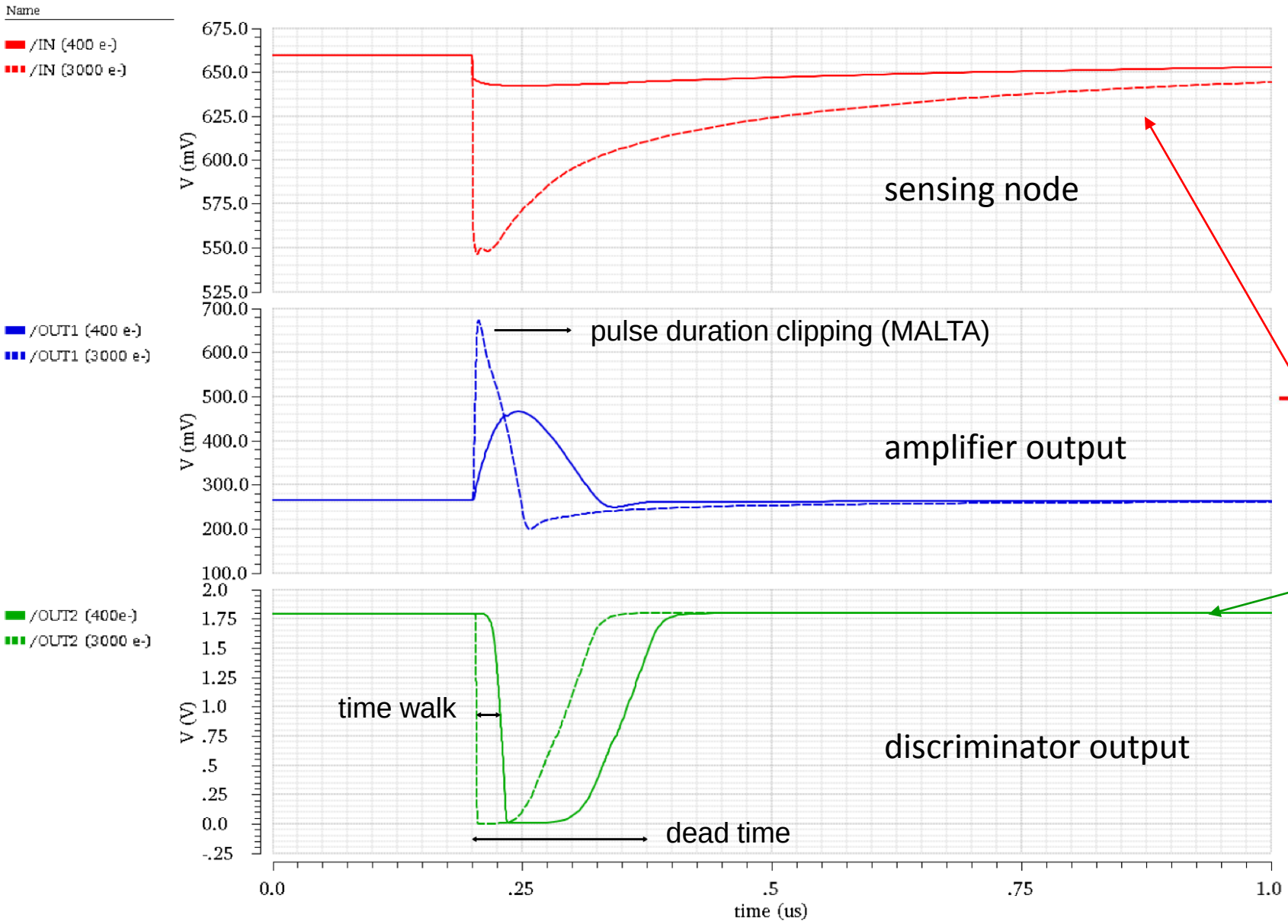
  T. Wang et al 2018 JINST 13 C03039

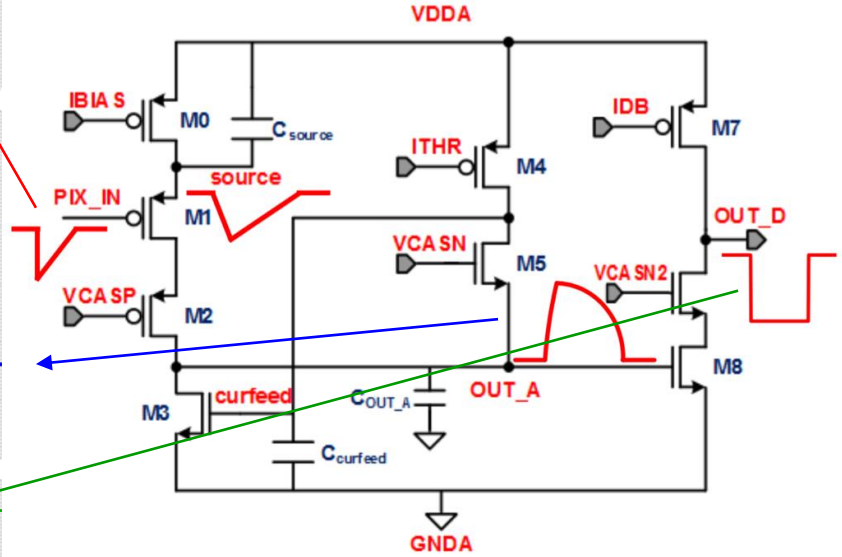
- Column drain readout
- 4 sectors with different pixel flavors
  - Improved low power column bus readout
  - Standard PMOS input reset
  - Adaptive input reset (leakage compensation)
  - Frontside HV biased, AC coupled pixels



- Pixel size 36 µm x 40 µm
- Low threshold dispersion, no in-pixel tuning
- ToT charge information
- Analog power < 1 µW per pixel (65 mW/cm^2)
- Digital power (Layer 4) ≈ 100 mW/cm^2

Front end optimization (simulation)





*I. Berdalovic et al 2018 JINST **13** C01023*

Adaptive PMOS reset

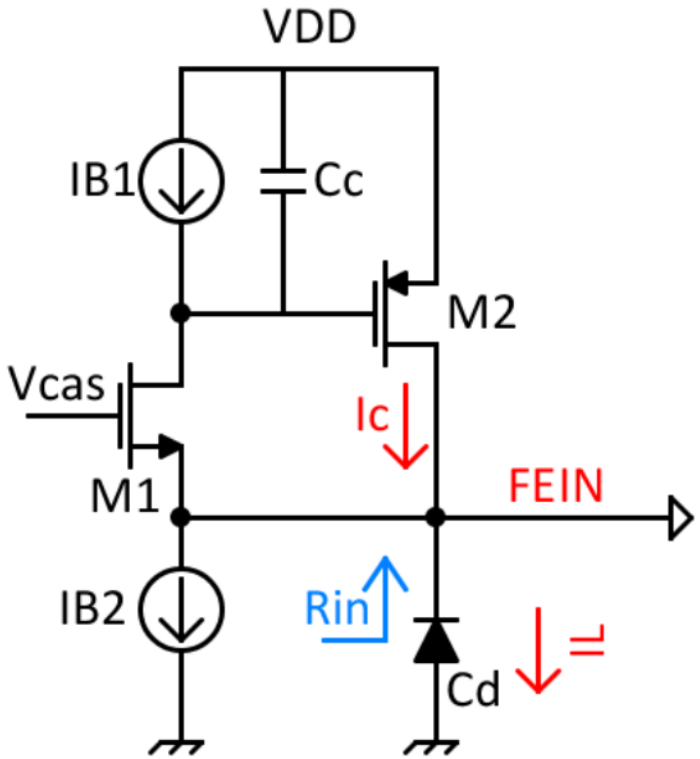
Circuit for reseting input in some pixel flavors

At high frequencies (hit)

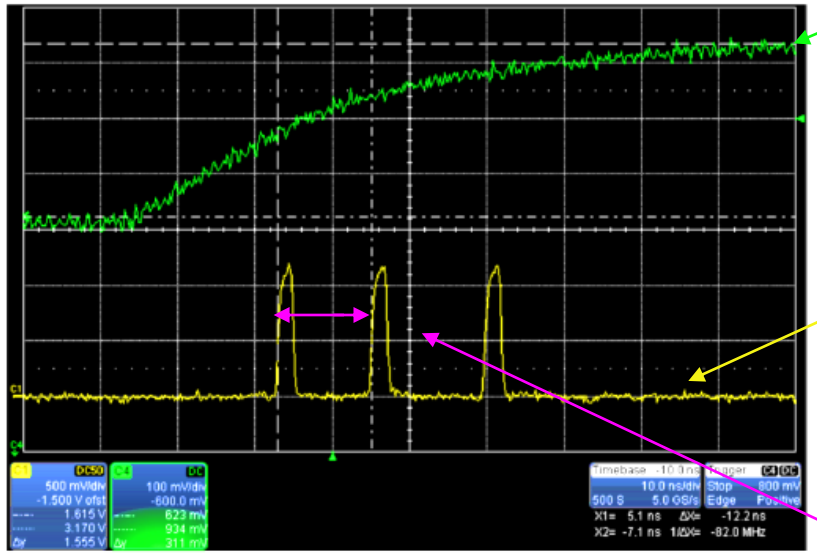
- fast input Reset
- adjustable

At low frequencies (leakage)

- Low frequency feedback
- Compensate for I_L
- Stability has to be guaranteed



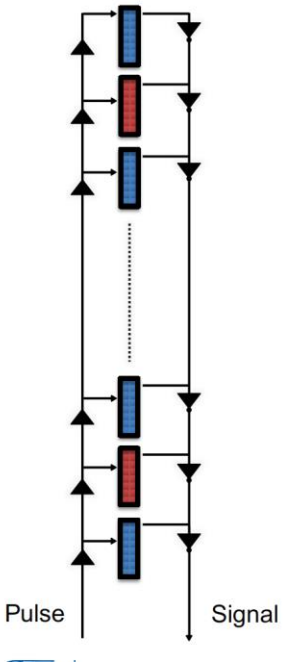
MALTA propagation delay



analog output of one of the pulsed pixels

Reference signals (asynchronous 2 ns pulse for each hit)

Measured delay between first two pulses 12.2 ns

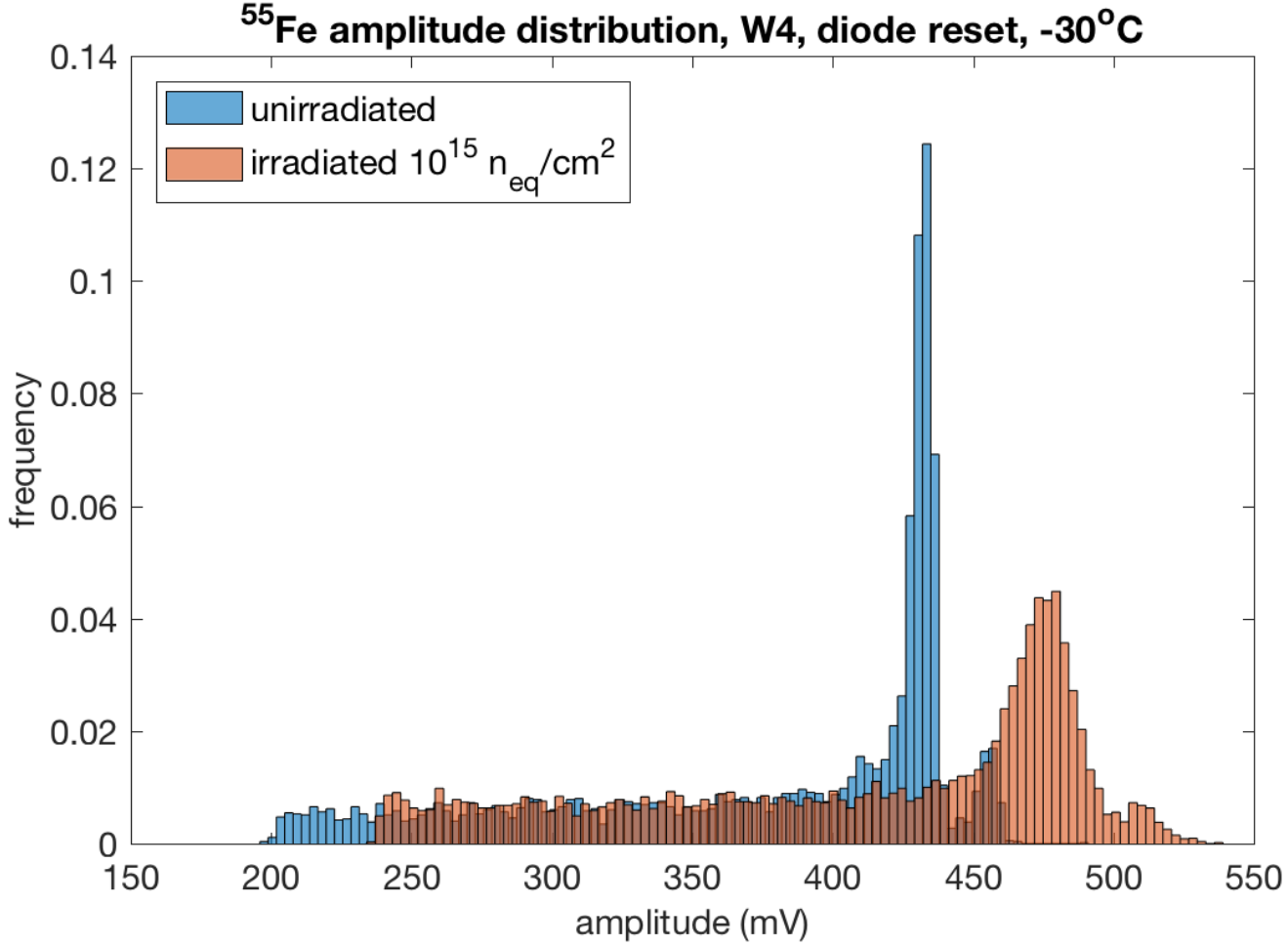


P-well bias	Simulation	2 groups [ps]	Column [ns]
0V	Pulse delay	460	14.75
	Signal delay	225	7.20
-0.5V	Pulse delay	478	15.29
	Signal delay	234	7.48
-1V	Pulse delay	490	15.68
	Signal delay	241	7.71
-1.5V	Pulse delay	503	16.10
	Signal delay	246	7.87
-1.8V	Pulse delay	511	16.35
	Signal delay	249	7.70

- Total delay for half a column = pulse delay / 2 + + signal delay / 2 = **12 ns** (-1.8 V p-well bias)

- Propagation delay of asynchronous signals through double column bus up to 8 ns

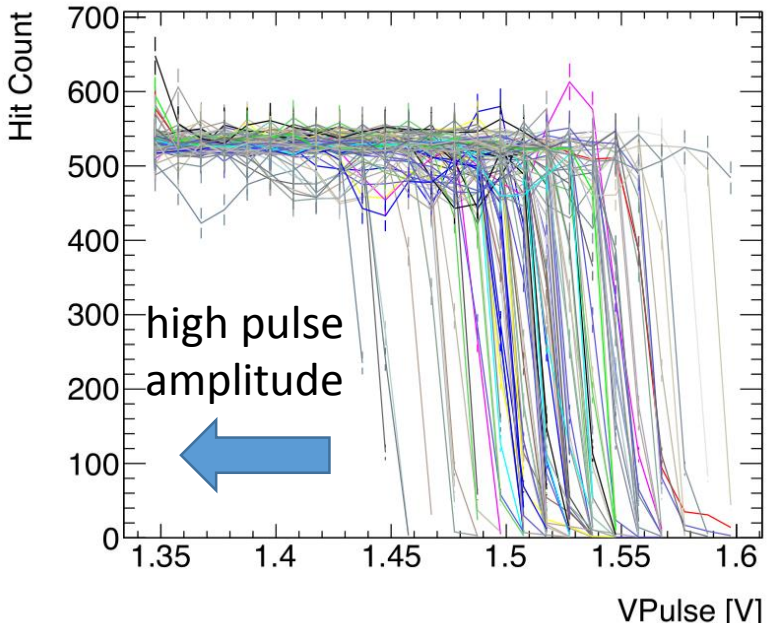
MALTA ^{55}Fe spectrum

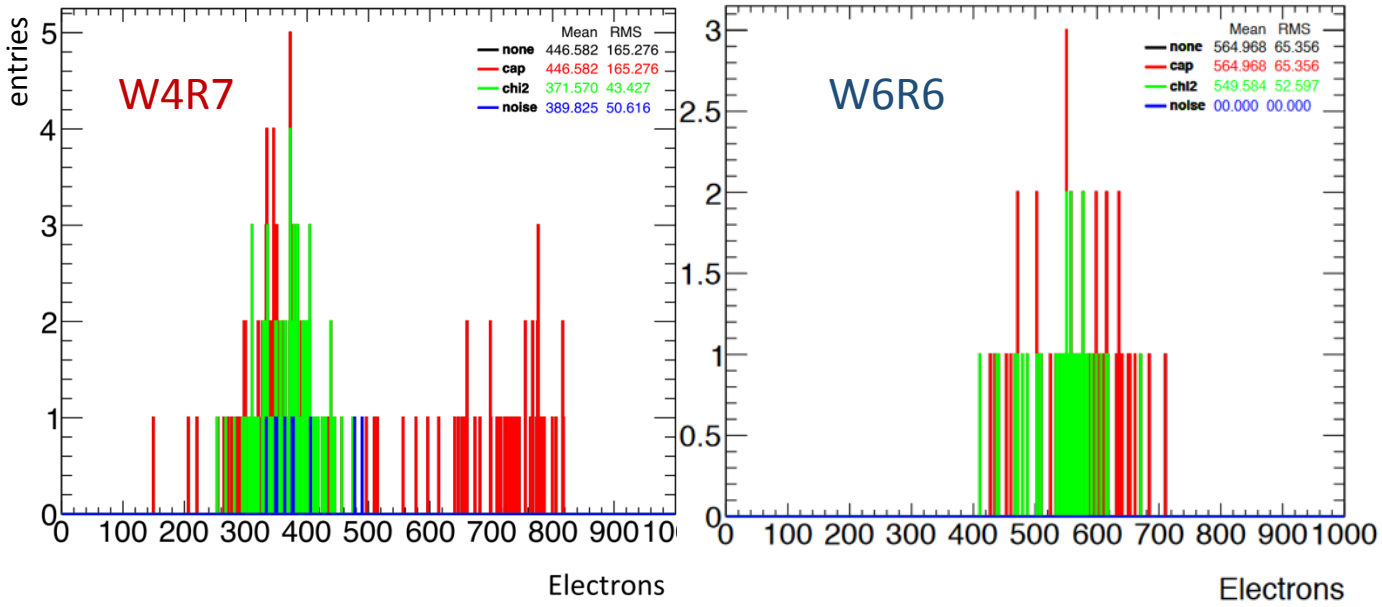


- Analog output from the front end
- Separation between K_α and K_β lines before and after irradiation
- Front end configuration not the same → signal size not directly comparable

MALTA threshold

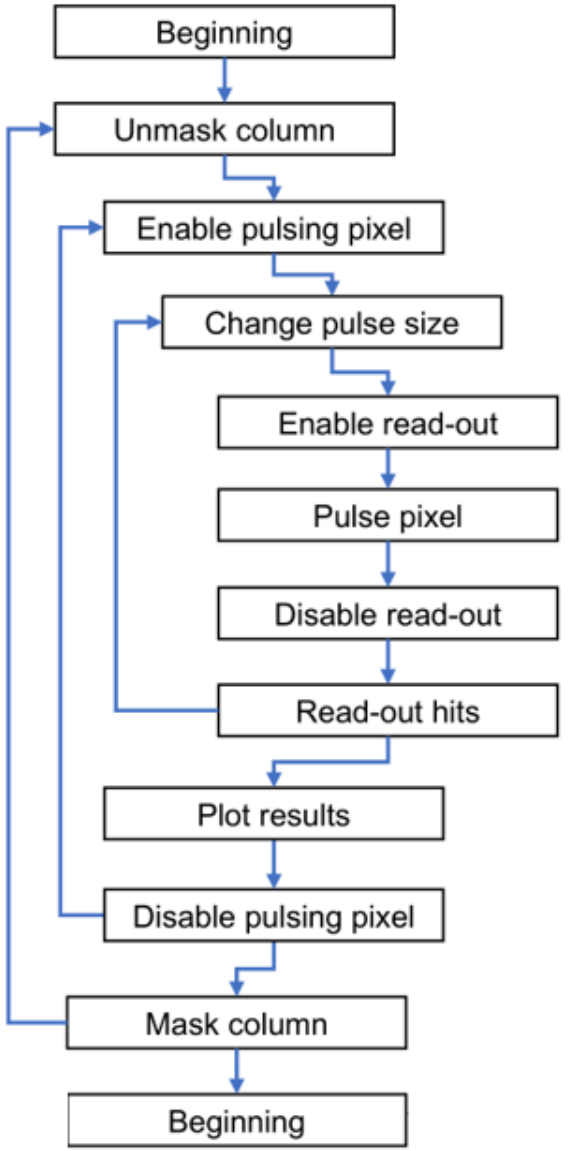
- Measurement of S-curves by electronically injecting charge in the front end
  - Charge calibration calculated from injection capacitance
- Without fully functional slow control difficult to measure correctly
  - Fit error function and make a χ^2 cut on fit quality
  - Analyzing only S-curves which passed the cut
- Samples (unirradiated):
  - W4R7 – Jan 2018
  - W6R6 – Jul 2018
- Thresholds
  - 371 e^- ± 43 e^- (W4R7)
  - 550 e^- ± 53 e^- (W6R6)
  - 10 % threshold spread
  - calibration verification necessary, f.e. ^{55}Fe
- After irradiation noise level increases substantially





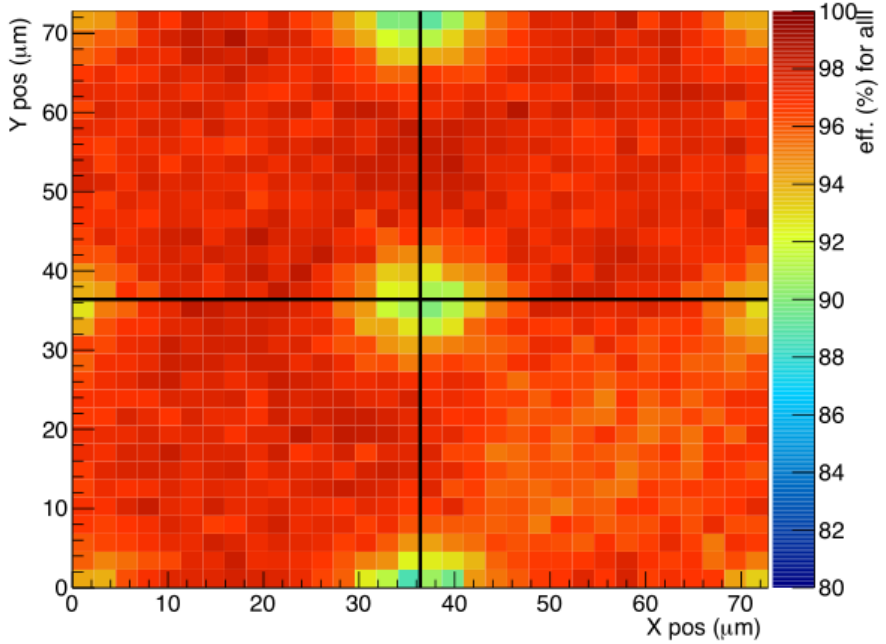
MALTA threshold scan

- Chip status
  - Merger is disabled, therefore high traffic in the output will resolve in incorrect reconstruction
  - Each slow control command is preceded by lowering VDD to 1.2V and followed by raising VDD to 1.8V
  - Cannot mask top half pixels
  - Fixed threshold settings (IMON2=1.3 V)
- Algorithm
  - Mask all the chip
  - Unmask selected column
  - Enable pulsing on selected pixel up to row 20
  - Change pulse size
  - Enable read-out, pulse, disable read-out
    - Repeat 500 times
  - Readout all hits in buffer
  - Only selected pixel + row 251 and 511 should respond

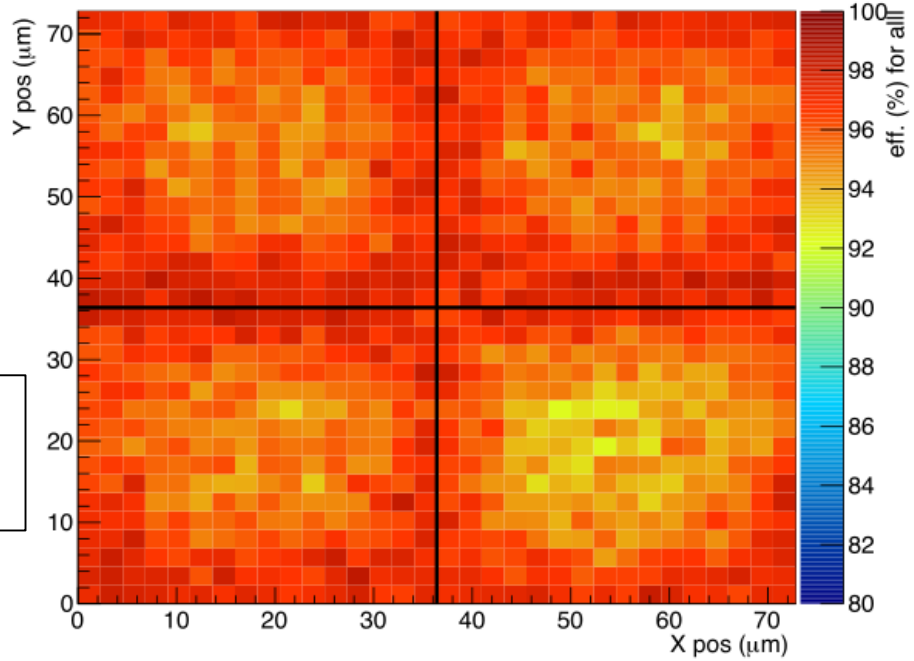


MALTA test beam unirradiated

In-pixel efficiency map (2 x 2 pixels), unirradiated, low threshold



Optimal HV bias configuration
SUB -15 V, PWELL -6 V



Sample W4R7 (Jan 2018)

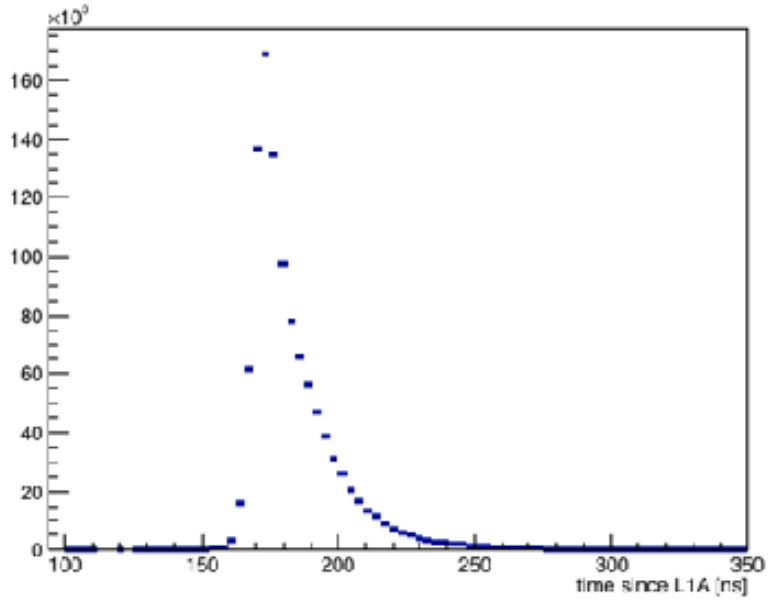
- Lower (90 %) efficiency in corners
- Overall efficiency > 96 %

Sample W6R6 (Jul 2018)

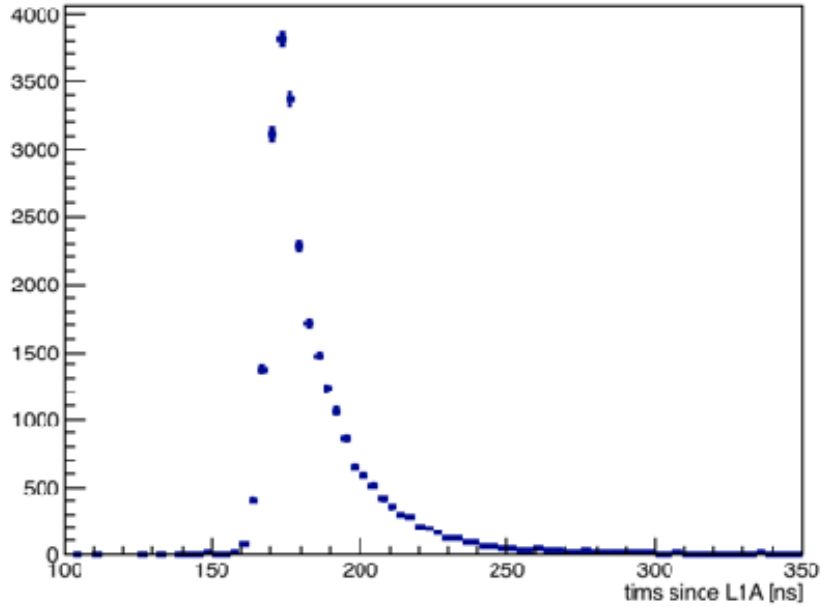
- Lower (93 %) efficiency in centers
  - Threshold is lower
  - Efficiency loss in center due to noise
  - Shared hits on edges – higher probability to detect at least one of two hits
- Overall efficiency > 96 %

Discrepancy between samples likely due to difference in threshold level, since process is unchanged

MALTA hit timing



unirradiated sample



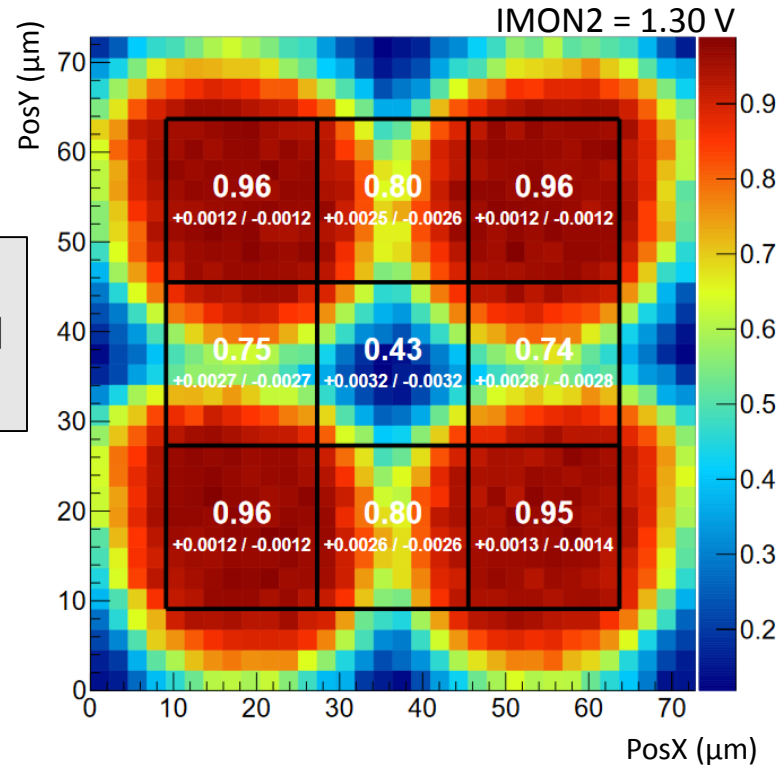
- Time of arrival for hits **matched** with a track
  - Peaked distribution as expected
  - In-time efficiency ignored for now
- Time of arrival for hits **not matched** with a track
  - For noise expecting **uniform** distribution
  - Indicates false hit reconstruction due to data collisions (merger circuit is disabled !)

Detection efficiency can be increased by improvement of electronical sector
- Masking individual pixels → remove noisy pixels
- Per pixel threshold tuning ?
- Merger circuit

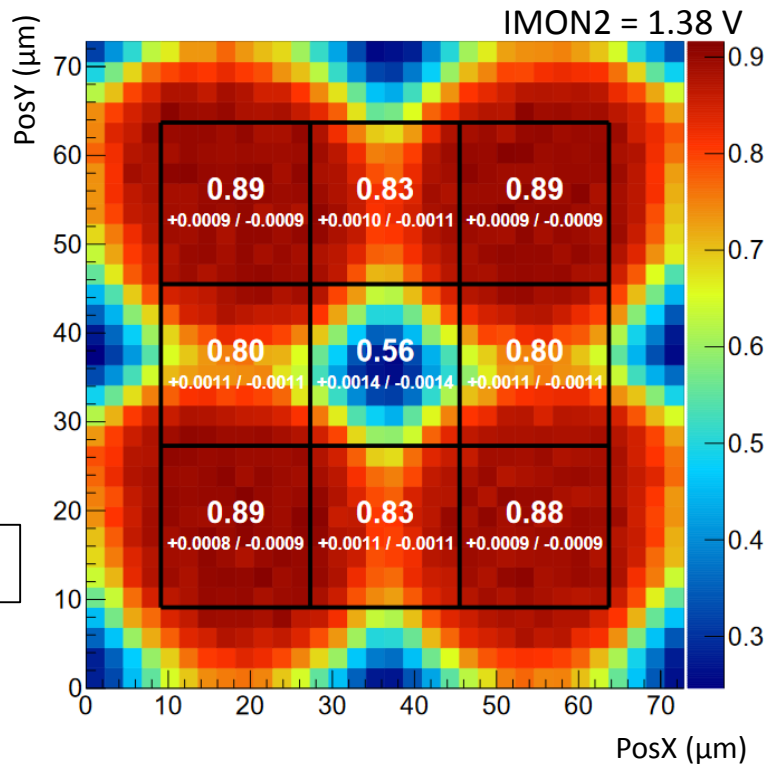
MALTA test beam irradiated

1e15 n_{eq}/cm^2 neutron irradiated sample (first submission)

(moderately) high threshold avg eff. 72 %



2 x 2 pixels



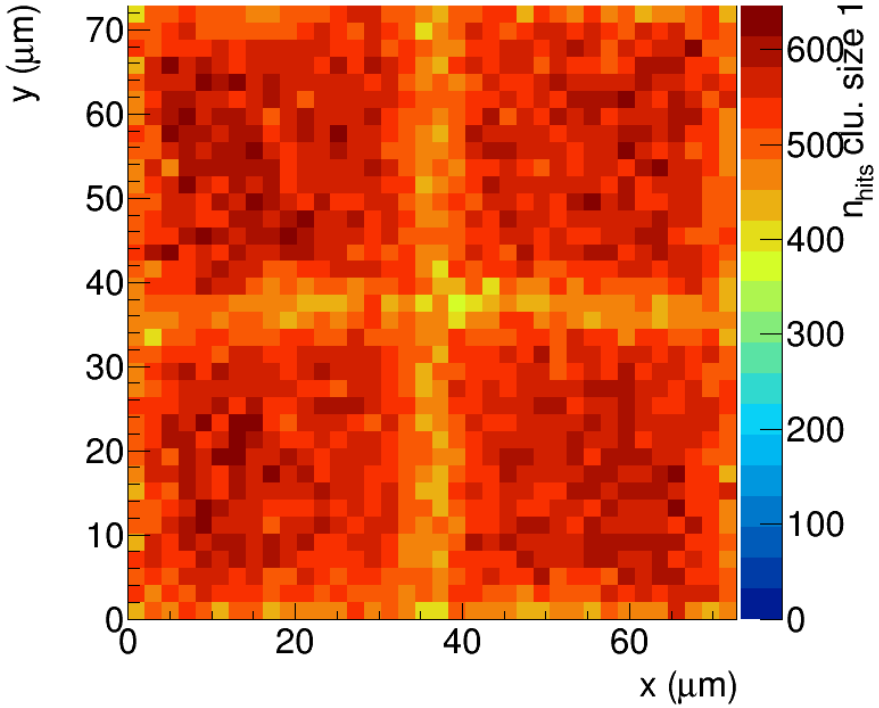
low threshold avg eff. 74 %

At a higher threshold:

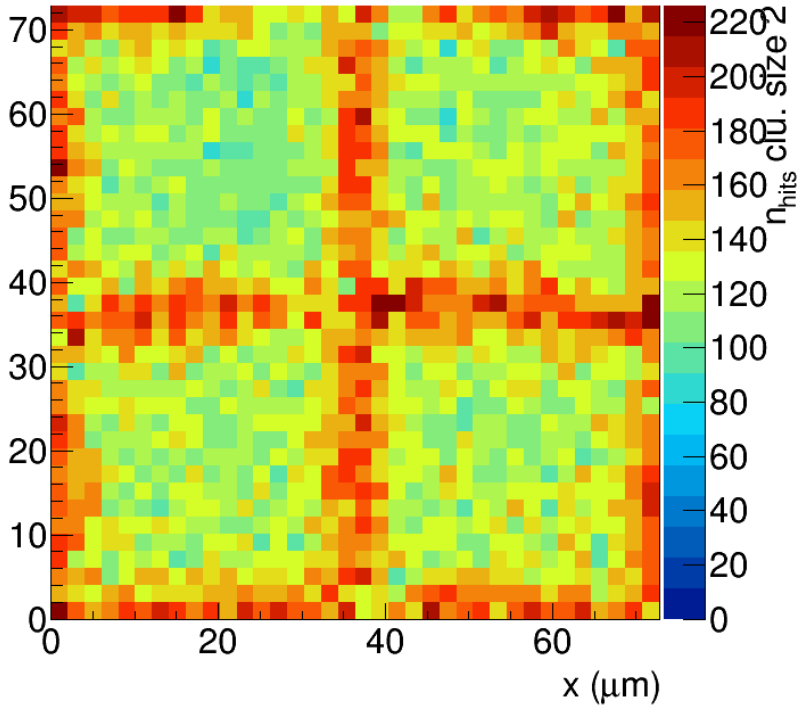
- Efficiency in corners reduces (expected)
- Efficiency in centers **increases**: Lower noise level → smaller probability for data collisions due to disabled merger

MALTA test beam irradiated

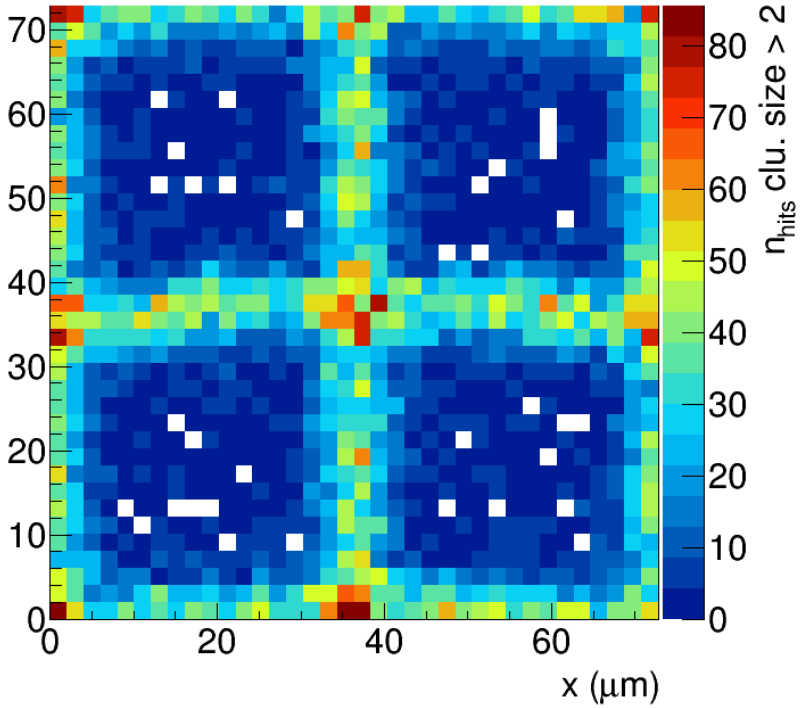
In-pixel cluster size



Cluster size 1



Cluster size 2

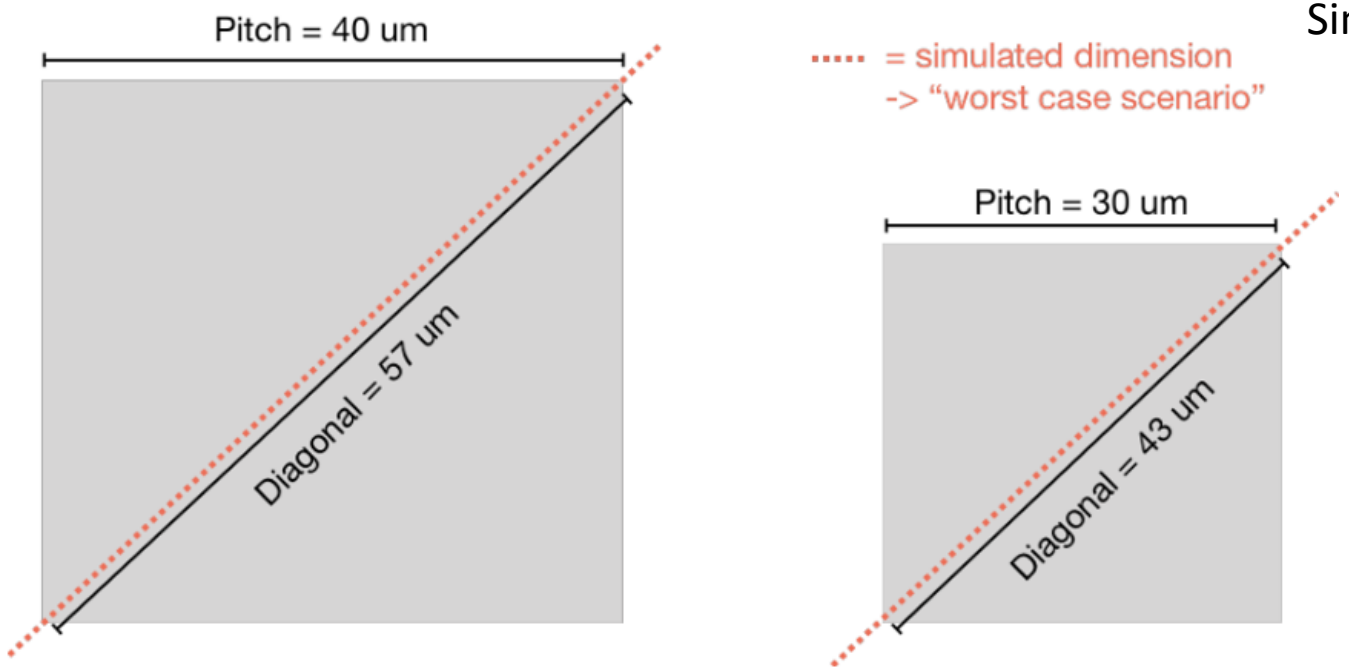


Cluster size > 2

1e15 n_{eq}/cm^2 neutron irradiated sample (first submission)

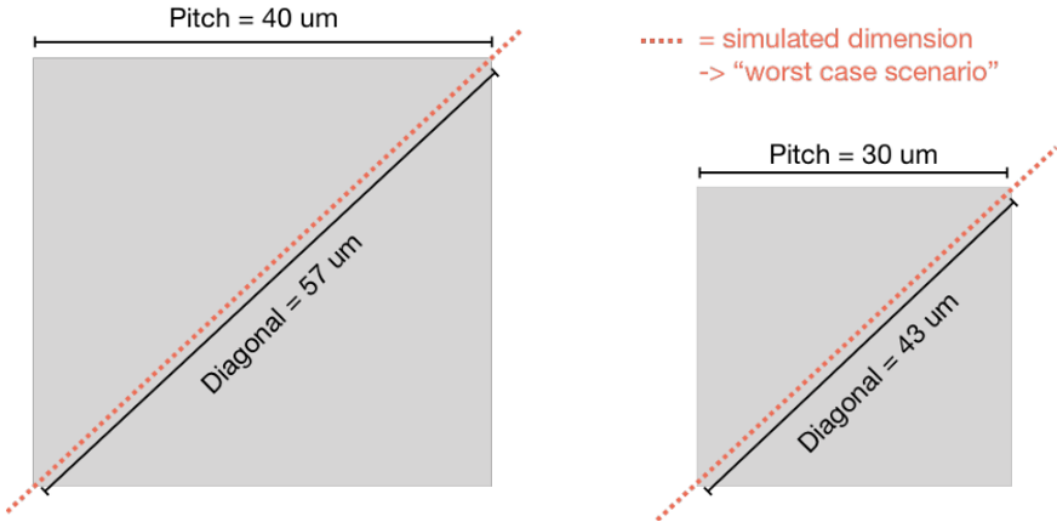
Device simulation

Simulation by M. Münker, Bonn



- First TCAD Simulation of charge collection after irradiation
- 2D simulation for simplicity, 3D in progress
  - Simulation in the plane on the diagonal between two pixels ("worst case")
  - Charge injected in the corner between four pixels

Device simulation model




```
Physics ( material = "Silicon" ) {
    Traps (
        ( Acceptor Level fromCondBand Conc=@<fluence*1.613> @ EnergyMid=0.42 eXsection=1E-15 hXsection=1E-14 )
        ( Acceptor Level fromCondBand Conc=@<fluence*0.9> @ EnergyMid=0.46 eXsection=5E-15 hXsection=5E-14 )
        ( Donor Level fromValBand Conc= @<fluence*0.9> @ EnergyMid=0.36 eXsection=3.23E-13 hXsection=3.23E-14 )
        # fromCondBand: relative to the conduction band
        # Conc: N_0 of radiation level (different energetic distributions of traps, e.g. exponential)
        # EnergyMid: defines the energy level with respect to the defined reference level (in this case relative to the conduction band)
        # The factors after the fluency are the "introduction rate" -> rate of defect levels produced for a certain dose)
}
```

Parameters (from: IEEE Trans.Nucl.Sci. 63 (2016) 2716-2723, DOI: 10.1109/TNS.2016.2599560)