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COLDATA PLL and Serializer: A 2.56GHz Phase Locked Loop (PLL) and a 1.28Gbps 10:1 Serializer Capable of Operating at Cryogenic Temperature

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We report the design, implementation, and measurement results of a 2.56 GHz PLL (COLDATA PLL) and a 1.28 Gbps 10:1 serializer (COLDATA SER) IC in a 65 nm CMOS process as part of the COLDATA prototype IC for the Deep Underground Neutrino Experiment (DUNE). The PLL employs a trip-path architecture with a temperature compensated path to achieve small VCO frequency drift, stable bandwidth and low jitter across a wide temperature range. The measurement results demonstrated that the PLL and SER IC can operate and achieve the targeting performance at both room temperature (300K) and cryogenic temperature (77K).

Summary

The COLDATA chip is a data concentrator operated in liquid argon at cryogenic temperature (77K). It sends the recorded data from multiple front-end integrated circuits (IC) out of the cryostat for Long Baseline Neutrino Facility (LBNF) and the Deep Underground Neutrino Experiment (DUNE). At the center of the COLDATA chip are a phase-locked loop (PLL) and sterilizers which serialize 128 Mbps 10-bit wide parallel input data (such as 8b10b, prbs15, prbs31) into single serial stream at 1.28 Gbps.

A key design concern of the PLL is the frequency drift of the VCO and its stability over large temperature variation. Because the on-chip inductors and capacitors are highly sensitive to the temperature variations, any change of the chip temperature would cause the VCO oscillation frequency to drift, and eventually drive the PLL out of lock. Therefore, PLLs with frequency compensation capability and high reliability are highly demanded. We designed a novel triple-path PLL (TPPLL) to compensate the VCO frequency drift caused by the large temperature variations meanwhile maintaining a stable bandwidth and good jitter performance. The proposed PLL architecture splits the VCO tuning loop into three paths as proportional, the integral, and the temperature compensation (TC) paths, respectively. The feed-forward TC path with a large VCO gain but a small bandwidth is adopted to realize the compensation for the VCO frequency temperature drift in a closed-loop manner without affecting the high-frequency performance of the VCO. The fixed control voltage on the proportional path and limited control-voltage variation on the integral path desensitize the VCO gain (KVCO) non-linearity and stabilizes the loop bandwidth over large temperature range. The small VCO gain on the proportional and integral paths contributes to low phase noise and spurs.

The 2.56 GHz COLDATA PLL and 128 Gbps 10:1 COLDATA SER were designed and implemented using 65nm CMOS process. The core circuits of the PLL occupy an area of 0.08 mm2, and the SER occupies an area of 0.01 mm2. The total power consumption of the PLL and SER is 9.8 mW. The silicon measurement results show that the PLL and the serializer can continuously work (without calibration) when the temperature changes from 300 K down to 77 K. The measured random jitter of the PLL output is 0.89 ps at 300 K, and 0.42 ps at 77 K. The measured random jitter of the serializer output data stream is 1.42 ps at 300 K, and 0.63 ps at 77 K with 8b10b encoded data stream as the input.

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