cpVLAD, a 10-Gbps per channel, 4-channel VCSEL array driver with an on-chip charge pump power supply

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Content

- Introduction and motivation of the work
- The design of cpVLAD (charge pump VcseL Array Driver)
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- Summary and the next steps
The problem that we set out to solve

Design challenge in VL+ pointed out in Jan Troska’s presentation in TWEPP2017:

At 8 mA and -35C, the forward voltage may rise close to be 2.5V, leaving no header room for the driving circuits.

Design challenges

- Largest unique challenge comes from ensuring sufficient voltage headroom for operation of VCSELs with 65 nm CMOS driver that limits voltage rail to 2.5 V
- Going cold and irradiating the VCSEL make the situation worse
- VCSEL forward voltage increases
- Need some voltage headroom for the driver’s output transistor
- Currently validating the margin we have for operation
The design, overall diagram and key features

- cpVLAD is based on VLAD14 (also reported in TWEPP2017), changed to follow the die-frame in VL+.
- The on-chip charge pump in each channel internally provides higher than 2.5V to the Output Buffer. This voltage follows the VCSEL’s forward voltage increase as the total dose accumulates, automatically controlled by the Feedback circuit.

Supply voltages: 1.2V and 2.5V only
A shared VCO provides the clock signal for each charge pump; clock signals are in different phase to reduce power noise.

Only 1.2V core devices are used in the whole design for considerations of radiation tolerance. Careful checks are performed to make sure that there is no overdriving violation in the power-up cycle.
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Supply voltages: 1.2V and 2.5V only
The design, the charge pump

- A simple and robust voltage doubler is chosen.
- The 800 MHz clock comes from the VCO. The frequency is chosen to reduce the capacitor area and voltage ripple.
- The charge pump can be disabled to send the 2.5V power supply to the output. In this case, the clock signal is also off.
Simulation of the charge pump power-up

Voltage is pumped to 3.2V 40 ns after power-up

Ripple of 15.8 mV proved not a problem
The design, the feedback circuit

• The negative feedback circuit keeps the voltage difference between the CP output and the anode of VCSEL constant when the VCSEL forward voltage changes. The voltage difference is also programmable by user.
• The dies of a MPW run arrived at CERN about 2 weeks ago. A few boards were assembled by CERN for electric and optical tests.
• Tests were carried out at CERN and at SMU. We report the preliminary results here.

Photo courtesy of Jan Troska (CERN)
• A voltage power supply V simulates the VCSEL forward voltage (Keithley 2410 is used, which can source or sink current).
• A scope is used to measure the output current over 50 ohm.

The input is PRBS $2^{31}-1$, differential, 100 mV_{p-p}.
• The input signal (at SMU) at 10 Gbps has a pre-emphasis that we cannot remove.
Testing, electric signals only
First eye diagram was from CERN

This is with the simulated forward voltage (Vout) at 2.8V. The eye is at 10 Gbps.
More eye diagrams from SMU

The reference channel (#3) without CP

1.8V  2.0V  2.2V  2.4V

The channel (#2) with CP on

1.8V  2.0V  2.2V  2.4V  2.6V  2.8V

3.0V  3.2V

Simulated forward voltage (V)
Probe the speed (designed for 10 Gbps)

The channel (#2) with CP on

10 Gbps
12 Gbps
14 Gbps
16 Gbps
Testing, the first glimpse of the optical eyes

At SMU we use a 3-D stage to bring the fiber to the VCSEL

An optical eye measured at CERN, through a coupler

An optical eye measured at SMU
Summary and the next steps

- Very preliminary test results about cpVLAD indicate that the prototype seems to work as designed. With 1.2 and 2.5V supply voltages, the driver functions with a simulated VCSEL forward voltage up to about 2.8V.

- If verified (with VCSEL in cold and after receiving the total dose), this design may provide a solution to the VL+ modules used in inner tracking systems.

- Not shown but checked: no measurable cross-talk among channels; the eye cross-point adjustment also functions as design. We ran one prototype over the weekend and measured it again Monday. We did not notice any changes.

- A lot more characterization will be carried out in the following weeks and months.

- After the function tests, we will perform irradiation tests up to the VL+ requirements.

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Thank you for your attention.